# Volume

# 1

TP4994E

# QUASI-DOPPLER RDF OPERATIONAL
# PROTOTYPE DESIGN

## VOLUME 1 : FINAL REPORT

by:

**Bayly Engineering Limited**
**167 Hunt Street, Ajax, Ontario**

Library and Information Centre /
Centre de Documentation (GSLA)
RECEIVED - REÇU LE
MAR 19 1986
Transport Canada / Transports Canada

October 1983

The contents of this report reflect the views of the contractor and not necessarily the official views or policies of the Transportation Development Centre.

## PROJECT TEAM

The project team involved in the Quasi-Doppler RDF Operational Prototype Design was comprised of:

| | |
|---|---|
| Z.A. Krajewski | Bayly, Ajax |
| F. Baehr | Bayly, Ajax |
| W. Ng | Bayly, Ajax |
| C. Lapointe | Bayly, Granby |
| D. Authier | Bayly, Granby |
| M. Lebeau | Bayly, Granby |

and supporting staff

# REPORT DOCUMENTATION FORM

| | | |
|---|---|---|
| **1. Transport Canada Report No.**<br>TP4994E | **2. TDC Project No.**<br>4822 | **3. Recipient's Catalogue No.**<br>36948 |

| | |
|---|---|
| **4. Title and Subtitle**<br>QUASI-DOPPLER RDF OPERATIONAL PROTOTYPE DESIGN<br>(2 VOLUMES) | **5. Report Date**<br>OCTOBER 1983<br>**6. Performing Organization Report No.**<br>290008 |
| **7. Author(s)**<br>BAYLY ENGINEERING LIMITED | **8. Transport Canada File No.**<br>D1455-133-5 |
| **9. Performing Organization Name and Address**<br>BAYLY ENGINEERING LIMITED,<br>167 HUNT STREET,<br>AJAX, ONTARIO<br>L1S 1P6 | **10. DSS File No.**<br>11SD.T8200-2-2541<br>**11. DSS or Transport Canada Contract No.**<br>0SD82-00122 |
| **12. Sponsoring Agency Name and Address**<br>TRANSPORTATION DEVELOPMENT CENTRE,<br>1000 SHERBROOKE STREET WEST, SUITE 2421,<br>MONTREAL, QUEBEC<br>H3A 2R3 | **13. Type of Report and Period Covered**<br>FINAL REPORT<br>NOVEMBER 1982-APRIL 1983<br>**14. Sponsoring Agency Code**<br>4822 |
| **15. Supplementary Notes**<br>VOLUME 1 : FINAL REPORT<br>VOLUME 2 : APPENDIX - TECHNICAL DESCRIPTION OF OPERATIONAL PROTOTYPE | **16. TDC Project Officer**<br>MICHA AVNI |

**17. Abstract**

The first part of this report describes work carried out on the original feasibility prototype VHF Radio Direction Finder developed under contract no. 1SD79-00129 with the target of identifying the problem areas and incorporating short-term changes so as to make the equipment operational.

The problem areas, and the subsequent remedial actions are described here, concluding in the final demonstration, and a listing of test results on the improved performance. Recommendations suggest the construction of a second prototype, built in the final engineering version.

The second part of the report is a documentation of the operational prototype "as is", comprising technical descriptions, specifications, circuit diagrams and test procedures. Two brief technical reports are also included, describing new developments incorporated in the improved equipment.

| | |
|---|---|
| **18. Key Words**<br>RADIO DIRECTION FINDER,<br>QUASI-DOPPLER | **19. Distribution Statement**<br>LIMITED NUMBER OF COPIES AVAILABLE FROM TRANSPORTATION DEVELOPMENT CENTRE, TRANSPORT CANADA |

| | | | |
|---|---|---|---|
| **20. Security Classification (of this report)**<br>UNCLASSIFIED | **21. Security Classification (of this page)**<br>UNCLASSIFIED | **22. No. of Pages**<br>410 | **23. Price**<br>NIL |

TDC/CDT 79-005

## FORMULE DE DOCUMENTATION POUR RAPPORT

**1. N° du rapport Transports Canada**
TP4994E

**2. N° de l'étude — CDT**
4822

**3. N° de catalogue du destinataire**
36948

**4. Titre et sous-titre**
QUASI-DOPPLER RDF OPERATIONAL PROTOTYPE DESIGN
(2 VOLUMES)

**5. Date du rapport**
OCTOBRE 1983

**6. N° du rapport de l'organisme exécutant**
290008

**7. Auteur(s)**
BAYLY ENGINEERING LIMITED

**8. N° de dossier Transports Canada**
D1455-133-5

**9. Nom et adresse de l'organisme exécutant**
BAYLY ENGINEERING LIMITED,
167 HUNT STREET,
AJAX, ONTARIO,
L1S 1P6

**10. N° de dossier — ASC**
11SD.T8200-2-2541

**11. N° de contrat — ASC ou Transports Canada**
0SD82-00122

**12. Nom et adresse de l'organisme parrain**
CENTRE DE DÉVELOPPEMENT DES TRANSPORTS,
1000 RUE SHERBROOKE OUEST, SUITE 2421,
MONTRÉAL, QUÉBEC
H3A 2R3

**13. Genre de rapport et période visée**
RAPPORT FINAL
NOVEMBRE 1982-AVRIL 1983

**14. Code de l'organisme parrain**
4822

**15. Remarques additionnelles**
VOLUME 1 : FINAL REPORT
VOLUME 2 : APPENDIX - TECHNICAL DESCRIPTION OF OPERATIONAL PROTOTYPE

**16. Agent de projet — CDT**
MICHA AVNI

**17. Résumé**

La première partie de ce rapport décrit les travailles exécuté sur le prototype de faisabilité original de radiogoniométre VHF développé pour le contrat no. 1SD79-00129 avec la butte de identifier les zones des problemes et incorporer les modifications a courte terme pour faire l'appareil fonctionner proprement.

Les zones des problèmes, et les actions de réperation conséquentes, sont décrit ici, terminant avec la démonstration finale et une liste des résultats des essais sur l'operation amélioré. Les recommandations suggére une construction de le deuxieme prototype construit en la version finale de génie.

La deuxieme partie de rapport est la documentation de prototype fonctionant "comme se trouve", contenant le descriptions techniques, les spécifications, les schémas de circuits et les procédures d'essais. Deux rapports techniques bréves sont compris aussi, décrivant les dévelopments nouveux employé dans l'appareil amélioré.

**18. Mots-clés**
RADIOGONIOMÈTRE
QUASI-DOPPLER

**19. Diffusion**
LE CENTRE DE DÉVELOPPEMENT DES TRANSPORTS DISPOSE D'UN NOMBRE LIMITÉ D'EXEMPLAIRES

**20. Classification de sécurité (de ce rapport)**
NON-CLASSIFIÉ

**21. Classification de sécurité (de cette page)**
NON-CLASSIFIÉ

**22. Nombre de pages**
410

**23. Prix**
NIL

# ACKNOWLEDGEMENTS

Bayly Engineering Limited gratefully acknowledges the advice and assistance of Transport Canada, Transportation Development Centre, in particular Mr. N.E. Rudback and Mr. M. Avni. The Company would also like to express its thanks to Mr. Z.A. Krajewski for his contribution to this report and field of direction finding.

## FOREWORD

This report provides a consolidated documentation on a Quasi-Doppler Radio Direction Finder System for Air Traffic Control. The Annex, Part 1 - Phase Detector Noise at the ±180° Threshold Points by Z.A. Krajewski, provides a detailed description on Phase Detector Noise and its effect on system accuracy as observed at, or near, ±180° threshold points. Also, a supplementary report, Microprocessor Correction of DF Antenna Readings due to Phase Detector Ambiguities forms Part 2 of the Annex. The Appendix (Volume 2) contains a Technical Description sub-divided into two sections - System Description and Unit Description, including circuit diagrams, etc.

## TABLE OF CONTENTS

VOLUME 1

| | | | Page |
|---|---|---|---|
| 1. | INTRODUCTION | | 1 |
| | 1.1 | Objective | 1 |
| | 1.2 | Work Program | 1 |
| 2. | DESIGN IMPROVEMENTS | | 2 |
| | 2.1 | Performance Review & Identification of Problem Areas | 2 |
| | 2.2 | Short-term Remedial Action | 2 |
| | 2.3 | Results of Tests on the Short-term Improvements | 3 |
| | 2.4 | Final Demonstration | 5 |
| | 2.5 | Recommendations and Conclusions | 5 |
| 3. | DOCUMENTATION | | 6 |

Annex

PART 1 Phase Detector Noise at the ±180° Threshold Points

PART 2 Microprocessor Correction of DF Antenna Reading due to Phase Detector Ambiguity

VOLUME 2 (separately bound)

APPENDIX Technical Description of Operational Prototype

# 1. INTRODUCTION

## 1.1 Objective

The overall objective of this task was to develop a doppler radio direction finder for fixed land based operation in the civilian air traffic control band of 117.5 MHz - 136.5 MHz, which will provide improved performance, greater reliability and lower cost, as compared with equipment presently in use by Transport Canada. More specifically, it was required to provide specifications and circuit details of an operational prototype quasi-doppler VHF radio direction finder designed for air traffic control applications.

## 1.2 Work Program

In order to meet the above objectives, the work under this contract was divided into two parts:

i) Review of design and performance of the equipment developed under contract no. 1SD79-00129 and tested in September 1982, identification of problem areas and short-term design changes to improve performance of the prototype to make it operational.

ii) Documentation of technical descriptions, specifications, circuit diagrams and test procedures of the operational prototype.

The first part of the program was planned for the months of September through December 1982, aiming at completion before the weather made it difficult to carry on with the field tests. The second part of the task was completed in-house by the Company personnel of the Granby and Ajax plants as soon as the design changes were finalized.

## 2. DESIGN IMPROVEMENTS

### 2.1 Performance Review & Identification of Problem Areas

Analysis of the test results obtained in the September 1982 demonstration (see Final Report No. TP4993E entitled Installation, Commissioning and Testing of Doppler Radio Direction Finder, dated October 1983) has shown the following areas where the equipment has failed to meet the target specifications:

i) Insufficient sensitivity of the DF system.

ii) DF accuracy - a consistent quadrantal error was shown at all frequencies when the target transmitter was moved around the DF antenna. This was accompanied by a constant zero shift.

iii) An operational discontinuity in a close vicinity of the 270° azimuth.

iv) Wide scatter of bearing readings in the presence of noise and interference.

v) System test facility not operational.

vi) In addition, difficulties were encountered in operation of the channel and frequency selection pushbuttons.

### 2.2 Short-term Remedial Action

A check on the equipment revealed a short circuit due to a loose drop of solder in one of the receiver channels, the removal of which has restored the full sensitivity (item i).

As regards the quadrantal error shown in the DF accuracy measurements, there remained a question as to whether its source was internal, due to the system design, or external, i.e. due to the field site effects. To be able to separate these effects, it was decided to design and construct a rotary mounting base for the DF antenna structure, which would allow rotation of the antenna array on its vertical axis, while the target transmitter remained in a fixed position. The zero offset was corrected immediately by adjustment of a control switch, already provided.

The 270° azimuth discontinuity was discovered to be an omission in the bearing processor software to allow for averaging of bearing readings over the 0°/360° threshold. Provision for an alternative program path has completely eliminated this problem.

The phase detector circuit, which measures the phase difference between the two DF receiver channel outputs, was found to be drifting with temperature and to suffer from inadequate linearity. The net effect was that of introducing additional bearing errors due to the warming up of the equipment and due to scatter in presence of noise and outside interference. The phase detector circuit was redesigned to provide linearity better than 0.1% and to give a stable d.c. output reference.

Measurements were made on the system self-test facility, which consisted of 4 test injection antenna elements, and a test generator. A conclusion was drawn that this method of testing cannot be made to operate without major re-routing and shielding of cables and drastic measures to improve radio frequency interference isolation between the modules. This could be solved only by repackaging the equipment.

The frequency selection pushbuttons were found to give multiple pulses of microsecond duration when pushed in and the encoding circuits were fast enough to record it. The trouble was removed easily by the addition of capacitors to slow down the triggers.

### 2.3 Results of Tests on the Short-term Improvements

On completion of the above improvements, the DF system was again tested, this time with the antenna array installed on the rotary mounting. A set of DF accuracy tests was performed and the new results were examined. The bearing readings were now more consistent and the 270° discontinuity had been eliminated. However, it has been shown that the previously observed quadrantal error was still appearing in the test by antenna rotation, indicating that it was a part of the instrumental performance of the system. This error was steady and repeatable, hence it was proposed to correct it automatically by programming a software correction in accordance with a set of calibration results which would be obtained on installation.

Such a calibration chart was drawn up and a calibration correction program was included in the software of the second microprocessor of the Bearing Processor sub-system. The results of the DF accuracy readings, after the automatic correction, are shown in Fig. 1, as obtained in a test on December 16, 1982. The instrumental bearing errors were now contained in the ±3° limits, but the noise scatter of the readings was still pronounced, reaching ±1.5° at the maximum sensitivity setting.

The centre test frequency, allocated for the tests by the Department of Communications, has proven troublesome on two accounts: this frequency is the air navigation channel for the Trenton Airport and occasional transmissions were being picked up, causing interference with the tests. Secondly, a spurious response was found in the DF receiving system at a frequency of 128.8 MHz, equal to the fourth harmonic of the second local oscillator (32.2 MHz). The spurious interference was also causing some breakthrough at the test frequency of 128.7 MHz. To demonstrate these effects, tests were made outside the sources of interference at 127.6 MHz and at 127.9 MHz and the sensitivity was shown to be normal.

46 1323

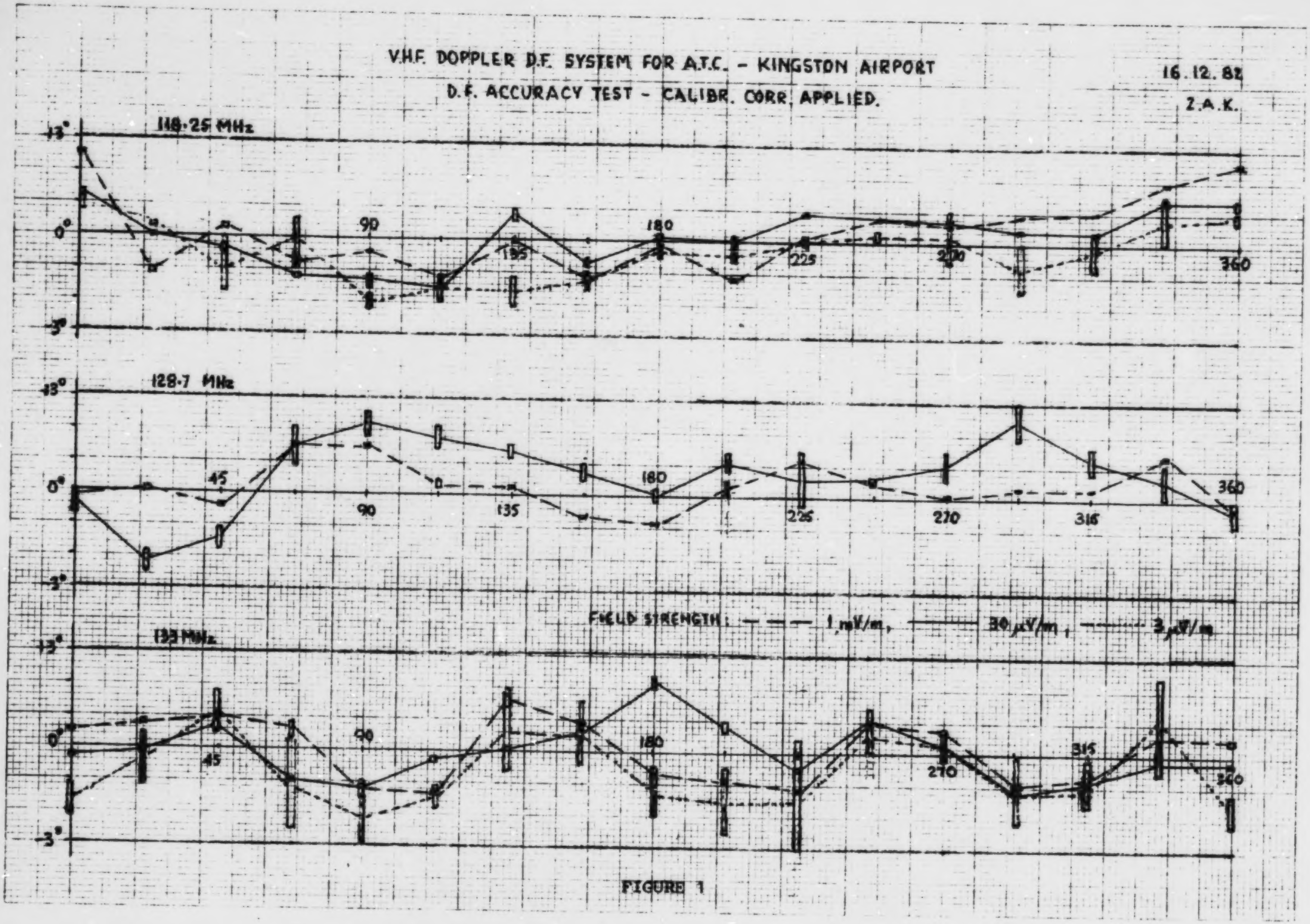


FIGURE 1

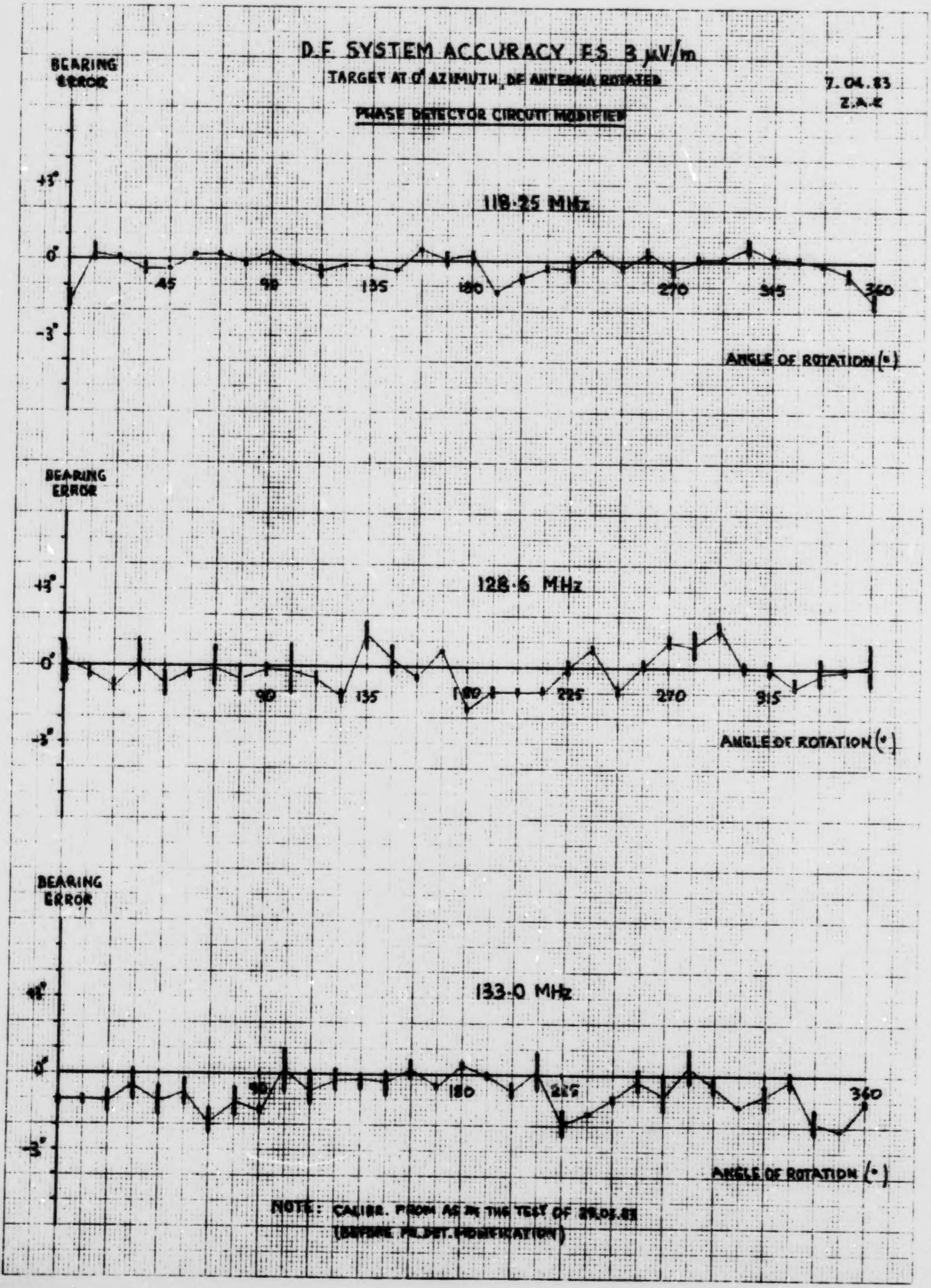
## 2.4 Final Demonstration

The performance of the system was again checked in January and in February 1983, showing substantially the same results. Finally, a demonstration was arranged for Transport Canada at the end of March 1983, the results of which can be seen in Appendix 2 of the Final Report on Installation, Commissioning and Testing, No. TP4933E, dated October 1983. One problem showed up during the demonstration - measurements at 11.25° intervals (not previously tested) displayed noise errors due to the discontinuity of the phase detector. The phase detector was modified to take care of this noise and the DF accuracy tests were repeated in April 1983, showing the final achievements obtained with the first prototype. The final test results are shown here in Figs. 2-4, clearly indicating the improvements since 1982.

## 2.5 Recommendations and Conclusions

Performance of the first prototype shows it to be operational for the ATC purposes, however, it leaves considerable scope for improvement in reaching the complete target specifications. Further improvements to this prototype are difficult, owing to the build-up of consecutive modifications and the wear and tear on the connectors, wiring and the component parts. It is, therefore, recommended that a second model be constructed, which will incorporate all the latest improvements and also allow for additional design changes to meet the performance features, as yet not realized.

FIGURE 2



46 1513

10 X 10 TO THE CENTIMETER

FIGURE 3

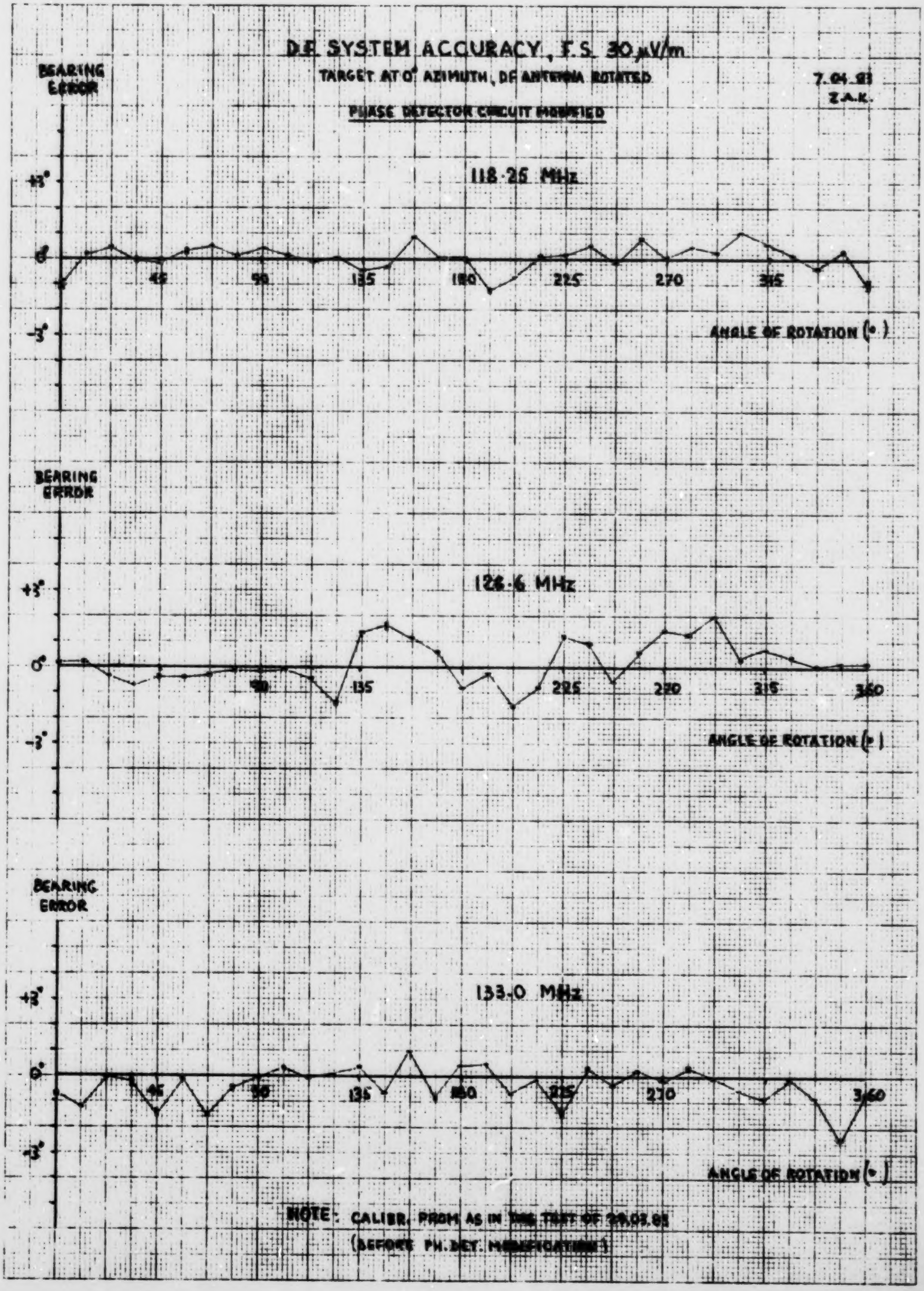
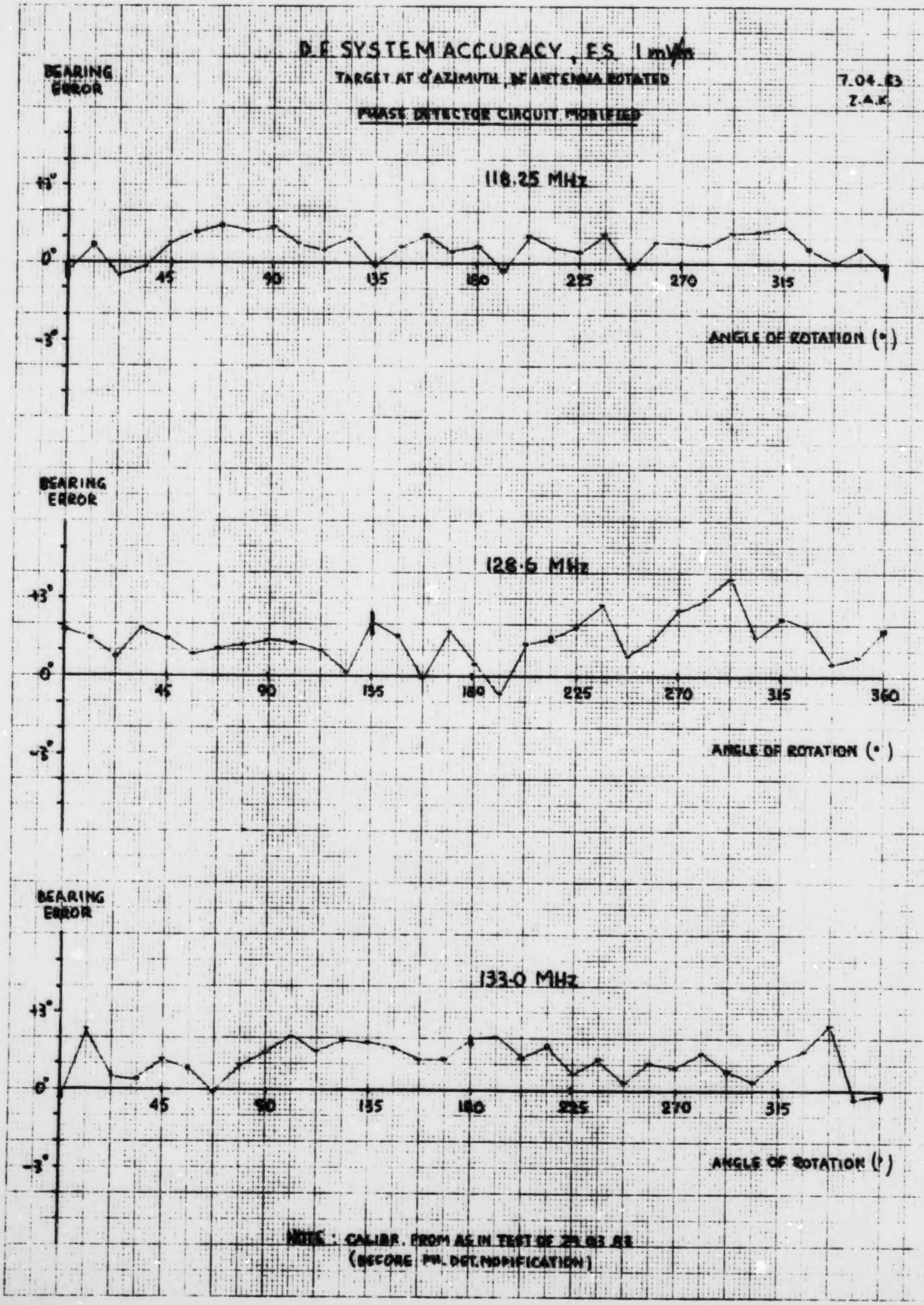

D.F. SYSTEM ACCURACY, F.S. 30 µV/m
TARGET AT 0° AZIMUTH, DF ANTENNA ROTATED
PHASE DETECTOR CIRCUIT MODIFIED
7.04.83
Z.A.K.
BEARING ERROR
+3°
0°
-3°
118·25 MHz
45
90
135
180
225
270
315
ANGLE OF ROTATION (°)
BEARING ERROR
+3°
0°
-3°
126·6 MHz
90
135
225
270
315
360
ANGLE OF ROTATION (°)
BEARING ERROR
+3°
0°
-3°
133.0 MHz
45
90
135
180
225
270
360
ANGLE OF ROTATION (°)
NOTE: CALIBR. PROM AS IN THE TEST OF 29.03.83
(BEFORE PH.DET. MODIFICATION)

FIGURE 4


D.F. SYSTEM ACCURACY , E.S. 1 mV/m

TARGET AT 0° AZIMUTH , DF ANTENNA ROTATED

7.04.83
Z.A.K.

PHASE DETECTOR CIRCUIT MODIFIED

NOTE : CALIBR. FROM AS IN TEST OF 29.03.83
(BEFORE PH. DET. MODIFICATION)

46 1513

K-E 10 X 10 TO THE CENTIMETER
KEUFFEL & ESSER CO.

## 3. DOCUMENTATION

The second part of the contract concerns preparation of technical descriptions, specifications, circuit diagrams, and alignment procedures of the operational prototype equipment, as improved in the first part of this assignment.

The documentation is divided into two sections:

i) System description and specification, and the descriptions of functional sub-systems and their respective interface specification. This section includes functional block diagrams drawn up to make it easier to understand the principles of operation of the system.

ii) Detailed circuit schematics with descriptions of operation and procedures of alignment and testing. This section also includes algorithms and software programs of the microprocessors forming part of the system.

The enclosed documentation completes the record on the 'as is' status of the operational prototype.

# ANNEX

## TABLE OF CONTENTS

Page

### PART 1

### Phase Detector Noise at the +180° Threshold Points

Introduction 1

The Problem of Crossing the Phase Detector Discontinuity 1

Cause of the Problem 3

Solution 3

### PART 2

### Microprocessor Correction of D.F. Antenna Reading due to Phase Detector Ambiguity

Abstract 5

Introduction 5

Description of the System 6

Correction Algorithm 6

Control of the Phase Detector 7

Trouble due to the Interrogator 8

References 13

# ANNEX

## PART 1

## PHASE DETECTOR NOISE AT THE +180° THRESHOLD POINTS

### INTRODUCTION

The Quasi-Doppler VHF Direction Finding System operates on the principle of analyzing the waveform of phase difference between pairs of adjacent dipoles scanned sequentially around the array. With sixteen dipoles, the waveform contains sixteeen steps which are available for sampling and for Fourier analysis by means of the bearing processor. This procedure can be carried out easily using a linear phase detector as long as the max./min. deviation does not exceed 360°. In practice, local reflections in the antenna structure, plus an accumulation of noise phase jitter and constant offsets cause the peaks of the phase detector output waveform to cross occasionally the ±180° linearity limits. An ingenious method for counteracting this tendency has been devised by this Company, as described in the Technical Memo by S. Karius and D. Vakili, dated December 6, 1982. In this method, a preliminary scan sample is taken and examined to decide which pulses are likely to approach the linearity limit and to program a microprocessor to direct reversal of the phase detector by 180° for the duration of such pulses in the set number of next (measurement) scans.

### The Problem of Crossing the Phase Detector Discontinuity

The above system was installed in the prototype and found to operate correctly over a range of ±230° except for pulses in the close vicinity of +180° or -180°.

At these points the phase detector output has a tendency to fluctuate widely between +180° and -180° with a random frequency anywhere between 4.8 kHz and 100 kHz. The average value of such a noise is near zero degrees and, therefore, no command can be given to reverse the phase detector. The net result is a wrong sample readout for the 'noisy' pulse, giving a bearing error of some 4° to 9° (compare Fig. 1). The problem was foreseen in the original design of December 1982 and a special noise detector or 'window comparator' was added to sample the fluctuations in the vicinity of 180° (say, 170° to 180°) (see the last paragraph of the report quoted on page 4, 'Trouble due to the Integrator'). However, operation of this 'window comparator' was not 100% successful which led to further investigation.

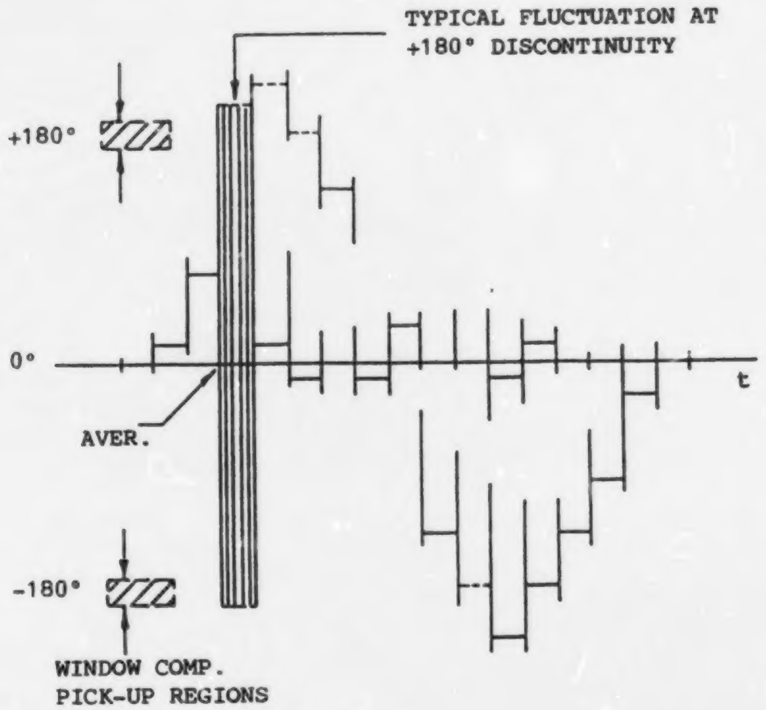

TYPICAL FLUCTUATION AT
+180° DISCONTINUITY
+180°
0°
t
AVER.
-180°
WINDOW COMP.
PICK-UP REGIONS

FIG. 1

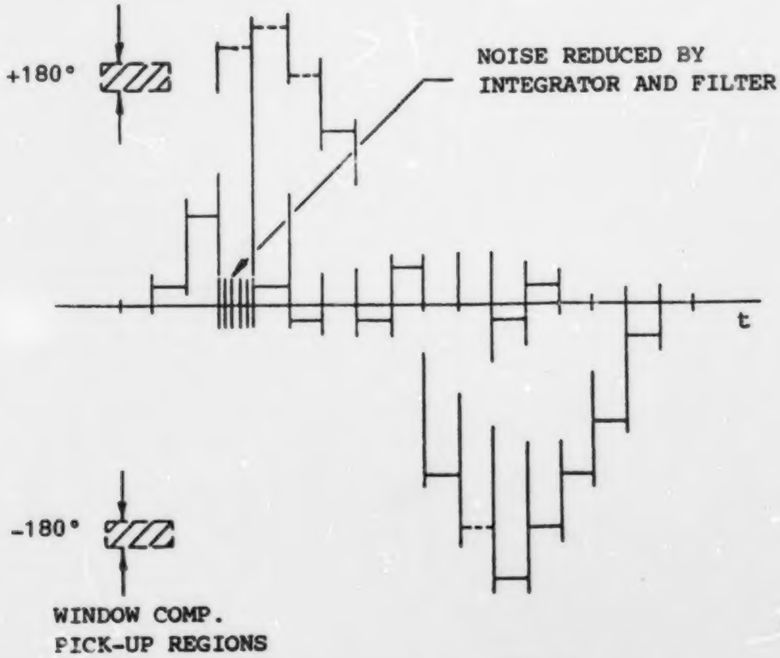

NOISE REDUCED BY
INTEGRATOR AND FILTER
+180°
t
-180°
WINDOW COMP.
PICK-UP REGIONS

FIG. 2

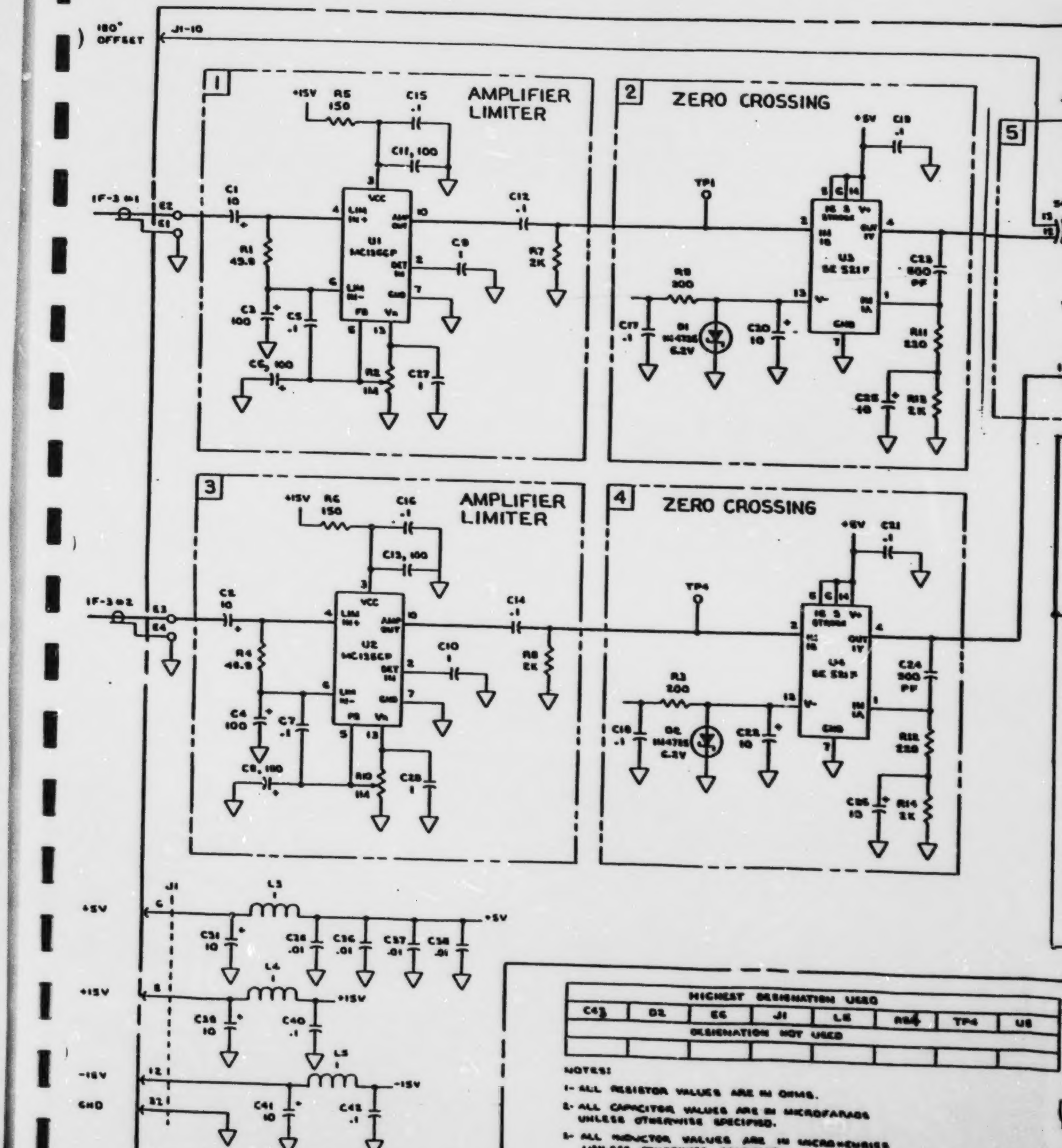
## Cause of the Problem

The phase detector waveform was investigated at some 'bad' target positions and frequencies where the bearing error was quite pronounced. In each case, the 'noisy' pulse was identified and the cause of the 'noise' was proved by eliminating it by means of shifting the zero axis of the phase detector. The 'window comparator' was found operating only when the noise was entering its pick-up region which was only in a small percentage of cases. The interesting fact observed was that the peak-to-peak noise amplitude was reduced by about 15 dB from its original ±180° swing (see Fig. 2). A quick calculation showed that this was due to the Integrator/Filter section (Item 6 on the attached circuit diagram), since the 'window comparator' input was taken from the same point as the bearing processor input.

## Solution

In order to make the 'window comparator' operative in all 'noise' cases, it was necessary to apply to it the phase detector output with a considerably wider bandwidth, so that the noise peaks could reach or even cross the 180° line limit. This was obtained by tapping the phase comparator flip-flop (Item 5) in parallel to the filter input and to provide a separate integration network with a time constant six times shorter than that for the bearing processor. An operational amplifier (Item 8) was added to bring up the level to that necessary to drive the 'window comparator'.

After initial adjustment, the circuit now correctly inverts the ±180° pulses, thus eliminating the 'noise' bearing errors without failure.


180° OFFSET
J1-10
1
AMPLIFIER LIMITER
2
ZERO CROSSING
3
AMPLIFIER LIMITER
4
ZERO CROSSING
5
IF-3 #1
IF-3 #2
E1
E2
E3
E4
+15V
R5 150
R6 150
C15 .1
C16 .1
C11, 100
C13, 100
C1 10
C2 10
R1 49.9
R4 49.9
U1 MC1355P
U2 MC1355P
C3 100
C4 100
C5 .1
C7 .1
C6, 100
C8, 100
R2 1M
R10 1M
C27 1
C28 1
C9 1
C10 1
C12 .1
C14 .1
R7 2K
R8 2K
TP1
TP4
+5V
C19 .1
C21 .1
U3 SE 521F
U4 SE 521F
R9 200
R3 200
D1 1N4735 6.2V
D2 1N4735 6.2V
C17 .1
C18 .1
C20 10
C22 10
C23 300 PF
C24 300 PF
R11 220
R12 220
R13 2K
R14 2K
C25 10
C26 10
J1
L3
L4
L5
+5V
+15V
-15V
GND
C31 10
C35 .01
C36 .01
C37 .01
C38 .01
C39 10
C40 .1
C41 10
C42 .1

| HIGHEST DESIGNATION USED | | | | | | | |
|---|---|---|---|---|---|---|---|
| C43 | D2 | E6 | J1 | L5 | R24 | TP4 | U6 |
| DESIGNATION NOT USED | | | | | | | |
| | | | | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES UNLESS OTHERWISE SPECIFIED.

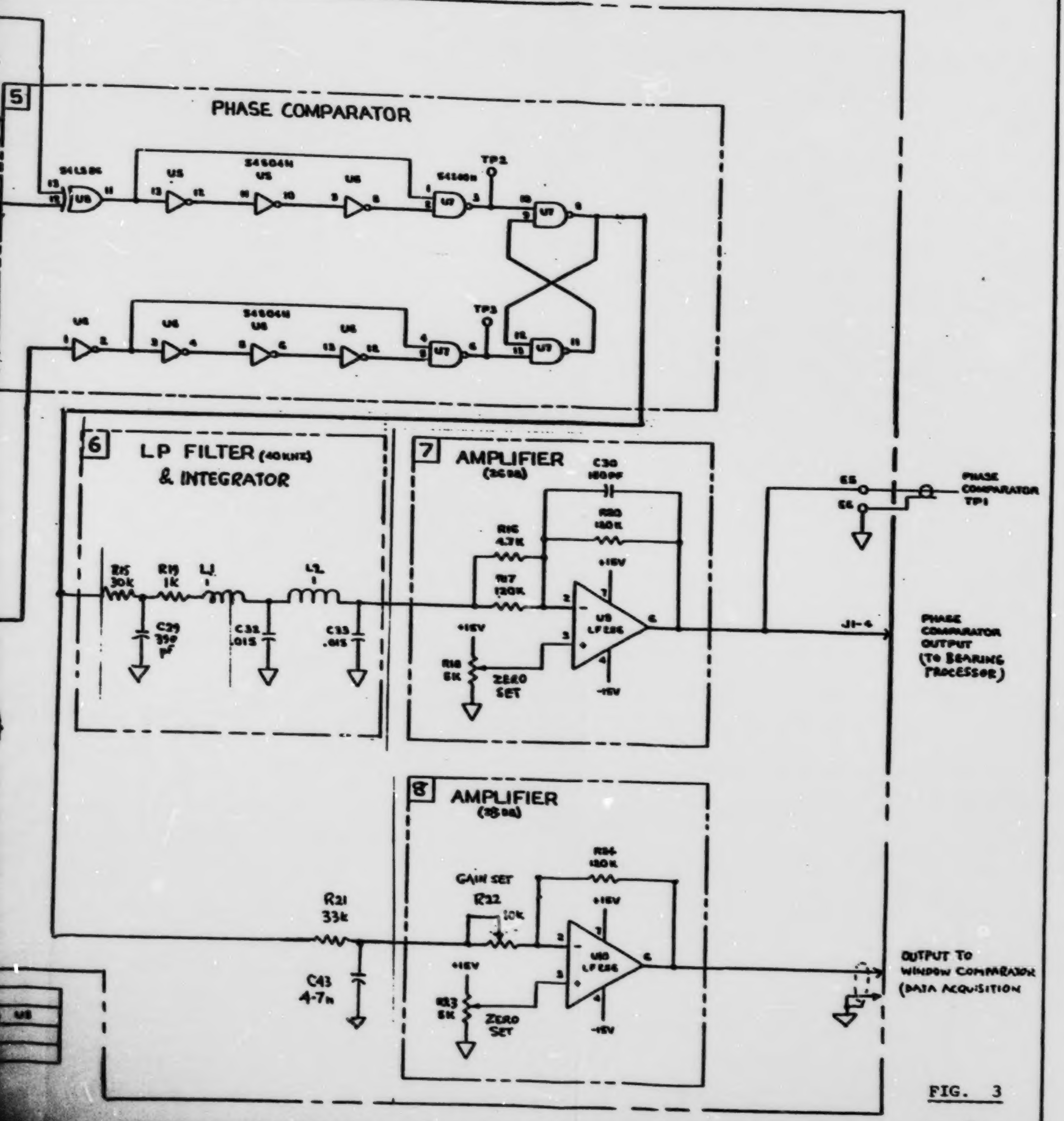

5
PHASE COMPARATOR
54LS86
U8
13
12
11
U5
13
12
54S04N
U5
11
10
U6
9
8
54S00N
U7
1
2
3
TP2
10
9
U7
8
U6
1
2
U6
3
4
54S04N
U6
5
6
U6
13
12
4
5
U7
6
TP3
12
13
U7
11
6
LP FILTER (40KHZ)
& INTEGRATOR
R15
30k
R19
1k
L1
1
L2
1
C29
390
pF
C32
.015
C33
.015
7
AMPLIFIER
(26DB)
C30
180PF
R20
180K
R16
4.7K
R17
120K
+15V
2
3
U9
LF256
6
7
4
+15V
R18
5K
ZERO
SET
-15V
E5
E6
PHASE
COMPARATOR
TP1
J1-4
PHASE
COMPARATOR
OUTPUT
(TO BEARING
PROCESSOR)
8
AMPLIFIER
(28DB)
R24
120K
GAIN SET
R22
10k
R21
33k
C43
4.7n
+15V
2
3
U10
LF256
6
7
4
+15V
R23
5K
ZERO
SET
-15V
OUTPUT TO
WINDOW COMPARATOR
(DATA ACQUISITION
U8

FIG. 3

| IC'S SUPPLY DISTRIBUTION | | |
|---|---|---|
| DESIGNATION | GND | +5V |
| [illegible] | PIN 7 | PIN 14 |

BAYLY

SCHEMATIC DIAGRAM
PHASE COMPARATOR

# ANNEX

## PART 2

## MICROPROCESSOR CORRECTION OF D.F. ANTENNA READING DUE TO PHASE DETECTOR AMBIGUITY

### ABSTRACT

A Digital Correction Procedure is presented for correction of the ambiguous phase detector readings of the Doppler Direction Finder. The ambiguity is due to the phase detector sensing of angles outside the -180° to 180° range.

Such large phase angles may occur because of the large antenna dipole spacing designed for higher sensitivity, further augmented by noise and harmonic distortions of the antenna patterns.

### INTRODUCTION

For increasing the sensitivity of the DF antenna, an increased dipole spacing is very desirable. However, such an increase causes ambiguity in the sensing of the dipole phase difference signal by a linear phase detector when the phase angle exceeds ±180°. This is because such detections normally produce readout for one cycle only (-180° to +180°). The phase angles out of this range are folded back producing readouts within the above range, i.e. with a 360° error.

The method commonly used is to design the dipole spacing for 120° maximum phase difference (ref. 1). This leaves 60° margin for noise and other distortions. However, unpredicted noise, harmonic deformation, antenna assymetry, and field effects may cause the phase signal to exceed -180° to +180° range, even for such optimum designs.

A correction on the phase detector output must, therefore, be done to improve the accuracy of the direction finder.

In a digital D.F. system, such a correction is best applied after the sampling and digitizing of the phase detector readout. This is desirable both from an accuracy and implementation points of view.

Following, a typical Digital D.F. system and the correction method are described.

## DESCRIPTION OF THE SYSTEM

In Fig. 4, a typical Doppler D.F. system is shown with a digital bearing angle acquisition processor (ref. Fig. 5). Here, the dipoles of a circular array antenna are selected in pairs, and the signals out of the last IF stages of the two receivers are compared in phase. To reduce the effects of noise, the phase is integrated for a time window which covers the flat and transient free part of the time a particular dipole pair is selected - Fig. 5. The result of this integration, which is proportional to the phase difference for the selected pair, is sampled and digitized (by an A to D converter) and is brought out to the digital filter and bearing angle calculator.

The correction to be discussed should be applied after the A-D converter, and before the calculation of the bearing angle.

This corrector is a small microprocessor (Intel 8048 is used in the Bayly Engineering DF system). It observes the phase signal for one scan (reference scan) and identifies the samples to be corrected. These samples are then corrected and brought out to the angle calculator in the course of the following n scans (measurement scans) where n is the averaging constant over which the findings of the measurement scans are averaged. Therefore, each DF cycle consists of one reference scan and n measurement scans.

## CORRECTION ALGORITHM

The algorithm to identify the samples to be corrected is based on the assumption that the original phase signal, before the phase detector, never exceeds 240°. This is about twice the design value of 120° and is a reasonable practical assumption.

Under such an assumption, the folded back phase of the phase detector output falls in the 120° to 180° (or -120° to -180°) region - Fig. 6. Therefore, comparing the incoming sample levels to ±120° identifies the samples to be corrected (bad samples) and the samples not to be corrected (good samples). An attempt would be made to correct the bad samples in the following measurement scans.

The correction is accomplished by controlling of the phase detector by the corrector microprocessor. This is done by shifting the phase detector range from -180° to 180° to 0 to 360° (or -360° to 0), as explained later.

As a result of the range shifting, the portions of the signal prone to foldback will be detected as shifted by 180° but, as a whole, with no swap and foldbacks - Fig. 7. These portions would be corrected in the measurement scans, by adding, or subtracting, 180° from the samples before feeding them to the angle calculation.

To decide which samples should be added and which subtracted at 180° in the above correction, the relative position of the sample is required with respect to the main positive zero crossing of the signal. This zero crossing is, in fact, roughly equal to the target angle (bearing angle) and is calculated by the angle calculator in the previous measurement scan. It is reported as feedback to the corrector microprocessor in the reference scan.

The rule for deciding whether to add or subtract is to add 180° for samples to the right of the above discussed zero crossing (up to half the total number of samples) but to subtract otherwise.

The above procedure, however, suffers from the lack of zero crossing report in the very first reference scan at the power up. Therefore, an initialization scan is required at the power up of system. During this scan, the corrector microprocessor does nothing on the incoming samples but just passes them to the angle calculator. The target calculation, in this initialization scan, is used in the next scan of the DF which is a reference scan. A diagram of the scans which the DF system encounters during its cyclic operation is shown in Fig. 8.

## CONTROL OF THE PHASE DETECTOR

A block diagram of the phase detector used in Bayly Engineering DF system is shown in Fig. 9. It consists of two limiter amplifiers, two edge detectors, and an R.S. flip-flop. The limiters convert the receiver final IF stage outputs to square waves, and the flip-flop is set by the positive edge of the output of one channel and negative edge of the other. Therefore, the flip-flop produces a pulse with a duty cycle proportional to the phase difference angle of the two receivers, i.e. for a phase angle change linearly from -180° to +180° the duty cycle changes from 0 to 100%. The following integrator stage converts this duty cycle to a DC voltage output.

To shift this detector from -180° to 180° range to 0 to 360° range, it is sufficient to make use of positive edge detection in both channels rather than set the flip-flop with positive edge of the output of one channel and negative edge of the other.

Moreover, to make the phase detector controllable, one of the edge detectors should be made switchable from positive to negative, or vice versa, by a selector, driven by a digital input line. This is done on the phase detector of Fig. 9 as modified in Fig. 10, i.e. for control input S high, the range of the detector is -180° to +180° and for S - low, the range is 0° to 360° (or -360° to 0).

## TROUBLE DUE TO THE INTEGRATOR

The portions of the phase signal in the vicinity of ±180° can have noise spikes which may, or may not, fold back at the output of the phase detector. The phenomenon after integration produces averaged readouts in the good sample region (-120° to 120°) and no attempt could be made to correct them.

To avoid the problem, a window comparator is used to sense the output of the phase comparator. This window comparator, upon sensing a readout close to -180° or 180° (say, over 170°), during the integration window produces an interrupt to the corrector microprocessor. This interrupt identifies the sample as a bad sample, to be corrected even if the microprocessor senses it as a good sample by comparing the integrated reading to ±120°.

The overall correction scheme is block diagrammed in Fig. 11.

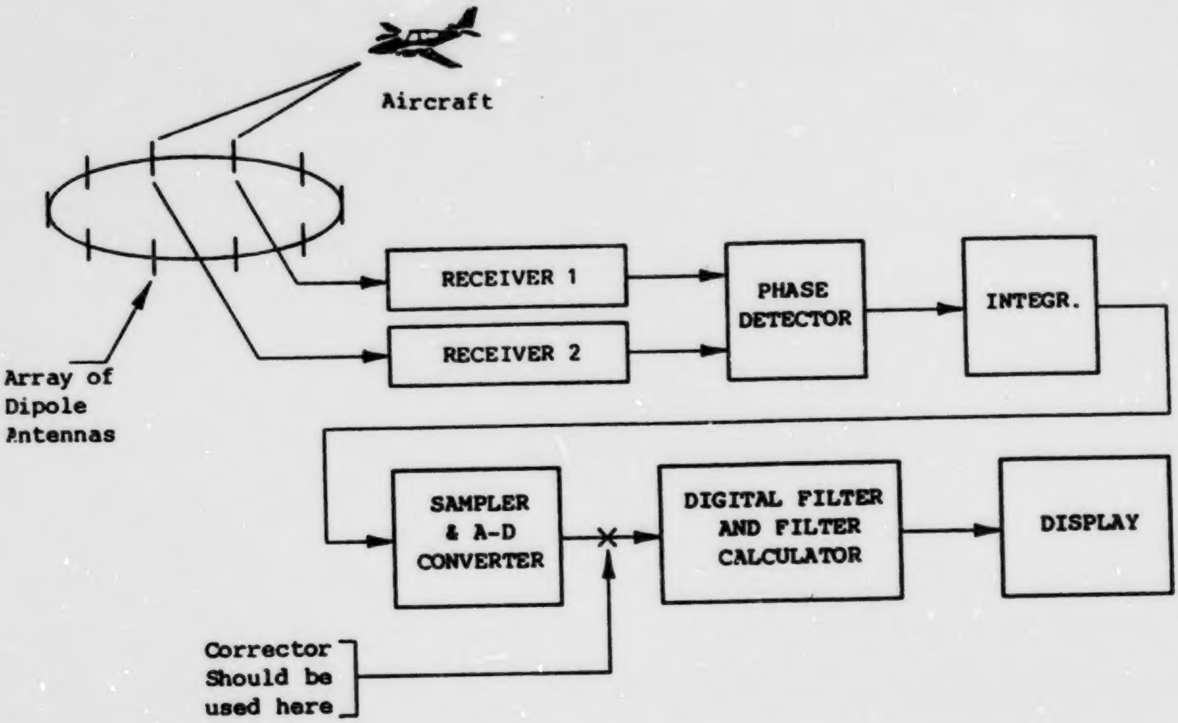

Aircraft
Array of Dipole Antennas
RECEIVER 1
RECEIVER 2
PHASE DETECTOR
INTEGR.
SAMPLER & A-D CONVERTER
DIGITAL FILTER AND FILTER CALCULATOR
DISPLAY
Corrector Should be used here

FIG. 4 : TYPICAL DIPOLE ARRAY D.F. SYSTEM WITH DIGITAL BEARING ANGLE CALCULATOR

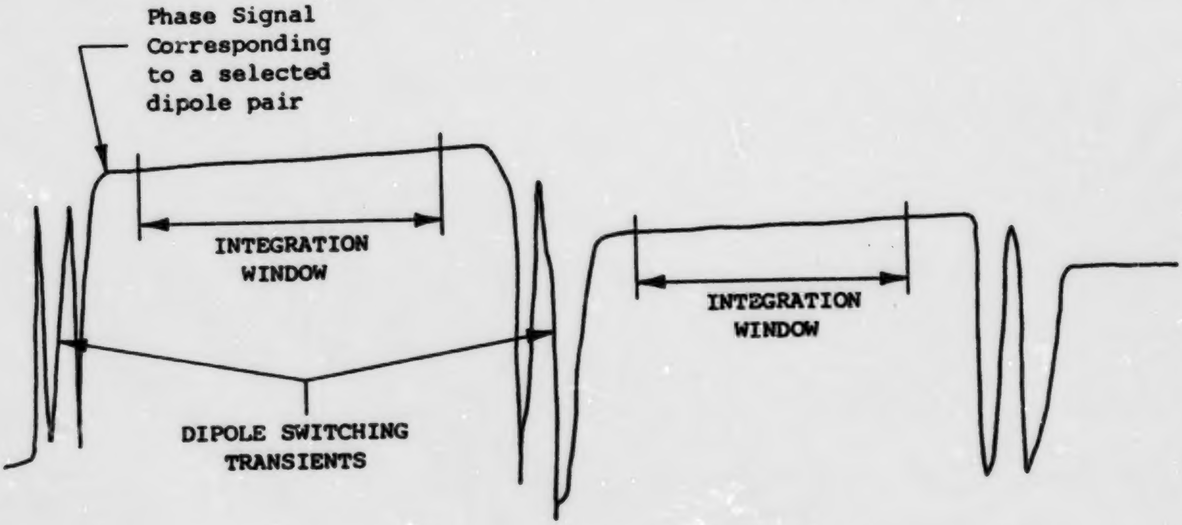

Phase Signal Corresponding to a selected dipole pair
INTEGRATION WINDOW
INTEGRATION WINDOW
DIPOLE SWITCHING TRANSIENTS

FIG. 5 : THE PHASE DETECTOR READOUT IS INTEGRATED FOR THE FLAT AND TRANSIENT FREE PORTION OF A SELECTED DIPOLE PAIR TIME

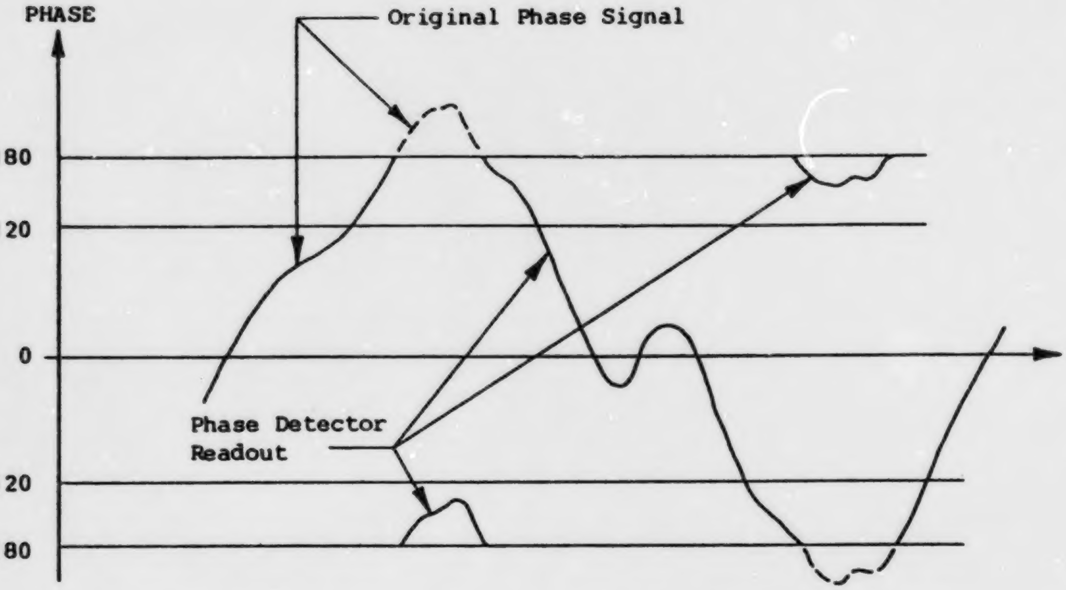

PHASE
Original Phase Signal
180
120
0
Phase Detector
Readout
-120
-180

FIG. 6 : FOLDING BACK OF PORTIONS OR ORIGINAL PHASE SIGNAL WHICH EXCEEDS ±180°

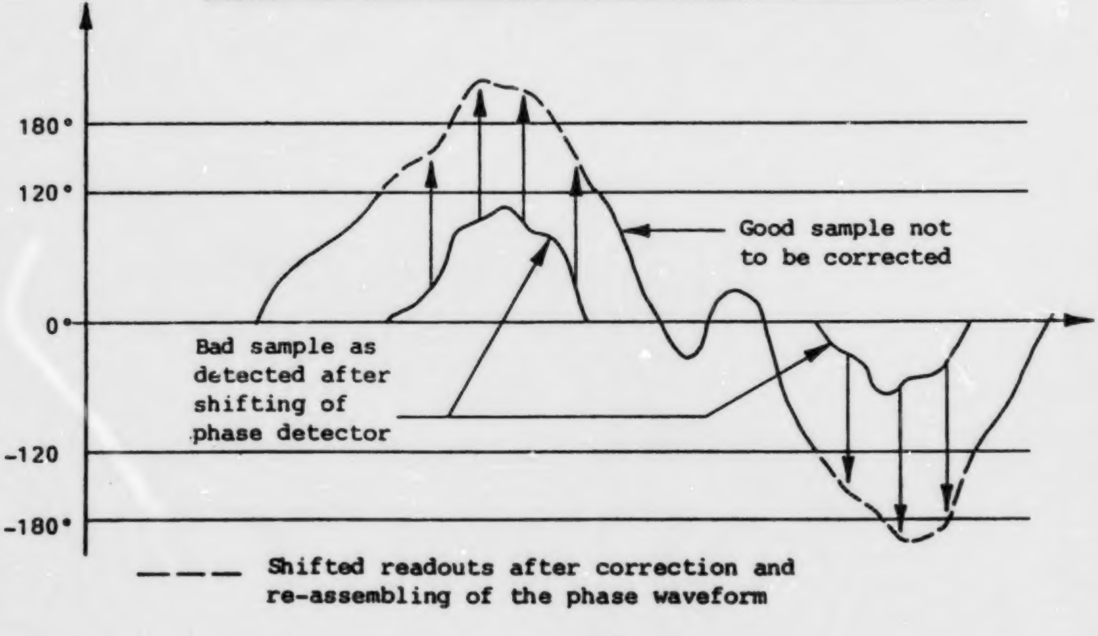

180°
120°
Good sample not
to be corrected
0°
Bad sample as
detected after
shifting of
phase detector
-120
-180°
Shifted readouts after correction and
re-assembling of the phase waveform

FIG. 7 : SHIFTING AND CORRECTION OF PORTIONS OF WAVEFORM PRONE TO SWAPS

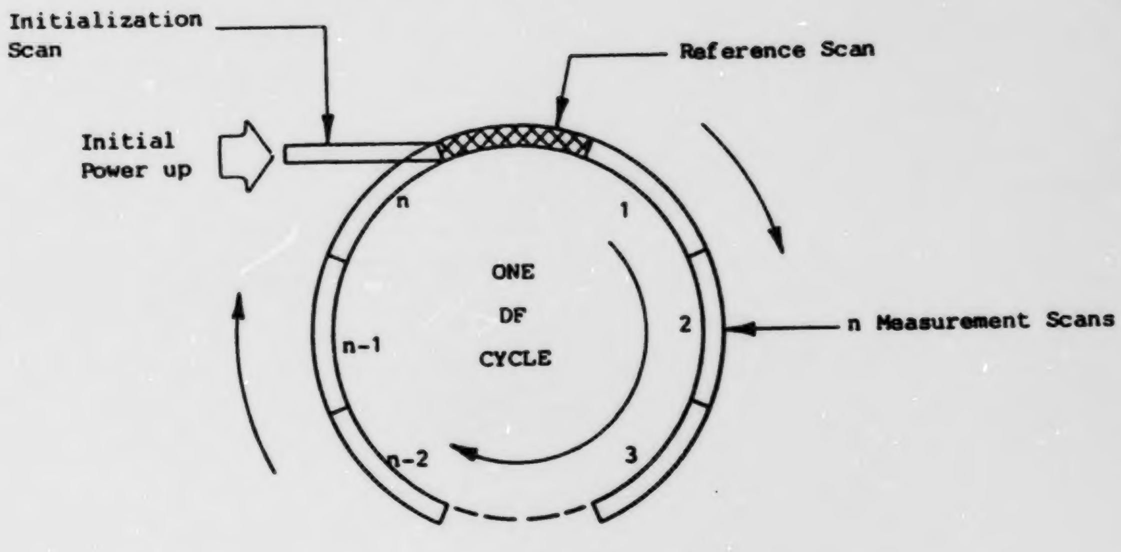

Initialization Scan
Reference Scan
Initial Power up
n
1
ONE
DF
CYCLE
2
n Measurement Scans
n-1
n-2
3

FIG. 8 : SCANS OF ONE CYCLE OF D.F. SYSTEM

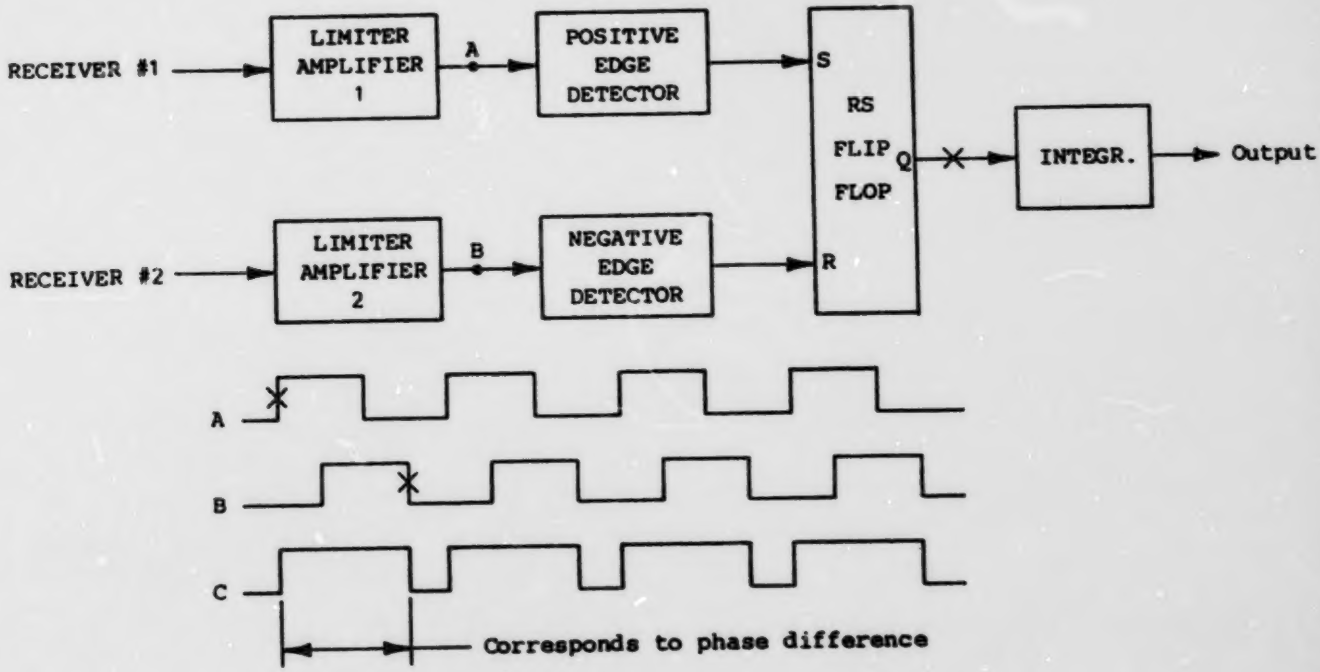

RECEIVER #1
LIMITER AMPLIFIER 1
A
POSITIVE EDGE DETECTOR
S
RS FLIP FLOP
Q
INTEGR.
Output
RECEIVER #2
LIMITER AMPLIFIER 2
B
NEGATIVE EDGE DETECTOR
R
A
B
C
Corresponds to phase difference

FIG. 9 : PHASE DETECTOR USED IN THE DF SYSTEM

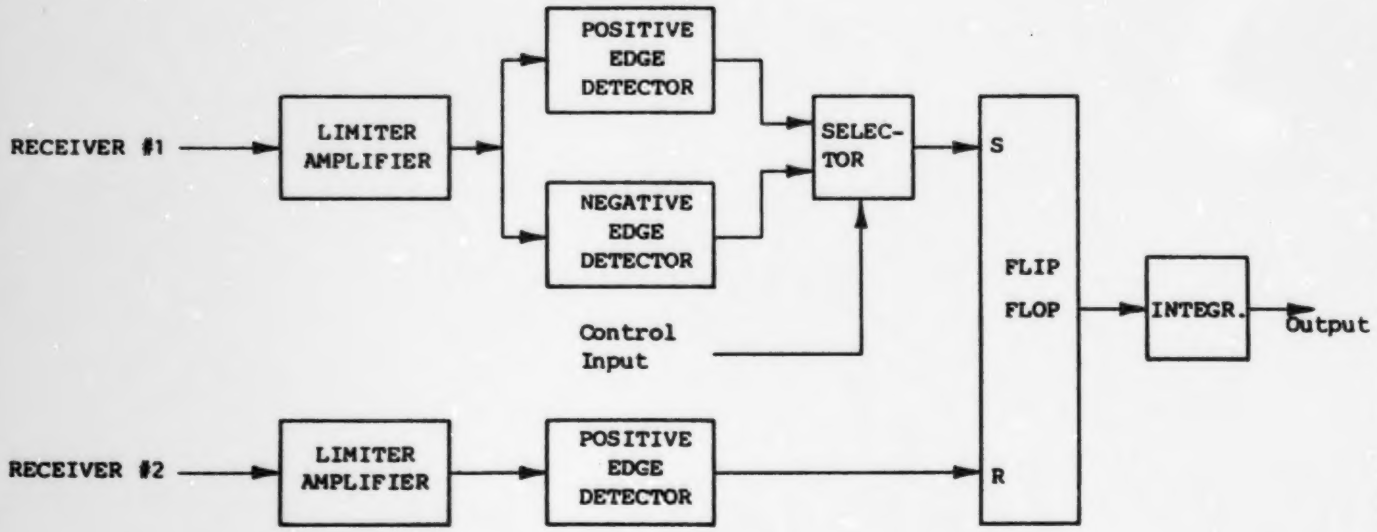

RECEIVER #1
LIMITER AMPLIFIER
POSITIVE EDGE DETECTOR
NEGATIVE EDGE DETECTOR
SELEC-TOR
S
FLIP FLOP
INTEGR.
Output
Control Input
RECEIVER #2
LIMITER AMPLIFIER
POSITIVE EDGE DETECTOR
R

FIG. 10 : PHASE DETECTOR MODIFIED TO BE RANGE SHIFTABLE

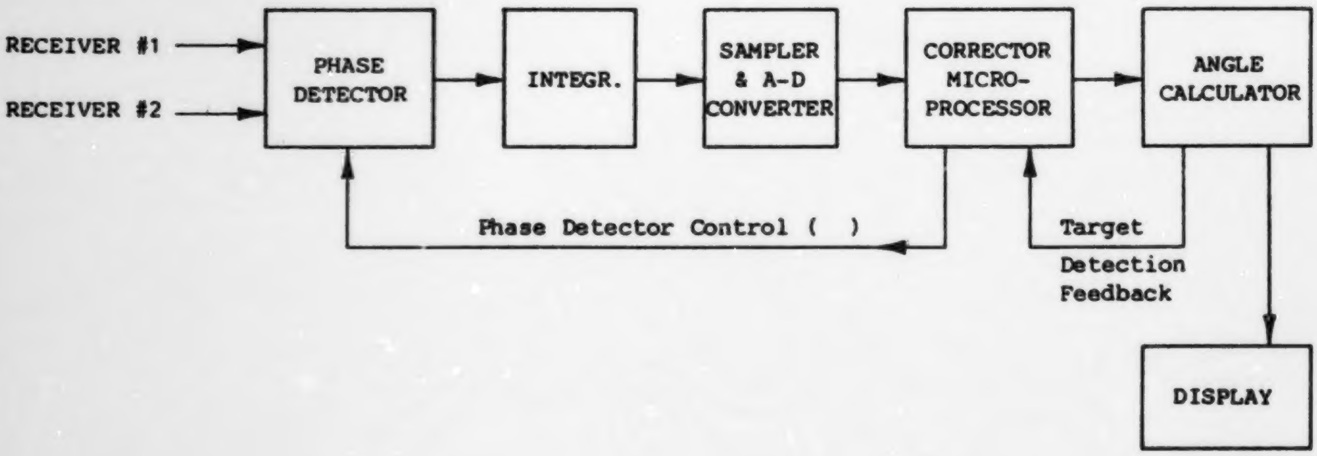

RECEIVER #1
RECEIVER #2
PHASE DETECTOR
INTEGR.
SAMPLER & A-D CONVERTER
CORRECTOR MICRO-PROCESSOR
ANGLE CALCULATOR
Phase Detector Control ( )
Target Detection Feedback
DISPLAY

FIG. 11 : OVERALL SYSTEM DIAGRAM OF D.F. WITH CORRECTOR FEATURE

## REFERENCES

1. The Practical Evolution of Commutated Aerial D.F. System; C.W. Earp, J. Cooper, Proc. IEE, Vol. 105, Part B, Supplement #9, March 1958.

2. Internal Reports of Bayly Engineering on Doppler Direction Finder.

# Volume

# 2

TP4994E

# QUASI-DOPPLER RDF OPERATIONAL
# PROTOTYPE DESIGN

## VOLUME 2 : APPENDIX

Library and Information Centre /
Centre de Documentation (CSLA)
RECEIVED / REÇU LE
MAR 19 1986
Transport Canada / Transports Canada

## TECHNICAL DESCRIPTION
## OF OPERATIONAL PROTOTYPE

DEVELOPED UNDER CONTRACT NO. 09SD.T8200-9-9530
11SD.T8200-2-2541

for

Transport Canada
Transportation Development Centre
1000 Sherbrooke St. West, Suite 2421
Montreal, Quebec, H3A 2R3

by:

Bayly Engineering Limited
167 Hunt Street, Ajax, Ontario

The contents of this report reflect the views of the contractor and not necessarily the official views or policies of the Transportation Development Centre.

## NOTE

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

# REPORT DOCUMENTATION FORM

| | | |
|---|---|---|
| **1. Transport Canada Report No.**<br>TP4994E | **2. TDC Project No.**<br>4822 | **3. Recipient's Catalogue No.**<br>36948 |
| **4. Title and Subtitle**<br>QUASI-DOPPLER RDF OPERATIONAL PROTOTYPE DESIGN<br>(2 VOLUMES) | | **5. Report Date**<br>OCTOBER 1983 |
| | | **6. Performing Organization Report No.**<br>290008 |
| **7. Author(s)**<br>BAYLY ENGINEERING LIMITED | | **8. Transport Canada File No.**<br>D1455-133-5 |
| **9. Performing Organization Name and Address**<br>BAYLY ENGINEERING LIMITED,<br>167 HUNT STREET,<br>AJAX, ONTARIO<br>L1S 1P6 | | **10. DSS File No.**<br>11SD.T8200-2-2541 |
| | | **11. DSS or Transport Canada Contract No.**<br>0SD82-00122 |
| **12. Sponsoring Agency Name and Address**<br>TRANSPORTATION DEVELOPMENT CENTRE,<br>1000 SHERBROOKE STREET WEST, SUITE 2421,<br>MONTREAL, QUEBEC<br>H3A 2R3 | | **13. Type of Report and Period Covered**<br>FINAL REPORT<br>NOVEMBER 1982-APRIL 1983 |
| | | **14. Sponsoring Agency Code**<br>4822 |
| **15. Supplementary Notes**<br>VOLUME 1 : FINAL REPORT<br>VOLUME 2 : APPENDIX - TECHNICAL DESCRIPTION OF OPERATIONAL PROTOTYPE | | **16. TDC Project Officer**<br>MICHA AVNI |

**17. Abstract**

The first part of this report describes work carried out on the original feasibility prototype VHF Radio Direction Finder developed under contract no. 1SD79-00129 with the target of identifying the problem areas and incorporating short-term changes so as to make the equipment operational.

The problem areas, and the subsequent remedial actions are described here, concluding in the final demonstration, and a listing of test results on the improved performance. Recommendations suggest the construction of a second prototype, built in the final engineering version.

The second part of the report is a documentation of the operational prototype "as is", comprising technical descriptions, specifications, circuit diagrams and test procedures. Two brief technical reports are also included, describing new developments incorporated in the improved equipment.

| | |
|---|---|
| **18. Key Words**<br>RADIO DIRECTION FINDER,<br>QUASI-DOPPLER | **19. Distribution Statement**<br>LIMITED NUMBER OF COPIES AVAILABLE FROM TRANSPORTATION DEVELOPMENT CENTRE, TRANSPORT CANADA |

| | | | |
|---|---|---|---|
| **20. Security Classification (of this report)**<br>UNCLASSIFIED | **21. Security Classification (of this page)**<br>UNCLASSIFIED | **22. No. of Pages**<br>410 | **23. Price**<br>NIL |

TDC/CDT 79-005

# FORMULE DE DOCUMENTATION POUR RAPPORT

1. **N° du rapport Transports Canada**
TP4994E

2. **N° de l'étude — CDT**
4822

3. **N° de catalogue du destinataire**
36948

4. **Titre et sous-titre**
QUASI-DOPPLER RDF OPERATIONAL PROTOTYPE DESIGN
(2 VOLUMES)

5. **Date du rapport**
OCTOBRE 1983

6. **N° du rapport de l'organisme exécutant**
290008

7. **Auteur(s)**
BAYLY ENGINEERING LIMITED

8. **N° de dossier Transports Canada**
D1455-33-5

9. **Nom et adresse de l'organisme exécutant**
BAYLY ENGINEERING LIMITED,
167 HUNT STREET,
AJAX, ONTARIO
L1S 1P6

10. **N° de dossier — ASC**
11SD.T8200-2-2541

11. **N° de contrat — ASC ou Transports Canada**
0SD82-00122

12. **Nom et adresse de l'organisme parrain**
CENTRE DE DÉVELOPPEMENT DES TRANSPORTS,
1000 RUE SHERBROOKE OUEST, SUITE 2421,
MONTRÉAL, QUÉBEC
H3A 2R3

13. **Genre de rapport et période visée**
RAPPORT FINAL
NOVEMBRE 1982-AVRIL 1983

14. **Code de l'organisme parrain**
4822

15. **Remarques additionnelles**
VOLUME 1 : FINAL REPORT
VOLUME 2 : APPENDIX - TECHNICAL DESCRIPTION OF OPERATIONAL PROTOTYPE

16. **Agent de projet — CDT**
MICHA AVNI

17. **Résumé**

La première partie de ce rapport décrit les travailles exécuté sur le prototype de faisabilité original de radiogoniométre VHF développé pour le contrat no. 1SD79-00129 avec la butte de identifier les zones des problemes et incorporer les modifications a courte terme pour faire l'appareil fonctionner proprement.

Les zones des problèmes, et les actions de réperation conséquentes, sont décrit ici, terminant avec la démonstration finale et une liste des résultats des essais sur l'operation amélioré. Les recommandations suggére une construction de le deuxieme prototype construit en la version finale de génie.

La deuxieme partie de rapport est la documentation de prototype fonctionant "comme se trouve", contenant le descriptions techniques, les spécifications, les schémas de circuits et les procédures d'essais. Deux rapports techniques bréves sont compris aussi, décrivant les dévelopments nouveux employé dans l'appareil amélioré.

18. **Mots-clés**
RADIOGONIOMÈTRE
QUASI-DOPPLER

19. **Diffusion**
LE CENTRE DE DÉVELOPPEMENT DES TRANSPORTS DISPOSE D'UN NOMBRE LIMITÉ D'EXEMPLAIRES

20. **Classification de sécurité (de ce rapport)**
NON-CLASSIFIÉ

21. **Classification de sécurité (de cette page)**
NON-CLASSIFIÉ

22. **Nombre de pages**
410

23. **Prix**
NIL

CDT/TDC 79-005

# TECHNICAL DESCRIPTION OF OPERATIONAL PROTOTYPE

## TABLE OF CONTENTS

| | | Page |
|---|---|---|
| 1.0 | SYSTEM AND SUB-SYSTEM DESCRIPTION | 1-1 |
| 1.1 | General System Description | 1-1 |
| 1.2 | Advantages of the Design Concept | 1-6 |
| 1.3 | Antenna Array and Dipole Commutation | 1-11 |
| 1.4 | DF Receiver Sub-System | 1-18 |
| 1.5 | Bearing Processor | 1-26 |
| 1.6 | Control and Display Circuits | 1-36 |
| 1.7 | Voice and Data Transmission | 1-48 |
| 1.8 | Omni-directional Monitoring Receivers | 1-53 |
| 1.9 | Power and Interconnections | 1-57 |
| | | |
| 2,0 | UNIT AND MODULE DESCRIPTIONS | 2-1 |
| 2.1 | Antenna Array | 2-2 |
| 2.2 | Antenna Modules | 2-3 |
| 2.3 | Receiver Modules | 2-23 |
| 2.4 | Bearing Processor Modules | 2-89 |
| 2.5 | Power Supply and Interconnections | 2-170 |
| 2.6 | Control and Display Modules | 2-180 |
| 2.7 | Audio and Data Transmission | 2-230 |

# 1.0 SYSTEM AND SUB-SYSTEM DESCRIPTION

## 1.1 General System Description

### 1.1.1 Introduction

The operational prototype DF system is designed on the Quasi-Doppler principle, measuring the phase difference between successive dipole pairs scanned around a symmetrical circular array. The signal samples are amplified by a matched pair of receiver channels and applied to a linear phase detector which produces a stepped phase waveform synchronized to the scan frequency. A digital bearing processor examines the phase waveform and applies Fourier analysis to complete the phase and amplitude of its fundamental component frequency. This phase angle, related to the North reference is a measure of the bearing of the incoming radio signal.

### 1.1.2 System Configuration

Designed for fixed, land-based installation to operate in the Air Traffic Control band of 117.5-136.5 MHz, the system comprises a stationary circular antenna array with a top-of-the-mast mounted antenna unit, a remote receiver unit located in a shelter and a local display/control unit at the console of the Air Traffic Controller. The antenna and the receiver units are connected with a set of 4 RF cables and a multi-core control cable. The receiver is linked to the display/control unit by means of a standard 4-wire telephone line.

The direction finding facility is supplemented by two other features:

1) Facility to demodulate the VF intelligence of the incoming signal (AM detector) and to transmit it to the display/control unit.

2) Emergency call detection, operating on 121.5 MHz to indicate the presence of an emergency call or to override temporarily the normal operation of the system in order to show the bearing of the distress transmitter.

Both the audio and the emergency receivers operate from an omni-directional antenna, independent of the DF array and immune from its interference.

## 1.1.3 General System Specification

### DF System

Frequency Range : 117.5-136.5 MHz (civilian air traffic control) VHF

Principles of Operation : Large aperture Quasi-Doppler with differential sampling of 16 antenna elements

System Accuracy : ≤ ±3° max. bearing error measured in an obstruction-free site at a field strength of 30uV/m

Polarization Error : ≤2° with 45° tilt of transmitter antenna

Sensitivity (vertical polarization) : ≤3uV/m for ±3° of noise flicker

Group Delay Error : Cancelled out by digital processing

DF Receiver Phase Match Error : Cancelled out by bearing processor

Mode Operation : Continuous, unattended

Number of Frequency Channels : Emergency channel plus 10 switch-selected - each channel frequency programmable within the equipment; full range of 720 channels, operator selectable by push-button dialing

Channel Spacing : 25 kHz

Acceptance Bandwidth : Approximately ±50ppm of the carrier frequency

Adjacent Channel Breakthrough : ≤1° error with adjacent channel signal up to 30 dB above wanted signal but not exceeding 3mV/m

Bearing Indication : 4 digits with LED display numerals blanking out at no signal unless connected to store; display at both local and remote units. Analog display circle of LED's in 5° steps at Operator's Panel only.

Response Time : 100 ms to 1.0 sec. depending on the signal strength and the setting of integration constant

Bearing Readout Update : Equal to integration constant

Valid Display Indication : Inaccurate bearings fluctuating by more than ±10° are blanked out

Operator Panel Controls : Power On/Off; dimmer lamp test; channel select (pushbutton and indicator light) ODM/QDM; integration (4 positions); store On/Off with indicator; remote control indicator; system alarm indicator; signal overhead indicator; frequency select mode and reset

Receiver Panel Controls : As above except no store On/Off and indicator; squelch On/Off, synthesizer phase lock indicator

Auxiliary Data Output : At both local and remote units, TTL compatible parallel data bit format

Auxiliary Channel Select : At the remote unit for control from another site

Squelch Threshold : Fully adjustable from front panel of remote

Service Telephone : Jacks provided for 2-way communication between remote and local units (audio channel disabled)

Aircraft Warning Light : Integrated with antenna structure (may be left out if not required)

### Cables

Antenna Head to Remote Receiver : 4 coaxial double-shielded 1/2 inch and 1 multicore; 50 ft. max; RF connectors N-type

Remote to Local : 4-wire telephone line

### Audio Monitoring Facilities

Omni-directional Antenna : Centre of the Array

Frequency : Automatically tuned with the DF System

Type of Detector : AM

Output : 0.5W loudspeakers on both remote and local units

Auxiliary Output : 50 mW at 600 Ohms on the local unit

Squelch : Provided on Remote Unit

AGC : Provided on Remote Unit

Volume Control : Individual with each loudspeaker

### Emergency Receiver Facility

Antenna : Common with audio monitoring provided with separator filter

Tuning : Set at 121.5 MHz

AGC : Pre-set

Detector : Carrier presence above threshold pre-set at the Remote Unit

### Additional Controls

Auto/Man : At both local and remote units

Alarm : LED indicators at local and remote units

### Environmental Conditions

Temperature Range Operational

Antenna : -55°C to +55°C

Local and Remote Unit : -20°C to +55°C

Humidity : 95% max.

Wind Load (Antenna) : 160 Km/hr max.

Salt Spray (Antenna) : Equivalent to MIL specifications

Drip-proofing (Antenna) : Equivalent to MIL specifications

Ice Formation (Antenna) : Up to 2 inch thickness

### 1.1.4 Functional Sub-systems

For the purpose of a detailed description the system is considered as a series of functional sub-systems, each performing a different function which can be technically defined in terms of cause and effect or inputs and outputs. In this concept, a functional sub-system is not necessarily confined inside a single piece of equipment but may be divided into several sections housed in different units.

Seven such functional sub-systems can be clearly separated in the Quasi-Doppler Radio Direction Finder System:

i Antenna Array with Dipole Commutation

ii DF Receiver

iii Bearing Processor

iv Control and Display Circuits

v Audio and Data Transmission

vi Omni-directional Monitoring Receivers

vii Power and Interface

## 1.2 Advantages of the Design Concept

1.2.1 Doppler DF Systems have been used successfully for over 40 years, over several generations of design approaches and stages of technology. What distinguishes the present System can be summarized in the following points:

i Ultra-stable antenna structure of "bicycle wheel" concept

ii "Soft-switching" technique of dipole commutation

iii Two-channel sampling of the array dipoles

iv Linear Phase Detector with over-swing capacity

v Processing the bearing by Fourier analysis

vi Channel and frequency selection by frequency synthesizer

vii Compensation for site errors

viii Separate audio and emergency receivers

ix Audio and data transmission over standard telephone lines

### 1.2.2 Antenna Structure

The antenna array, consisting of 16 DF dipoles and an omni-directional centre element is supported by a mechanical structure resembling a bicycle wheel with a rigid, insulated rim and a network of criss-crossed steel cables, or "spokes" which form a conducting ground plane. Vertical support is provided by a set of insulated radial struts which restrict any flexing of the array plane. This type of structure has an inherent rigidity and mechanical stability under all conceivable wind and ice loading conditions. For given precision of relative dipole positions this design was proven lighter and easier to construct than other ways of constructioon.

Ref: See paragraph 5.5 of the Final Development Report

### 1.2.3 Soft-switching Technique

The 16 antenna dipoles are selected in pairs by means of pin-diode switches operated by control pulses of the scan-logic system. Such commutation normally produces an infinite series of mixing products which appear as side-bands of the received carrier. In this design the higher order mixing products are reduced by using "soft" control pulses of special waveform which make the switch attenuate in the critical change-over period. As a result, it is possible to receive a bearing from a weak signal with an interfering signal 30 dB higher in the adjacent channel, i.e. 25 kHz away.

Ref: See paragraph 5.3 of the Final Development Report

### 1.2.4 Two-channel Sampling

By sampling two instead of one dipole, the restrictions are removed on the aperture of the array - there being no ambiguity of bearing as the diameter becomes larger than the wavelength. The same system design may be used with different sizes of arrays, say with 16 elements and 32 elements.

Speed of commutation is not critical. There is no need to ensure a frequency deviation large enough in comparison with the stability of the carrier. The only criterion is that of the bearing response time. A rotation frequency of about 100 Hz provides a bearing reading averaged over 8 cycles in 0.1 second. A low commutating frequency has the advantage of less interference with the audio reception. Furthermore, the splash-over of intermodulation products into the adjacent frequency channels is also reduced.

The two i.f. channel voltages are similar in amplitude and contain equal percentages of AM or FM and an equal share of atmospheric noise and of the noise of the local oscillators. By measuring their relative phase any modulation or noise effect is reduced to negligible proportions. The phase comparator operates throughout each period of dipole pair sampling so that there is minimum waste of real time in receiving the signal. It is the cyclical waveform of the phase output which contains the azimuth information.

### 1.2.5 Linear Phase Detector

A large antenna aperture, needed to provide immunity from field site errors makes it necessary to measure a range of phase differences of up to ±180°. This makes it impractical to use a conventional phase detector with sinusoidal characteristic. For this reason a linear phase detector was adopted, converting the phase difference between the two receiver channel outputs to pulse width modulation, followed by an intergrating network. Phase angles exceeding ±180° can still be detected by instantly reversing one of the channel inputs by 180° and then correcting the reading in the software section by adding or subtracting the 180° constant.

### 1.2.6 Fourier Analysis

The cyclical waveform of the phase output contains a number of components which have to be separated and identified:

i A zero offset due to group delay and the phase unbalance of the twin-channel DF receiver and phase detector sub-system.

ii The fundamental scan frequency, the phase of which relative to "North" is a measure of the DF bearing

iii Harmonics of the scan frequency due to combined reflections of other dipoles, the support structure and miscellaneous field site effects.

iv Phase jitter noise due to interference of either atmospherics or system noise or the effect of presence of other signals of different frequency.

Processing the bearing by Fourier analysis secures the information of item ii) (phase of the scan frequency) and rejecting the others. The computed bearing is obtained much faster than would be possible by using an analog filter tuned to the scan frequency. Furthermore, the group delay of such a filter is no longer a source of possible error.

### 1.2.7 Frequency Synthesizer

In the older generations of Doppler DF Systems it was coventional to select a limited number of frequency channels by switching crystal oscillators. The modern approach is to use a frequency synthesizer, phase locked to a master crystal oscillator and tuned in steps by means of digital programming. In this prototype there is provision for 11 preset channel frequencies and also for direct dialing of any frequency channel within the ATC band. Ten of the pre-selected channels can be manually set to the desired frequency by means of DIP switches inside the equipment. The 11th channel is permanently set to the emergency frequency of 121.5 MHz.

Ref: See paragraph 7.3 of the Final Development Report.

### 1.2.8 Compensation for Site Errors

The large antenna aperture (1.5 wavelength) used in this system ensures that the effects of field site reflections are relatively small as can be demonstrated by moving a car or metal object in the vicinity of the DF tower. However, a further step was taken to reduce the field site errors by introducing appropriate bearing corrections in the software of the bearing processor sub-system. The procedure is to calibrate the bearing errors for a full circle of azimuth of a target transmitter and to enter a correction chart into the microprocessor software. This correction is accurate to the extent of the stability of the field site error, i.e. it still remains subject to minor fluctuations due to weather changes and the position of mobile objects and their frequency of resonance.

### 1.2.9 Separate Audio and Emergency Channel

A separate omni-directional antenna, located at the electrical centre of the array is connected to a separate receiver channel turned to the same frequency as the two Doppler channels. The i.f. portion is provided with AGC and connects to an AM demodulator. Re-radiation of the commutation pulses from the DF dipoles is reduced by keeping this antenna separate and somewhat elevated with respect to the plane of the array. The audio output of this receiver can be monitored in the remote unit and is further available for transmission to the local unit.

Since the FM cancellation for DF no longer depends on the signal from the centre antenna, the entire audio channel can be left out if this facility is not required.

Emergency call signals at 121.5 MHz are monitored by the centre antenna and processed via a separate emergency receiver with fixed tuning, terminating in a detector, the output of which responds to the emergency condition.

Two modes of Emergency Channel are provided:

#### Mode 1 - Fully Automatic

In the auto position, the detection of an emergency signal automatically allows the Direction Finder to determine a bearing and to transmit bearing data to the local site. In addition, an emergency status signal is transmitted to the local site where it illuminates an emergency indicator and sounds an audible alarm at both local and remote sites. A long release time constant ensures that the alarm remains locked even on pulsed signals. This override function will revert to normal at the end of the emergency call.

#### Mode 2 - Manual

In this mode, the MAN-AUTO switch is placed in the MAN position. Upon detection of an emergency signal, an emergency status signal is transmitted to the local site to illuminate the emergency indicator and sound the audible alarm. The operator may then, at his discretion, operate a switch to select the emergency channel frequency.

### 1.2.10 Interconnections and Audio and Data Transmission

The Antenna Head is connected to the Remote Unit by means of a multi-core control cable and four double-shielded coaxial cables. The length of this connection is of the order of about 50 ft. for a standard installation at the airport.

A complete set of data-above-voice modems is built into the system to provide a facility for remote control from one or more locations.

The Remote-Local link consists of a standard telephone wire quad, in the form of a buried cable. C1 grade characteristics are advisable to avoid losses at the data transmission frequencies. Up to 10 Km distance is envisaged which can be extended by the addition of standard telephone repeaters. An alternative Local-Remote link for short distances up to 100 m would consist of a multi-core control cable with the omission of the "data-above-voice" modems.

## 1.3 Antenna Array and Dipole Commutation

### 1.3.1 Introduction

The Doppler antenna consists of a number of vertical dipoles tuned to the top of the frequency band and spaced equally in a circle. All the dipoles are connected with equal length cables to the commutator located in the centre hub. Two adjacent dipoles are sampled similtaneously, the pair being switched round the circle at a rate set by the commutation generator. The voltages induced in the sampled pair remain almost constant but their relative phase undergoes cyclical variation as the switching progresses through 360 degrees. This phase can be measured continuously after the signals are processed through two identical receiver channels, each consisting of RF amplifiers, frequency converters and i.f. stages.

The Phase Comparator operates at the final intermediate frequency and produces an output of a stepped waveform superimposed over a sine function, each step corresponding to a different pair of dipoles. It is the positive-slope zero crossing of this waveform which determines the angular position of the target.

The DF antenna sub-system is shown on the block diagram of Fig. 1.3. It can be subdivided into three sections:

- the dipole array
- commutation network
- scan logic control

The commutation network, the scan logic and the front-end of the receiver sub-system are contained in a waterproof enclosure (Antenna Unit) mounted close to the mast, underneath the ground plane of the array.

### 1.3.2 The Dipole Array

The prototype developed for the ATC has 16 dipoles with a wide tuning range of 115 MHz-140 MHz. They are spaced at approximately 120° maximum phase difference (1/3 of the wavelength) at the highest signal frequency. The dipoles are mounted at the extreme points of a star-shaped artificial ground plane made up of a mesh of stainless steel tension cables. The ground plane is continued on the outside of the array with a set of 16 horizontal counterpoise rods, balancing the polar pattern of horizontally polarised waves around each dipole. Dipoles are connected to the switching network with a set of 75 ohm coaxial cables matched to the same electrical length with an accuracy of a fraction of a degree at the highest frequency in the RF band.

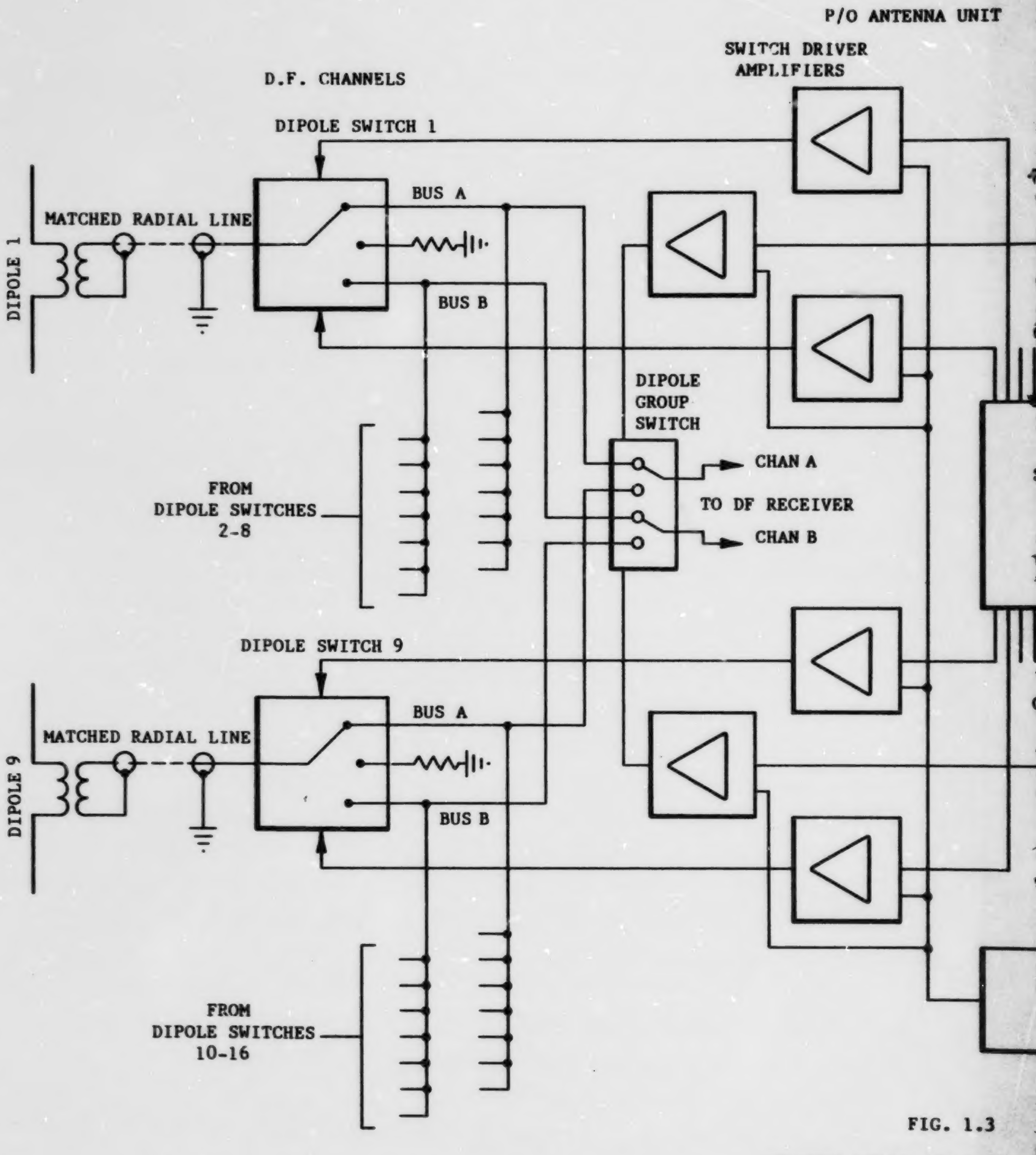

P/O ANTENNA UNIT
SWITCH DRIVER AMPLIFIERS
D.F. CHANNELS
DIPOLE SWITCH 1
BUS A
MATCHED RADIAL LINE
DIPOLE 1
BUS B
DIPOLE GROUP SWITCH
CHAN A
TO DF RECEIVER
CHAN B
FROM DIPOLE SWITCHES 2-8
DIPOLE SWITCH 9
BUS A
MATCHED RADIAL LINE
DIPOLE 9
BUS B
FROM DIPOLE SWITCHES 10-16

FIG. 1.3

ANTENNA ARRAY AND DIPOLE

SUB-SYSTEM BLOCK DI

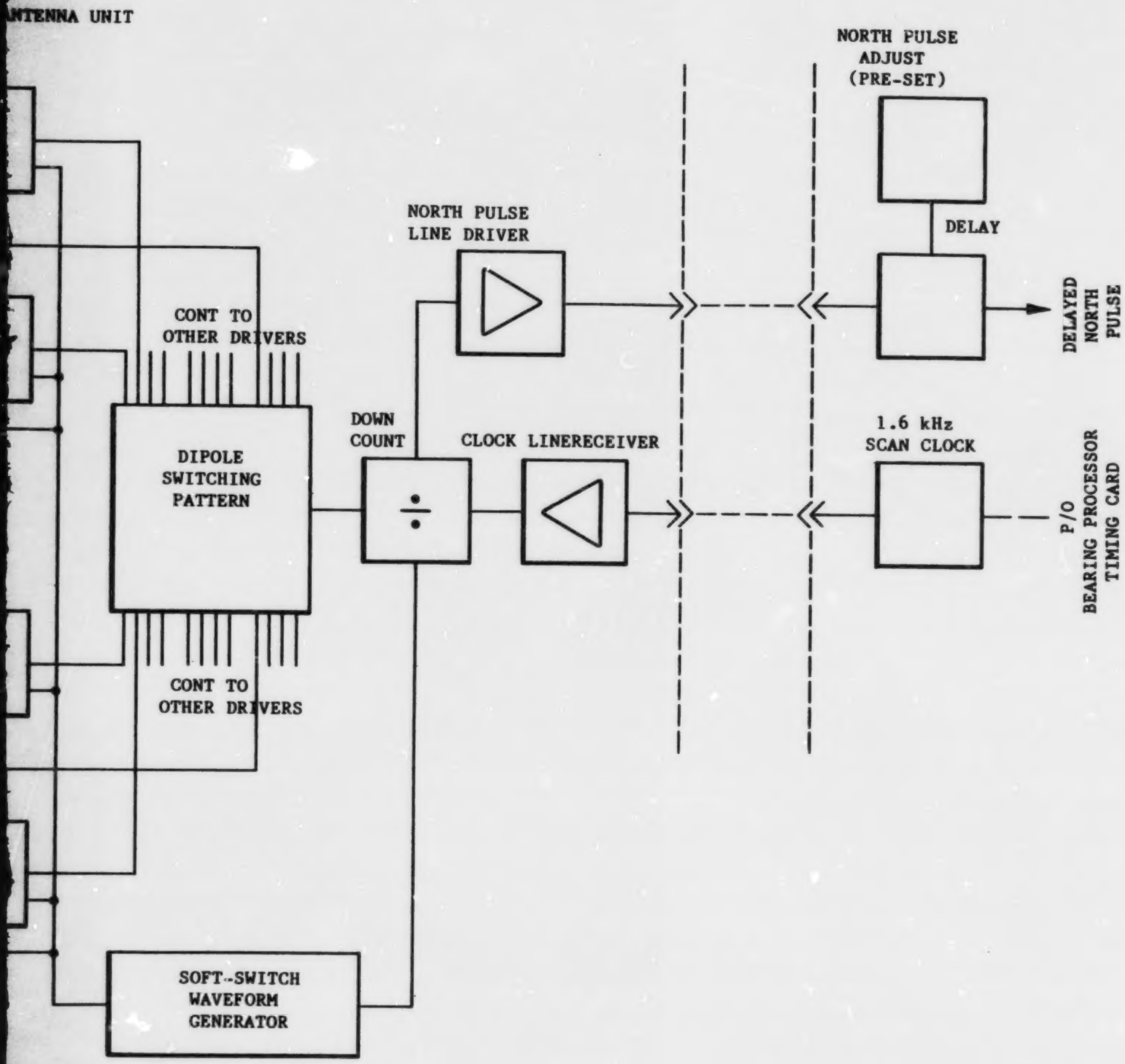

NTENNA UNIT
NORTH PULSE ADJUST (PRE-SET)
DELAY
NORTH PULSE LINE DRIVER
DELAYED NORTH PULSE
CONT TO OTHER DRIVERS
DIPOLE SWITCHING PATTERN
DOWN COUNT
CLOCK LINERECEIVER
1.6 kHz SCAN CLOCK
P/O BEARING PROCESSOR TIMING CARD
CONT TO OTHER DRIVERS
SOFT-SWITCH WAVEFORM GENERATOR

FIG. 1.3

AY AND DIPOLE COMMUTATION

STEM BLOCK DIAGRAM

The dipole design incorporates a unique lightning protection feature - a short-circuiting centre rod of a length corresponding to 1/2 wavelength for the band of frequencies in use. This rod is firmly bonded at the centre to the ground plane of the array. Additional corona protection is provided by placing cream lamps across each dipole element.

The mechanical structure supporting the dipoles relies on a non-metallic ring, suspended from the mast by virtue of a number of non-metallic rods above and below the centre line of the ring. An array of metallic cables in the centre line of the ring places the ring in tension and at the same time provides the necessary ground plane for the antenna. Precision springs on one end of all the rods and cables ensure correct pre-tensioning of all the structural members during installation without the need for any complex tension-measuring devices. They also ensure stability of the structure under temperature and ice-loading stresses making it possible to maintain the relative symmetry of the dipole array to better than 0.02° of the bearing angle.

### 1.3.3 Commutation Network

Sequential switching of the dipole pairs onto a pair of DF receiver channels requires that each dipole be provided with a coaxial 3-way switch so that it can be linked to either channel A or channel B of the receiver or to a dummy load when not actively engaged. The pair sampling proceeds at a rate approximately 660 ms per step giving an array scan frequency of approximately 100 Hz.

The outcome of this sequential sampling produces, from each dipole, an RF signal which is interrupted at the rate of the scanning frequency, i.e. a pulse modulated signal. This signal, therefore, is made up of the fundamental RF frequency in addition to the upper and lower sidebands of all the components of the switching frequency. These additional products can extend over a bandwidth covering several hundred kHz creating interference on a large number of adjacent channels and resulting in severe degradation in D.F. performance. This is avoided in the prototype, where the switching action is accomplished with a special waveform of low zero-slope. In such a 'Soft Switch', fewer of the higher order products are generated thus reducing interference of adjacent channel transmissions.

The 3-way 'soft switch' is made up of PIN diodes which can be considered as variable RF resistors whose resistance is inversely proportional to the forward current. By employing these diodes in a (T) configuration, it was possible to contstruct an RF switch having an attenuation which is directly controlled by the shape of the driver waveform. In this circuit the largest change in attenuation occurs during the first few milliamperes of current through the diodes. This implies that the first volt of bias will have the greatest impact on the performance of the switch.

Therefore, it follows that in order to reduce the generation of unwanted IM products, the slope of the input drive voltage must be kept as low as possible. To obtain this effect a special waveform was generated by driving a triangular signal through a network consisting of diodes and resistors. The slope at the diode's knee is used to provide soft switching for both the on and off conditions, with minimum slope occurring at the transition region. The shape of the centre portion of the driving pulse is simply squared off to give the "full on" condition.

The 16 dipole selectors are arranged in two sets of 8 in order to reduce the shunt loading of the unused sections. Each set of 8 handles a semi-circle of the antenna array and in turn the appropriate semi-circle is chosen by a four-sector switch connected in cascade, making up the total number of switch boards to 20. The switches are driven by push-pull driver circuits, mounted 4 to a card, thus making a total of 5 driver cards. The drivers take their inputs from the scan logic control which determines the sequence of operation of the dipoles.

### 1.3.4 Scan Logic Control

Antenna array scanning is controlled by a frequency derived from a clock which is part of the bearing processor. The clock frequency is counted down and shaped into a triangular wave which is then modified into the special "soft switching" waveform used to drive the dipole switches. The switch selection is dictated by reference to a PROM contained on the scan logic card.

Every time the scan makes a full circle, a reference pulse is generated, called the "North Pulse" which is sent down to the bearing processor as reference for the computation of bearing. The North Pulse generated on the scan logic control board is positioned half-way through the engagement period of dipoles 1 and 16. When arriving at the bearing processor it undergoes two modifications:

i It is delayed by a time equal to the group delay of the DF receiver.

ii It's timing is further corrected by a manual DIP switch which allows a minor adjustment to be made of the true North position relative to the mechanical "North" of the antenna array.

### 1.3.5 Sub-System Specification, Antenna Array and Commutation

#### Antenna Array

Frequency Range : 117.5-136.5 MHz

Number of Dipoles : 16 with N-type connectors

Diameter of The Array : 1.7 wavelengths at max. frequency

Dipole Impedance : 75 Ohms single-ended at mid-range, VSWR $\leq 2$ over the entire band

Dipole Protection : Internal short-bar, $\lambda/2$ resonant at mid-range additional corona protection with neon tubes

Dipole Antenna Factor : 6 dB approximately

Dipole Feed Cable : 75 ohm coaxial high-phase stability type, cut to $2\lambda$ length at mid-range (all feed cables to be matched in phase to within 0.2°) and connected to the switches with TNC connectors

Dipole Mounting Accuracy : 0.02° w.r.t. mast axis

Dipole Replacement : Individually removable from the outside of the support ring

Ground Plane : 16-point star of stainless steel cables bonded at points of crossing

Ground Counterpoise (each dipole) : Radial, horizontal rod of 3/8 approximately

Coarse "North" Setting : By rotating mounting plate during installation (adj. steps of 11.75°)

## Commutation Network

Dipole Selection : One pair of adjacent dipoles, scanned periodically in 16 steps in clockwise direction viewed from the top

Termination of Unused Dipoles : 75 Ohms, selected on the switch assembly

Dipole Switch Network : 2 sets of 8 3-way switches, in turn selected by a set of 4

Scan Frequency : 100 Hz approximately

Switch Action : 'Soft Switching' with special waveform to reduce intermodulation on adjacent channels

| | |
|---|---|
| Commutation Network Output | : Two matched 75 ohm cables with TNC connectors |

### Scan Logic Control

| | |
|---|---|
| Scan Clock | : 1.6 kHz supplied from the bearing processor |
| "Soft-Switch" Waveform | : Generated from the scan clock with a dual slope reduction circuit |
| Switching Programme | : 40 outputs (TTL level) to control the push-pull drivers of the dipole switches. Self-contained PROM |
| North Reference | : "North" pulse generated from the scan clock in the mid-position of the switching time of the dipole pair 1-16. Output to bearing processor |
| Delayed North Pulse | : Obtained in the bearing processor (timing card) to compensate for the group delay of the DF receiver and phase detector (approx. 200us) |
| True "North" Adjustment | : By pre-setting a binary DIP switch on the bearing processor timing card. Correction by software, min. ±10° |

## 1.3.6 Sub-system Test Procedure

| | |
|---|---|
| Dipole Impedance | Measure impedance of each dipole using a network analyzer with Smith-chart display over the full frequency range of 117.5-136.5 MHz. Ensure that the set of 16 dipoles is matched to within ±2%. |
| Dipole Phase Match | Apply a signal generator at 127.0 MHz to the omni-directional antenna situated above the array. Set level to +8 dBm. Measure phase difference between the output lines of the switching network using a vector voltmeter with a scope connected to its 20 kHz output. Put the |

bearing processor in operation so that the dipole pairs are scanned as in the normal DF procedure. Trigger the scope from the North pulse output (TP). Observe the output waveform of the phase difference on the scope over an entire scan cycle. The phase amplitude of all the dipole pairs should be equal and close to zero. Adjust the input trimmers on the dipole switch cards as necessary to even them out to better than ±1°. (A faulty dipole or switch will show as a distortion of the output: one pulse up and one down.)

**North Pulse and Dipole Sequence**

Connect the 2nd channel of the scope to the North pulse output. The pulse should appear at the start of the scan. Verify that dipole 1 is the first one on the scan time axis. This can be identified by bringing a 1/2 wavelength metal bar close to the dipole. Verify that all the other dipoles are connected in the correct sequence.

## 1.4 DF Receiver Sub-system

### 1.4.1 DF Receiver Concept

The two signals obtained from scanning the dipole pairs in the antenna array are amplified by two identical receivers and applied to a phase detector. This is conventionally called a "two-channel" receiver where the meaning of "channels" are the signal paths rather than tuning frequency allocations.

To be able to perform the phase measurement accurately, it is essential to design the receiver so that its corresponding channel sections are matched exactly to one another both in gain and in phase over a wide range of signal conditions and environmental factors. The underlying principle is to make the two channels with identical circuits, layouts and component values and to align them to match section by section.

The DF receiver for the Quasi-Doppler system has to satisfy the requirements of the low noise factor, adjacent channel selectivity and constant output over a wide dynamic range. These conditions are commonly expected from a conventional FM receiver. However, the twin-channel, i.e. receiver sub-system, also requires the phase and gains matching facilities and a group delay which is constant over the pass-band and as short as possible, while satisfying the bandwidth requirements. For common tuning, the two channels of the receiver must be fed from common local oscillators via phase-matched paths and through buffer stages with sufficient forward to back gain ratio to minimize interchannel crosstalk.

### 1.4.2 Frequency Plan and Filter Characteristics

The most critical part of the two-channel receiver are the band-pass filters used to select the wanted frequency channel and to reject any image or interference products. The phase-matching requirement limits the design of any individual filter to a maximum of 7 tuned circuits, five being preferable, for ease of alignment. To be able to utilize such filters, the DF receiver has three stages of frequency conversions. The last intermediate frequency of 200 kHz has been determined by the realisation of a seven-circuit filter to accomodate the 15 kHz bandwidth required by stability of transmitters with the 25 kHz channel spacing. This filter is of Legendre's type, with a linear phase response in the centre ±3 kHz of the band, combined with very steep edge of the band cut-off.

The first i.f. of 30 MHz was taken as approximately 1.5 times the width of the VHF input band so that tuning can be accomplished with a single sweep of the local oscillator without range switching of the VHF input filters. The input filters are divided into two sections:

1) A low-toss two-stage pre-tuning filter to pass the ATC VHF band to reduce the adjacent FM and amateur bands as well as to cut off the interference from secondary radar.

2) A full r.f. five-stage band-pass filter following the RF Amplifier with sufficient selectivity to suppress the local oscillator and image frequencies.

The second conversion produces 2.2 MHz, which is close to the geometrical mean of the first and the third i.f. The filter bandwidths of the 30 MHz and 2.2 MHz i.f. filters were made just wide enough to suppress the respective first and second i.f. image frequencies with a minimum number of tuned circuits in each.

**TABLE 1.4 - FREQUENCY PLAN OF DF RECEIVER**

| Input Band | $LO_1$ (freq. synt.) | $IF_1$ | $LO_2$ (crystal osc.) | $IF_2$ | $LO_3$ (crystal osc.) | $IF_3$ |
|---|---|---|---|---|---|---|
| 117.5-136.5 MHz | 147.166.5 MHz | 30 MHz ±400 kHz | 32.2 MHz | 2.2 MHz ±50 kHz | 2.4 MHz | 200 kHz ±7.5 kHz |
| Primary Image | | First i.f. Image | | Second i.f. Image | | |
| 177.5-196.5 | | 34.4 MHz | | 2.6 MHz | | |

The above frequency plan is relatively free of spurious responses in the input band, with two exceptions: the fourth harmonics of the first i.f. (4 x 30 = 120 MHz) and of the second local oscillator (4 x 32.2 = 128.8 MHz). Of these two, only the second (128.8 MHz) shows a significant pick-up at the input.

### 1.4.3 Front-End Separation

The antenna switching network is a fair distance from the receiver (50 ft or more) and a loss on the coaxial cables would cause a reduction of sensitivity. Furthermore, feeding very weak signals down the mast might lead to pick-up of interference from the power and control lines and from the mast current induced by atmospherics. This problem is avoided in the prototype by separating the front end of the receiver and placing it in the Antenna Unit which is mounted up on the mast. The front end contains r.f. amplifiers and the first frequency conversion so that the signals fed down the cables are at the first i.f. of 30 MHz and at a level of up to 36 dB higher than the commutation output. This arrangement has the following advantages.

i) The feeder cables carry a lower frequency, hence their loss is reduced.

ii) Owing to the gain of the front-end section, the cable loss has no effect on the noise figure of the receiver.

iii) The feeder cables can be more easily matched in phase.

iv) Interference pick-up is reduced first by 36 dB by the front-end gain of the receiver and then by another 14 dB due to reduction of bandwidth.

The first local oscillator (frequency synthesizer), which is used for this conversion, is located in the Receiver Unit so that it is more easily accessible for maintenance and is not exposed to the extremes of temperature. Its output is conducted up the mast to the Antenna Unit at a relatively low level (-4 dBm) where it is amplified, split-up and distributed by the $LO_1$ distribution module.

### 1.4.4 DF Receiver Functional Block Diagram

The functional block diagram of the DF receiver is shown in Fig. 1.4, where it is combined with a chart of minimum and maximum levels at the interface points. The levels correspond to the following three conditions of signal input:

i) Minimum input signal obtained with the highest DF sensitivity quoted, equivalent to a field strength of 30 uV/m.

ii) Intermediate level, just before the RF agc is brought into operation, equivalent to a field strength of 100 uV/m.

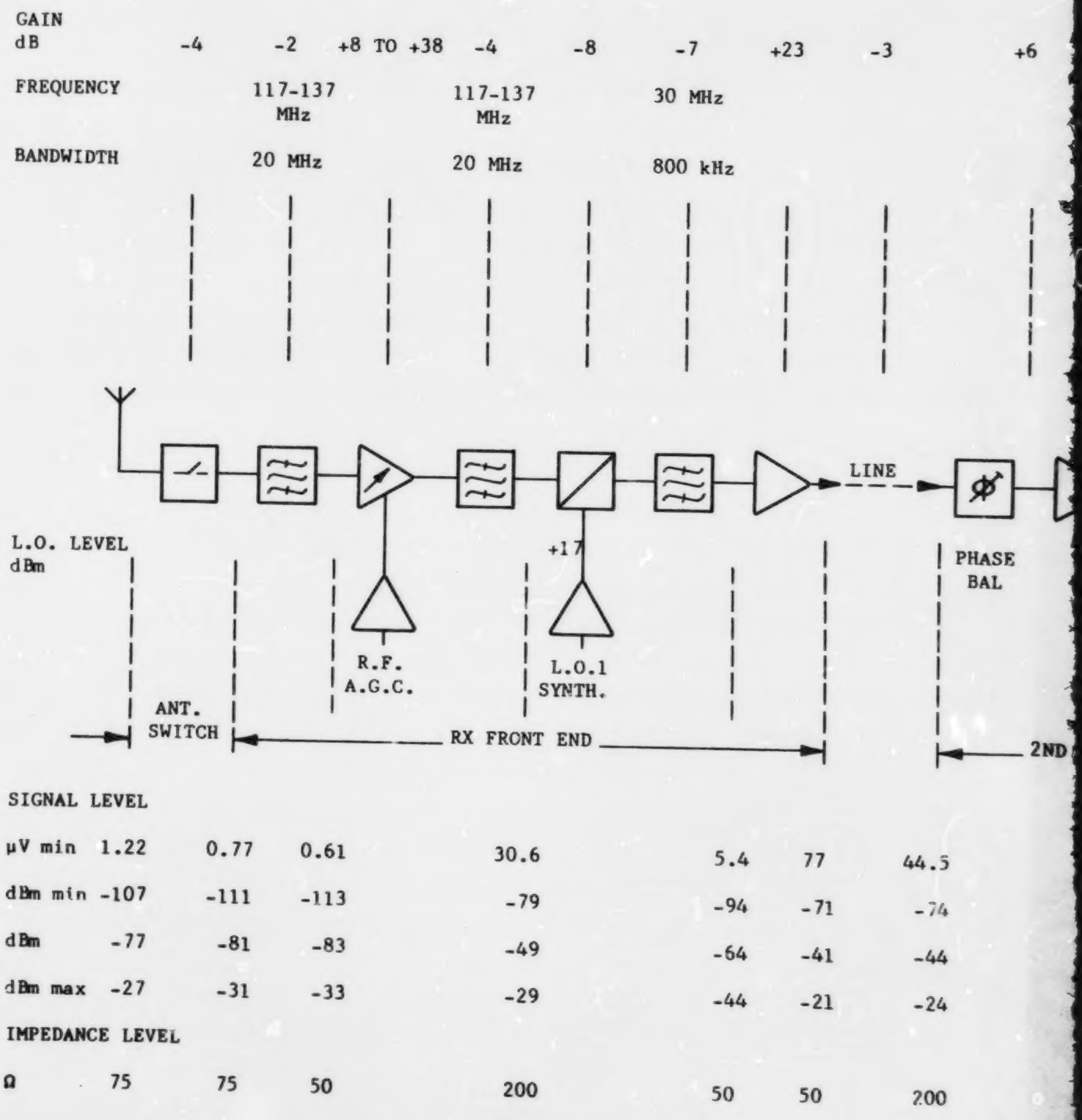
iii) Maximum allowable input with full action of the RF and IF agc, equivalent to a field strength of 30 mV/m.

### 1.4.5 DF Receiver AGC Network

Constant output of the two receiver channels is a necessary condition to make the phase detector perform accurately. For this purpose, the prototype is provided with two AGC networks - one in the r.f. section and one in the final i.f. stages. Thresholds of operation of the two networks are different. The i.f. AGC starts to function directly from the maximum sensitivity level and continues to control the receiver output down until the input level reaches 30 dB above the minimum. At this point, the r.f. AGC switches in, first with an attenuator pad of 10 dB, then with 20 dB and finally 30 dB. The next 20 dB increase, up to the maximum input of -27 dBm is taken up again by the if AGC loop.

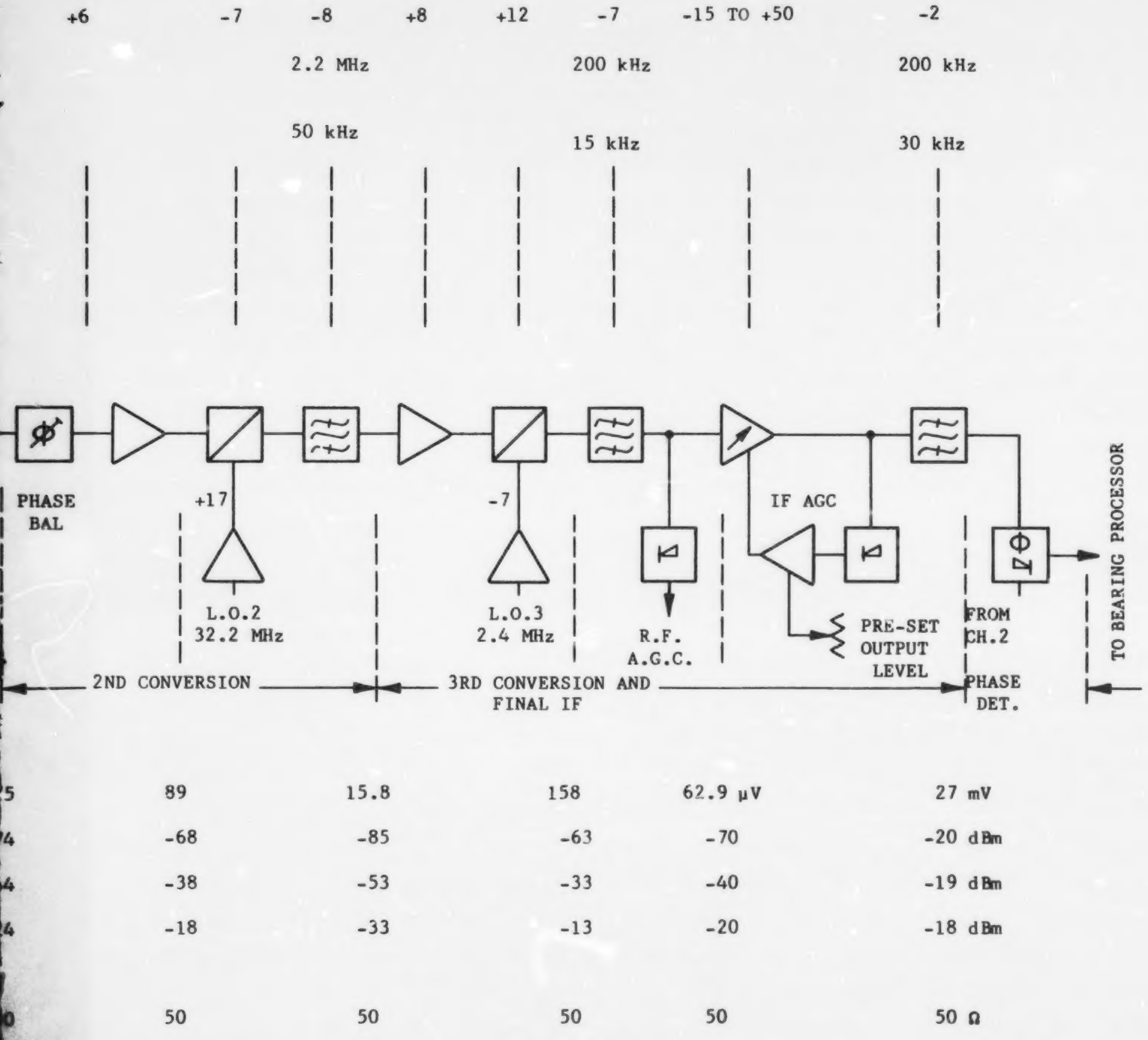
FIG 1.4 DOPPLER DF TWO

FUNCTIONAL BLOC


GAIN
dB
-4
-2
+8 TO +38
-4
-8
-7
+23
-3
+6
FREQUENCY
117-137 MHz
117-137 MHz
30 MHz
BANDWIDTH
20 MHz
20 MHz
800 kHz
LINE
L.O. LEVEL
dBm
+17
R.F. A.G.C.
L.O.1 SYNTH.
PHASE BAL
ANT. SWITCH
RX FRONT END
2ND
SIGNAL LEVEL
μV min 1.22 0.77 0.61 30.6 5.4 77 44.5
dBm min -107 -111 -113 -79 -94 -71 -74
dBm -77 -81 -83 -49 -64 -41 -44
dBm max -27 -31 -33 -29 -44 -21 -24
IMPEDANCE LEVEL
Ω 75 75 50 200 50 50 200

LER DF TWO CHANNEL RECEIVER

TIONAL BLOCK DIAGRAM


+6
-7
-8
+8
+12
-7
-15 TO +50
-2
2.2 MHz
200 kHz
200 kHz
50 kHz
15 kHz
30 kHz
PHASE BAL
+17
L.O.2
32.2 MHz
-7
L.O.3
2.4 MHz
R.F.
A.G.C.
IF AGC
PRE-SET
OUTPUT
LEVEL
FROM
CH.2
PHASE
DET.
TO BEARING PROCESSOR
2ND CONVERSION
3RD CONVERSION AND
FINAL IF
5
89
15.8
158
62.9 μV
27 mV
4
-68
-85
-63
-70
-20 dBm
4
-38
-53
-33
-40
-19 dBm
4
-18
-33
-13
-20
-18 dBm
0
50
50
50
50
50 Ω

The i.f. agc operates at 200 kHz with an amplifier of continuously variable gain and a detector fed from it's output, forming a self-contained loop in each of the two receiver channels. It's dynamic range is over 65 dB, leaving some margin for adjustment at the extreme ends of the range. Two adjustments are provided: the operating threshold and the loop gain.

The r.f. agc detects the signal level after the 3rd conversion in channel 1 of the receiver but before the i.f. agc loop. This signal is amplified and processed through a logic network to provide digital data for switching PIN-diode attenuator pads in the r.f. stages. Identical attenuators are switched similtaneously in both the receiver channels. The main objective of the r.f. agc is to keep down signal levels at the mixer inputs so as to avoid IM interference. There are two threshold adjustments of the trigger action for the 10 dB and the 20 dB pads respectively.

Both the i.f. and the r.f. agc loops are activated by signals inside the fundamental 15 kHz tuning band of the selected frequency channel, hence they do not respond to adjacent channel interference.

### 1.4.6 Local Oscillators

All the local oscillators used for frequency conversion are common to the two channels of the DF receiver and their feed points to the respective mixers, are isolated with buffer stages to prevent crosstalk. In the prototype DF receiver, there are three conversion stages and therefore, three local oscillators are needed.

The first local oscillator ($LO_1$) is a frequency synthesizer with the VCO operating at a frequency 30 MHz higher than the r.f. input. Its output is divided down to 25 kHz which is fed back in the phase-lock loop. The tuning is accomplished by digitally controlling the number of the count-down, giving a total of 720 steps, one every 25 kHz. The frequency synthesizer is contained in one module forming part of the receiver but the control network, including DIP switches for the pre-set channels, forms part of the Control/display sub-system. The $LO_1$ tunes both the DF channels and the audio channel of the DF system. It also provides a component part of the test frequency used in the Test Injection function. Output of the $LO_1$ goes directly to the audio channel in the Receiver Unit and also supplies a coax. line up the mast where it is further divided to feed the two DF channels and the test injection network. DF channel phase balance is provided in the Oscillator Distribution module in the Antenna Unit and individual buffers are located in the Front-end modules of the DF receiver channels.

The second local oscillator ($LO_2$) operates at 32.2 MHz and is crystal-controlled, fitted with a varactor and an optional control line for AFC. $LO_2$ for the DF receiver is mounted inside one of the 2nd conversion modules. The emergency channel has a separate source of $LO_2$ - also a crystal controlled oscillator (temporarily mounted in the rear of the receiver). This is intentionally separated from the DF channels since there must be no AFC action on the emergency monitoring when the DF is used for a different frequency channel.

The third local oscillator ($LO_3$) serves a dual purpose: it povides oscillator frequency for the third conversion stages of the two DF receiver channels and it serves also as the main reference frequency for the synthesizer phase-lock. It is located physically in the Frequency Synthesizer module.

### 1.4.7 Phase Detector

Constant amplitude outputs (approx. -20 dBm at 200 kHz) are applied from the two channels of the DF receiver to the input of a linear phase detector. The phase detector performs three consecutive functions: limiting and squaring, pulse-width modulation and integration combined with filtering out of the fundamental carrier wave. The detector has a linear range of 0°-360° which is normally shifted by an inverter to ±180°.

Output of the phase detector, with signal present, is a picture of the scan waveform broken into 16 steps corresponding to the positions of the switching of the 16 dipole pairs. This waveform is applied to the bearing processor which is made to neglect the switching transients and to sample the amplitudes of the flat portions of the steps which provide a measure of the consectutive phase differences between the dipole pairs.

Phase inversion of one of the channels is controlled externally by a logic pulse from the bearing processor. This allows to extend the linear range of the phase detector in places where it is known that the phase difference approaches or exceeds the +180° limit. The practical extended limit of linear operation is ±230° as explained later in the description of the Bearing Processor Sub-system.

The positive-slope zero crossing of the scan waveform shows the approximate bearing of the target taken with reference to the "delayed North Pulse" test output. The amplitude of the waveform is nearly constant for horizontally propagated waves but it decreases if the target is elevated. The ratio of decrease is used to trigger the "signal overhead" indication (60° evelation corresponds to a 50% level of the amplitude).

The only maintenance adjustment of the phase detector is the zero off-set of the output Op-amp which should be set to give zero volts dc with the two input lines shorted.

### 1.4.8 DF Receiver Specification

**Principle of Operation** : Two-channel receiver for measurement of phase difference

**Frequency Range** : 117.5 MHz - 136.5 MHz

**Tuning** : Digital control by frequency synthesizer in steps of 25 kHz (10 lines, TTL level)

**Tuning Stability** : ±5 ppm. over temperature range 0°C to +35°C

**Input Impedance** : 75 ohms, TNC terminals

**RF Noise Figure** : ≤7 dB each channel

**Dynamic Range** : 107 ddBm to -27 dBm

**RF AGC** : 30 dB max. in 10 dB steps, -77 dBm threshold ref. to input common to both channels

**Bandwidth** : 15 kHz (-3 dB), linear phase response over ±3 kHz from the center of the band

**Selectivity** : 70 dB at ±25 kHz

**Output to phase Det.** : -20 dBm-0+3 dBm, both channels

**Phase Match** : ±10° or better between the two receiver channels

**Phase Det. Output** : ±6.0V for input of ±180°

**Phase Det. Linearity** : ≤1% over the range ±175°

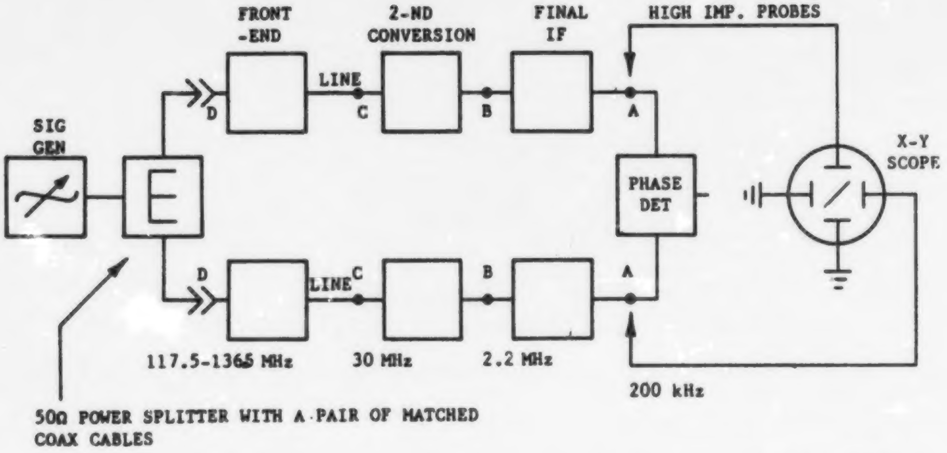
**Phase Reversal** : Reversal through 180° at input to phase comparator, controlled from bearing processor (TTL level)

**Group Delay** : 270us approx. receiver input to output of phase detector but not varying by more than ±10% over the ±3 kHz bandwidth and 80 dB dynamic range

## 1.4.9 DF Receiver Test Procedures

### Phase Match

Phase balance of the two receiver channels has to be measured step-by-step, from back to front, each time testing a common input to the two channel sections and probing the phase difference between the two outputs to the phase detector.


FRONT -END
2-ND CONVERSION
FINAL IF
HIGH IMP. PROBES
LINE
D
C
B
A
SIG GEN
PHASE DET
X-Y SCOPE
D
LINE
C
B
A
117.5-1365 MHz
30 MHz
2.2 MHz
200 kHz
50Ω POWER SPLITTER WITH A PAIR OF MATCHED COAX CABLES

NOTE: CONNECTORS A, B AND C ARE ALL SMA TYPE, D ARE TNC TYPE

### Procedure

1. Set up the oscilloscope for X-Y operation with equal gain in X and Y, verify that there is no phase shift between X and Y channels at 200 kHz. Connect scope probes to AA.

2. Disconnect both channels at FB and apply signal generator at 2.2 MHz via the power splitter to the inputs of final IF modules. Observe the phase difference of the fundamental on the Lissajoux figure on the "scope". If more than 10°, touch up alignment of the last IF filters.

3. Restore receiver connections at BB and break at CC. Apply signal generator at 30 MHz to the inputs of 2nd conversion modules. Observe the phase difference as before. If in excess of 10°, touch up alignment of 2nd conversion input tuned circuits.

4. Restore receiver connection at CC and break at DD. Apply signal generator at any RF within the band (117.5-136.5 MHz) to the two receiver inputs. (NOTE: A long cable may be used between the generator and the power splitter.) Observe the phase difference as before. If in excess of 10°, touch up the phase adjustment of LO, buffers in oscillator distribution module.

5. Return to normal setting for DF operation.

## 1.5 Bearing Processor Sub-System

### 1.5.1 Computation of the Bearing Angle

The main purpose of the bearing processor is to compute the angle of arrival (the bearing) of an incoming signal and to send the result to the numeric display.

The input of the bearing processor is the phase waveform received from the phase detector. Using this waveform and the North pulse, which give an indication when the North dipole is selected, the bearing can be determined.

The computation of the bearing is based on the Fourier analysis of the phase waveform. In fact the phase of the fundamental is the bearing. To achieve this, the waveform is first sampled and converted to numerical values. As the antenna is made of 16 dipoles, then 16 different samples are produced per rotation.

The samples are then multiplied by the sine and also by the cosine value corresponding to the dipole selected. The north dipole is at 0° and the East one is at 90° and so on. Each result is added to the previous one, and that for a complete cycle. If each sample is noted as $X_i$ (i being the dipole number ranging from 0 (North reference) to 15), then after one cycle the following two results are available:

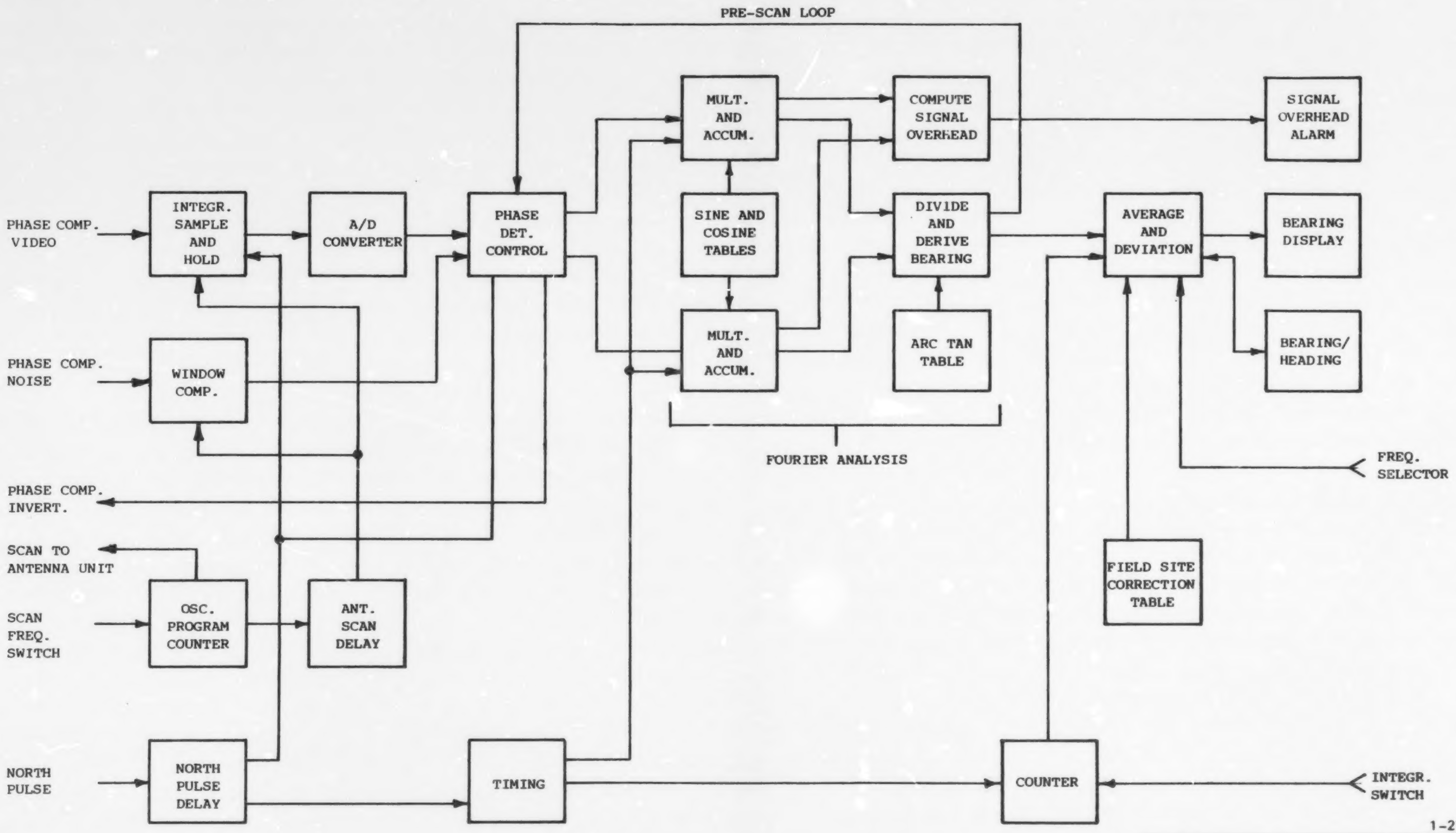
$$\left( \sum_{i=0}^{15} X_i \cos (22.5^\circ i) \right) \quad \text{and} \quad \left( \sum_{i=0}^{15} X_i \sin (22.5^\circ i) \right)$$

(360/16 = 22.5)

To find the bearing, then the sum of sine is divided by the sum of cosine. The arctangent of the result will give the bearing.

$$\text{Bearing} = \text{arctg} \left( \frac{\sum_{i=0}^{15} X_i \sin (22.5^\circ i)}{\sum_{i=0}^{15} X_i \cos (22.5^\circ i)} \right)$$

The Data Acquisition board is used to sample the phase waveform and to convert those samples to a numerical value. Then those values are sent to a DFT (Digital Fourier Transform) card which computes the sum of sine, and at the same time to another DFT card for the sum of cosine computation. The two results are finally read by the microprocessor which will compute the bearing.


PRE-SCAN LOOP
PHASE COMP. VIDEO
INTEGR. SAMPLE AND HOLD
A/D CONVERTER
PHASE DET. CONTROL
MULT. AND ACCUM.
SINE AND COSINE TABLES
MULT. AND ACCUM.
COMPUTE SIGNAL OVERHEAD
DIVIDE AND DERIVE BEARING
ARC TAN TABLE
FOURIER ANALYSIS
SIGNAL OVERHEAD ALARM
AVERAGE AND DEVIATION
BEARING DISPLAY
BEARING/ HEADING
FREQ. SELECTOR
PHASE COMP. NOISE
WINDOW COMP.
PHASE COMP. INVERT.
SCAN TO ANTENNA UNIT
SCAN FREQ. SWITCH
OSC. PROGRAM COUNTER
ANT. SCAN DELAY
FIELD SITE CORRECTION TABLE
NORTH PULSE
NORTH PULSE DELAY
TIMING
COUNTER
INTEGR. SWITCH

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| A | ORIGINATED | | Zoaie |

BAYLY ENGINEERING LTD a member of

SCALE
REMOVE BURR MAX 010R
MATERIAL
FINISH

TITLE
BEARING PROCESSOR
FUNCTIONAL BLOCK DIAGRAM

UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMALS ± ANGLES ± °

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. | |
|---|---|---|---|---|---|
| DS | 25.5.83 | | Zoaie | 066-0643.035 330.BD-B | A |

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

### 1.5.3 Integration of Noise

Direction finding by cyclical modulation of phase is easily accomplished when the signal is relatively strong. However, as the signal strength decreases. the bearing readout begins to fluctuate as a result of effective differential modulation of phase, caused by the background noise - internal or external to the system. If one assumes that the noise is random, then the fluctuation can be reduced by successive integration over a period of time. The bearing accuracy becomes then a trade-off between sensitivity and the response time.

The function of integration or averaging is performed successively in four different stages:

(1) 16 dipole pairs are scanned around the array circle, giving 16 samples of phase difference for the Fourier analysis to determine the bearing angle.

(2) The pulse width modulated signal derived from the phase detector is first integrated and then filtered to produce a phase waveform of scan frequency showing the steps of dipole pair switching.

(3) A sampling window of accurately fixed time width is applied over the flat section of each step. Over this time, a linear integrating circuit collects a charge proportional to the sample size, while averaging any ripple caused by noise or modulation of signal. The charge is held at the end of the window period and handed over for A/D conversion and the Fourier analysis.

(4) The Quasi-Doppler DF prototype, described here, has provision for four integration time constants, selected manually, giving response times from 0.1 seconds to 0.8 seconds, the longest one being used for the weak signal levels. Each scan cycle is analysed and the obtained bearing angles are further averaged over a given number of scan cycles: 8 for a 0.1 second response, up to 64 for a response of 0.8 seconds.

### 1.5.4 Pre-scan Cycle and the Correction to Phase Detector

The phase detector and its follow-up integration filter circuit present a periodic waveform of phase output made up of 16 steps for each scan cycle. Owing to certain internal reflections of the array, contribution of noise and receiver unbalance, it is possible for the peak steps of the phase waveform to reach, or even exceed, the ±180° limits which determine the normal range of operation of the phase detector. Under these circumstances, the phase waveform indicates isolated step readings of reverse polarity, leading to an error in the computed bearing.

Knowing which phase steps are exceeding the detector range and what is their polarity, it is still possible to obtain the correct measurement by shifting the phase detector characteristic by 180° (by inverting one of the input channels), and then correcting digitally for the amount of the shift. To make this possible, it is necessary to run a complete scan cycle (pre-scan) at the start of the processing sequence and to analyse the phase steps for close approach to the limits. This is done by the first microprocessor on the data acquisition board. The pre-scan cycle is run through with the normal polarity of the phase detector and a bearing angle is computed from the results. Owing to possible step reversals, it is recognized that this bearing angle may be in error by as much as ±10°, so the reading is not presented on the display. However, this accuracy is sufficient to carry out a correction procedure for a number of successive scans. For this purpose, any step positions are noted which exceed the ±130° limit. In these positions, the detector channels are reversed for the follow-up scans so that their phase readings can be taken nearer the centre of the detector characteristic. These step positions are counted from a nominal zero position determined by the bearing readout of the pre-scan cycle. The corrected steps which appear in the first eight positions of the scan cycle (positive half cycle) are then moved back by -180° in the digital section of the processor. Corrected steps in the second eight positions (negative half cycle) are then moved forward by +180°.

The final result of this process is a virtual extension of the phase characteristic of the phase detector to ±230°. The pre-scan required for detector corrections is repeated every nine cycles, i.e. each pre-scan cycle is followed up by eight corrected scans which are used for averaging and display of the corrected bearing.

A further detection network is employed to take care of errors in the close vicinity of the 180° discontinuity. A description of its operation is given in the details of the Phase Detector Module.

### 1.5.5 Signal Overhead Computation

The Doppler DF principle lends itself to determination of the angle of elevation as well as that of the bearing of the target transmitter. Whereas the bearing is given as the phase angle of the phase waveform relative to the North position, the elevation is a function of the relative amplitude of the phase waveform.

Thus, if the instantaneous value of the phase waveform is e

$$e = E \cos \varepsilon \sin (\omega t + \varphi)$$

Where:
E is the maximum amplitude of the waveform
$\varepsilon$ is the angle of elevation of the target above ground
$\omega$ is the Z ɪ x scan frequency
and $\varphi$ is the bearing angle relative to North

The Fourier analysis computes the sum components A and B of the sine and cosine of the bearing angle, where

$$A = \sum_{i=0}^{i=15} X_i \cos (22.5^\circ i) \quad \text{and } B = \sum_{i=0}^{i=15} X_i \sin (22.5^\circ i)$$

The amplitude of the fundamental scan frequency can be calculated as

$$E \cos \varepsilon = \sqrt{A^2 + B^2}$$

Hence, the elevation angle $\varepsilon = \text{arc cos} \sqrt{\dfrac{A^2 + B^2}{E^2}}$

E is maintained constant by a set of amplitude limiters and it corresponds to the scan frequency amplitude of the phase waveform when the target is at ground level.

The 'signal overhead' alarm is activated when $\sqrt{\dfrac{A^2 + B^2}{E^2}} \leq \cos 60^\circ \leq 0.5$

or (in practice) $\dfrac{A^2 + B^2}{E^2} \leq 0.25$

### 1.5.6 Bearing/Heading Conversion

Both bearing displays, digital as well as analog, show the bearing angle of the target as seen from the DF site. By pressing the 'Heading' button, the operator has a choice of indicating the heading direction which has to be followed by the pilot in order to reach the airport. On this command, both the digital and the analog indicators change to Heading and a green light comes on to indicate the condition. The conversion from bearing to heading is by a shift of 180° and is obtained digitally as part of the program of the second microprocessor (Microprocessor and Memory Module).

### 1.5.7 Determination of Data Valid Condition

The Fourier analysis and microprocessor system used for processing the bearings, has effectively a wide band characteristic and will respond to any sequence of samples from the phase detector output. Thus, when there is no signal present, the bearings computed in a sequence of scan cycles will show a wide and random fluctuation. This is obviously confusing for the operator who does not wish to be distracted when there is no plane to follow.

To avoid this inconvenience, a 'data valid' concept is established and the readings which do not meet the data valid criterion are simply blanked out.

A running average is computed of eight complete scan bearings. Any next scan bearing is compared with this average and is accepted only if it does not deviate by more than an agreed limit. The accepted bearings are now averaged for a total of 8, 16, 32 or 64, according to the setting of the integration switch. If more than 50% of the individual scan bearings are outside the acceptable spread limit, then the obtained bearing readout is not considered valid and the display is blanked out. For the 16 dipole installation, it was found that a spread limit of 10 degrres will reduce the noise fluctuation of bearing to approximately $1^{\circ}$ or better at the 3 uV/m sensitivity limit.

### 1.5.8 Site Error Correction

Any DF system is subject to bearing errors depending on azimuth and frequency and on the complex status of environmental conditions. The bearing errors are a combination of:

i Instrumental errors (internal to the system)

ii DF field site errors

iii Transmitter site errors

The instrumental errors are a fixed part of the system and quite repeatable. They are limited by a tight set of specifications.

The DF field errors consist of the effect of diffraction and reflections from objects in the close proximity to the DF site (up to 20 wavelengths away). They can be calibrated to some approximation for a fixed configuration of conducting objects (wires, vehicles, ladders, antenna whips, etc.). They may be also affected by weather and the condition of the ground.

Transmitter site errors may be caused by reflecting objects in the vicinity of the transmitter or by directivity of the transmitter antenna. This type of error usually appears in ground transmissions, such as from the control tower or from a portable transmitter used for calibration. This error is often frequency dependent.

The digitial bearing processor of the Bayly prototype can be programmed to compensate for a large proportion of the bearing errors so as to present the operator with a more accurate bearing capability. The compensation is incorporated in the software of the second microprocessor (Microprocessor and Memory Module) and takes care of the combined area of azimuth and frequency, in steps of 5 degrees and for up to 5 frequency sub-bands.

The compensation effectively reduces the combination of errors i) and ii) (instrumental and DF field site). The setting up procedure requires a set of calibration charts for the frequencies and azimuth points in question. Bearing errors are then computed from these charts and a set of corrections is programmed into the microprocessor memory.

## 1.5.9 BEARING PROCESSOR SPECIFICATIONS

### 1.5.9.1 Functional

(a) Principle : Digital data processing for computing bearing and elevation of an incoming signal based on 16 samples per scan of antenna rotation

(b) Scan Frequency : 100 Hz approx. ±10%

(c) Response Time : 0.1 sec. plus Integration Constant (1, 2, 4 or 8 multiplied by 0.125 sec.)

(d) Accuracy : 0.2°

(e) Readout Resolution : 0.1°

(f) Sample Window : Integration, sample and hold of the steady state level of each input pulse

(g) Integration of Noise : Rejection of excessive error compared against a running average of eight.

Integration of average result of 8, 16, 32 or 64 samples, according to setting of the integration switch.

(h) Control of Phase Detection Range : To enable acceptance of phase angle samples of up to ±230°

(i) Automatic Reset : To restart the programs when power is appliied to the system, or after an emergency stop of the system

(j) Inputs:

North Pulse (0° bearing reference) : 200 mV p-p, 10 μs approx.

Phase Step Video : Normal Level ±5.8V ±0.1V

Phase Detector Noise : The level is 5% higher than the phase step video

Frequency Code : 8 MSB bits binary code TTL Level

Integration Constant : 2 bits binary code TTL Level

QDR/QDM : TTL Level

(k) Outputs:

Scan Clock : 32 times scan frequency, 100 mVolt p-p

Bearing/Handling Display : 4 digits BCD format TTL Level

Data Ready : TTL Level

Data Valid : TTL Level

Signal Overhead : Set to activate when target elevation ≥60° TTL Level

(l) North Pulse Delay Adjustment : To compensate for the group delay of the DF system (180-220 μs)

(m) Scan Delay Adjustment : To allow correct setting of the sample window

(n) Phase Detection Noise Adjustment : To adjust detection limits of the ±180° threshold noise

1.5.9.2 **Electrical Power** : +5V ±5%
±15V ±1V

### 1.5.9.3 Environmental

Operating Temperature : 0° - 35°C

Humidity : $\leq 80\%$

## 1.6 Displays and Controls Sub-System

### 1.6.1 Control and Display Functions

All control and display functions for the Doppler D.F. are handled by control/display panels. There are normally two, one at the receiver site (also called the 'Remote Panel') and one at the Operator's site (also called the 'Local Panel'), although a system may use more than one Operator's Control Panel. The displays and controls are almost identical on both panels, with the exception of the circular display, the storage display and its controls (provided on the Operator's Panel only) and the LOCAL/REMOTE switch (Receiver Control Panel) -vs- the MASTER/SLAVE switch (Operator's Control Panel). Communication between the two control/display panels is over a standard 4-wire telephone line which carries the data (FSK) and voice (receiver audio or optional telephone conversation between the two sites).

The requirements for the control and display sections are outlined below.

### 1.6.2 Requirements for Remote Site

(a) The following data is generated by this section:

Bearing/Heading, 4 digits, BCD format

Channel Number, 1 digit, BCD format
Frequency, 6 digits, BCD format

Note: only the channel number OR the frequency is transmitted, depending on the operating mode selected

Emergency Alarm : when a signal is received on the Emergency Channel

Sense Indication : bearing (QDR) or heading (QDM)

Data Valid : to indicate that the displayed bearing is meaningful

Signal Overhead : indicates that the transmitting craft passes over the site (elevation $\geq 60^{\circ}$)

Remote/Local Indicator : tells the operator if the receiver is under the control of the Control Centre or is operated by a person at the Receiver Site

System Alarm : to detect and report a break in communication with the Control Site

(b) The following data is either received from the Operator Control site or generated from the receiver control panel and must be processed at the Receiver site

Desired Channel Number (10 Channels and Emergency) or operating frequency

Sense Selection : bearing (QDR) or heading (QDM)

Integration Constant Selection (4 positions)

Auto/Manual Selection of the Emergency Channel

Remote Power ON/OFF : to permit Receiver shutdown and activation from the Control site

System Test Facility : for remote testing of the Receiver installation (4 positions)

Antenna Scan Frequency : can select one of 3 different scan frequencies to minimize interference

(c) Another control feature of the Receiver site:

Remote/Local Control Switch : to transfer control from the Control site to the Receiver site

### 1.6.3 Requirements for Local Site

(a) The signals described in section 1.6.2 (a) are processed to provide the following indications:

4 Digit Bearing/Heading Readout

Sense Indicator Lamp : to alert the operator that the heading is displayed

Channel Number Indicator (10 channels + Emergency) OR Receiver frequency readout

System Alarm Warning Lamp

Emergency Channel Receiver Indicator

Data Valid Indicator

'Signal Overhead' Indicator Lamp

(b) To generate the signals described in section 1.6.2 (b), the following controls are provided

System Test Selectors : selection of 4 different bearings

Antenna Scan Frequency : selection of 3 different frequencies

Auto/Manual Emergency Selector:

Integration Constant : up to 4 different integration times

Heading/Bearing Selector (default to 'Bearing' mode)

Remote Receiver Power ON/OFF

Channel Selection : 10 'normal' and 1 Emergency Channel

OR

Frequency Selection : all 720 channels used in the VHF ATC band.

(c) Other features at the Control Site:

Storage of Bearing or Heading on demand

Aux Data Output (Parallel Format with Connector) : available but not wired to the output

Voice Output over an external speaker as well as an Auxilliary output

### 1.6.4 Operator's Control and Display Panel

The system is normally controlled from one Operator's Control/Display Panel, which would be located in the airport's control room, while the Receiver Control/Display Panel would be used for maintenance purposes only. Additional Operator's Control/Display Panels may be added to the system to extend the monitoring and control capabilities to other locations.

Fig. 1.6.4 shows the front panel of the Operator's Control/Display Panel, while Table 1.6 provides a detailed description of the controls and displays. As mentioned previously, the controls and displays on the Receiver Control/Display Panel are essentially identical.

## TABLE 1.6
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| 1. | PWR SW. | Applies ac power to the CDU (Control/Display Unit) | Switch will not be included on production models |
| 2. | PANEL ACTIVE lamp (white) | When lit, indicates that this CDU controls the system | Refer to Item 8. |
| 3. | REMOTE POWER switch | Controls on/off dc power supplies in receiver section of Receiver Unit (the Antenna Unit is powered by dc from the RU) | This switch is disabled if the LOCAL/REMOTE switch on the Receiver Control/Display Panel is in the LOCAL position |
| 4. | DIMMER Rotary Control | Controls brightness of panel indicator lamps and displays | Disabled for LAMP TEST |
| 5. | LAMP TEST pushbutton | When pressed, all lamps should light to full brightness | No DIMMER control |
| 6. | SYSTEM ALARM lamp (red) | When flashing, indicates a malfunction at the Receiver Unit or break in the telephone cable from the CDU to the RU | |
| 7. | SYSTEM ALARM RESET pushbutton | When pressed, resets the system alarm to extinguish the SYSTEM ALARM lamp after the trouble has been cleared. Typically, the button must be pressed during system start-up after REMOTE POWER is switched on | If the trouble persists, the SYSTEM ALARM RESET has no effect |

## TABLE 1.6 (Cont'd)
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| 8. | MASTER/SLAVE switch | When set to MASTER position, the CDU has both control and display capability. When set to SLAVE position, the CDU has display capability only. | One or several CDU's can be used in the system. Only one CDU can be MASTER at any given time (PANEL ACTIVE lamp 'on') |
| 9. | PHONES jack | Used with standard headset to monitor audio (if any) on the df receiving channel using an omni-directional antenna for signal pick-up | Not a telephone facility |
| 10. | VOLUME rotary control | Controls level of audio output from omni-directional antenna receiving channel | |
| 11. | ANT. SCAN /1-2-3 rotary switch | Three positions for selecting df antenna electronic rotation speed. Percentage variation is about 8% above and below mid speed (position 2) | If signal 'flicker' is present, there is one position where the effect is minimal |
| 12. | INTEGR. SEC/ .1-.2-.4-.8 rotary switch | Four positions for selecting the minimum integration time necessary to accurately resolve a df bearing | This integration factor is dependent on both the electronic rotation switching speed of the pairs of dipoles in the antenna array and the signal strength |
| 13. | CHANNEL or FREQUENCY SELECT pushbutton and lamp arrangement (see below) | This keyboard arrangement consists of ten pushbuttons (marked 0 through 9) and ten lamp indicators (amber). There are two modes of operation. See * entries below for channel select mode. See ** entries below for selectable frequency mode | The lamp indicators are mounted above or adjacent to their corresponding pushbuttons |

## TABLE 1.6 (Cont'd)
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| 14. | 0-1-2-3-4-5-6-7-8-9 pushbuttons for above keyboard arrangement | * Channel select mode. One pushbutton is used to select one of the ten df channels by number. The channel frequency is pre-set in the Receiver Unit for any channel number selected | |
| 15. | Indicator lamps (ten amber) for above pushbuttons | * When a channel is selected (as above), the corresponding amber lamp will come 'on' | |
| 16. | FREQ. MODE pushbutton. NOTE: for cancellation of FREQ. MODE, see Item 17 | ** Selectable frequency mode. When pressed, initiates the selectable frequency mode of the 0 through 9 pushbuttons. This action does not by itself disturb the operation of the Receiver Unit. Instead, the RU is made ready to accept tuning to any frequency in the VHF ATC band | Amber (or red) lamp goes out when FREQ. MODE button is pressed and the last frequency that was selected in this mode is selected again |
| 17. | FREQUENCY MHz six-place red numeral display with fixed three-place decimal resolution. NOTE: This display should normally be blank. If not, the FREQ. RESET button (Item 18) should be pressed first | ** Can be used during FREQ. MODE only. This display is normally blank. The 0 through 9 pushbuttons can be used to enter a six digit frequency value on the display. When the sixth (and last) numeral is entered, the Receiver Unit is instantly retuned to the displayed df receiving frequency. This frequency should be centred on a valid df channel in the VHF ATC band. (Channel spacing is required to be 25 kHz) | The actual switch to the new frequency can only take place when the complete channel/ frequency information has been entered |

## TABLE 1.6 (Cont'd)
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| (Cont'd) | (Cont'd) | (Cont'd) | (Cont'd) |
| 17. | FREQUENCY MHz six-place red numeral display with fixed three place decimal resolution | ** The FREQ. MODE (see above) can be cancelled including blanking of the FREQUENCY MHz display. This is done by pressing the FREQUENCY RESET button (see Item 18) | Note that when the amber lamp comes on, a channel has been selected |
| 18. | FREQ. RESET pushbutton | ** Can be used during FREQ. MODE or channel select mode. When pressed, the channel lamp or the FREQUENCY MHz display (complete or incomplete) is cancelled. When cancelled, a new or corrected FREQUENCY MHz display can be entered. | The FREQ. RESET button will always leave the receiver in the channel select mode. If the frequency select mode is desired, the FREQ. MODE pushbutton must be pressed again |
| 19. | EMERGENCY indicator lamp (red) | When lit, indicates that the emergency channel is selected and locked on (see Item 20) | |
| 20. | EMERGENCY mode MAN./AUTO switch | Selects system EMERGENCY operating mode<br>In the MAN. position, the df system will operate normally. To operate on the emergency channel, the EMERGENCY pushbutton (see Item 21) must be pressed. When the EMERGENCY light (see Item 19) comes on the Receiver Unit is locked on the emergency channel | |

## TABLE 1.6 (Cont'd)
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| (Cont'd) | (Cont'd) | (Cont'd) | (Cont'd) |
| 20. | EMERGENCY mode MAN./AUTO switch | The system is released from this mode when a 0 through 9 pushbutton is pressed, or a frequency is selected | |
| | | In the AUTO position, a signal (call) on the emergency frequency will automatically lock the Receiver Unit on the df emergency channel. At the same time, the EMERGENCY lamp will light | If the emergency call signal fades intermittently or ceases, the system will hold in AUTO emergency mode for about 1.5 sec., then revert to the normal df channel previously selected |
| 21. | EMERGENCY pushbutton | Used to manually select the system emergency df channel operation. The MAN./AUTO switch can be set to either position without affecting this function | The EMERGENCY pushbutton is another channel select button and works the same way as the 0 through 9 pushbuttons. However, the associated frequency (121.500 MHz) is factory selected and cannot be easily altered in the field. |
| 22. | NESW numerical and analog bearing display (red numerals and analog dot) | When a df bearing in a selected receiving channel has been resolved, the bearing angle (in degrees) is displayed numerically across the centre of the circular clear red plastic overlay. At the same time, an analog of the bearing angle (±5°) is indicated by a red dot light at the overlay circumference | Any NESW display bearing information can be blanked for one of two reasons. First, if the associated df signal becomes invalid (i.e. if the transmission ceases or becomes too weak). Second, if the transmitting aircraft passes over the receiver site (overhead pass condition). |

## TABLE 1.6 (Cont'd)
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| (Cont'd) | (Cont'd) | (Cont'd) | (Cont'd) |
| 22. | NESW numerical and analog bearing display (red numerals and analog dot) | The displayed bearing angle (both numerical and analog) is visible only when a valid signal is received on the selected channel (or frequency). The display will be blanked if the signal is lost, or the aircraft passes over the installation | Normally (but see Step 23) at the instant of NESW bearing information 'loss', the numerical part of the information is automatically transferred to appear on the STORED BEARING display. This action occurs for every 'loss' so that the STORED BEARING display is always updated with the last valid NESW display bearing |
| 23. | STORED BEARING numerical display | Any df bearing angle appearing numerically on the NESW display can be 'permanently stored on the STORED BEARING display. This is done by pressing the STORE button momentarily (no effect on the NESW display). This STORE action will also occur automatically for the first valid emergency df bearing if the EMERGENCY mode MAN./AUTO switch is in the AUTO position when the emergency signal is last (see Item 20)<br>The STORED BEARING/STORE feature is intended to protect NESW display bearing information under certain operational conditions. Examples are: during aircraft overhead pass (see Item 27); and during an EMERGENCY channel alert | Observe that (unlike the action of Step 22), when the STORE button is used, the STORED BEARING display cannot be blanked out except by pressing the RESET button<br>Note also, that when no valid display is shown on the NESW display, the RESET button has no immediate visible effect. However, the STORED BEARING display is unlocked and will be automatically updated again when the next valid bearing is received. |

## TABLE 1.6 (Cont'd)
## OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

| ITEM # | MARKING/NAME | OPERATING FUNCTION | REMARKS |
|---|---|---|---|
| (Cont'd) | (Cont'd) | (Cont'd) | (Cont'd) |
| 23. | STORED BEARING numerical display with STORE and RESET buttons | When required, the RESET button is used to 'unlock' the stored display | |
| 24. | SYSTEM TEST/ 45°-135°-225°-315° pushbuttons (four) | When one pushbutton is pressed, the circular NESW display will indicate the numerical and analog angle of a test bearing corresponding to the pushbutton marking. The display is resolved from a signal radiated by one of four test antennas that are installed on the antenna array | This feature can be used both to encourage operator confidence and to facilitate maintenance requirements |
| 25. | HEADING pushbutton | When pressed, the NESW numerical and analog bearing angle display will show a 180° change in the display angle. This shifted bearing is that of the df antenna site made from the aircraft. Ignoring wind direction vectors, it is the heading to be maintained by the aircraft if it is required to fly over the df antenna site | |
| 26. | HEADING mode indicator lamp (green) | When lit, indicates that the NESW numerical and analog display angle has become a heading angle | |
| 27. | SIG. OVERHEAD indicator lamp (blue) | When lit, indicates that the aircraft is within an air space shaped like an inverted cone with its apex on the antenna site. The slope of the cone relative to ground horizontal is about 60° | The NESW display will be blanked during this condition since any reading would be too inaccurate to be useful. However, as usual, when the NESW display becomes inactive, the last valid reading will be transferred to the 'Stored Display' |

### 1.6.5 Receiver Control/Display Panel

On the Receiver Control/Display Panel, Item #8 is called the LOCAL/REMOTE switch. The function is very similar: In the REMOTE position, the Receiver Panel has control and display capability, while any Operator's Panels will have monitoring function only (their PANEL ACTIVE lamps will be off no matter where the MASTER/SLAVE switch is set to show that they are no longer in control). In the LOCAL position, control is transferred to the Operator's Panel(s) and the Receiver Control/Display Panel is acting only as a monitor.

Item #22 and the analog NESW display referred to in Item #23 are not incorporated in the Receiver Control/Display Panel, and any reference to the 'Stored Display' or the analog NESW display should be deleted for this unit. Physically, the digital (or numerical) Bearing Display is moved to the location held by the STORED DISPLAY on the Operator's Panel.

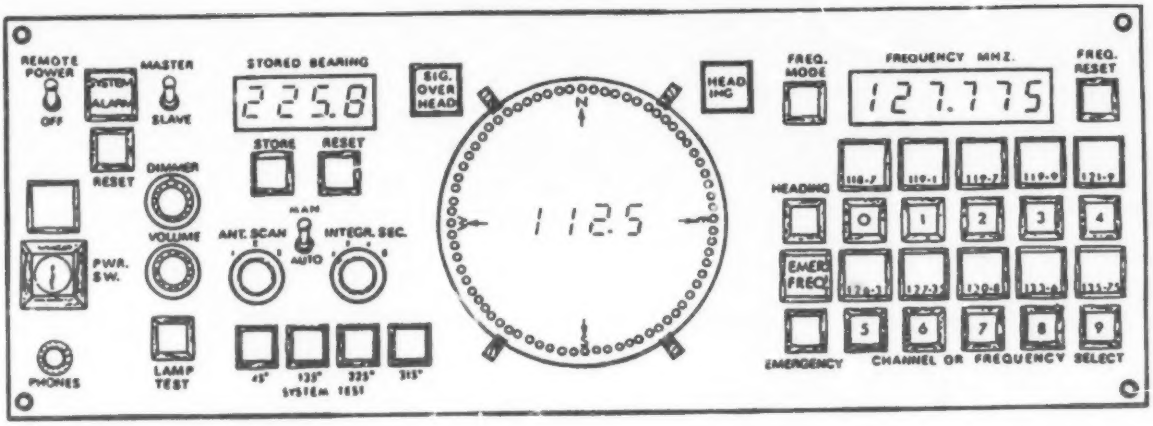

REMOTE POWER
OFF
SYSTEM ALARM
RESET
MASTER
SLAVE
STORED BEARING
225.8
STORE
RESET
SIG. OVER HEAD
HEAD ING
N
112.5
DIMMER
VOLUME
PWR. SW.
PHONES
LAMP TEST
ANT. SCAN
MAN
AUTO
INTEGR. SEC.
45°
135°
225°
315°
SYSTEM TEST
FREQ. MODE
FREQUENCY MHZ.
127.775
FREQ. RESET
118-7
119-1
119-7
119-9
121-9
HEADING
0
1
2
3
4
EMER FREQ
5
6
7
8
9
EMERGENCY
CHANNEL OR FREQUENCY SELECT

FIGURE 1.6.3

OPERATOR's CONTROL/DISPLAY PANEL, CONTROLS AND INDICATORS

## 1.7 Data and Voice Transmission Sub-System

### 1.7.1 General Description

The VHF Doppler DF system can be operated either from the Operator's site ('Local' control/display panel) or from the Receiver Site ('Remote' control/display panel). Communication between the two panels is over a standard 4-wire telephone line which carries the data (FSK transmission) and the voice (receiver audio or optional telephone conversation between the two sites).

The following features are incorporated:

Link operates on a standard 4-wire telephone quad.

'Data over Voice' operation with voice frequencies limited to 2.3 kHz; Data channel to use FSK in the 2.5 to 3.0 kHz band.

Data generated at either site is serialized and sent as a 32 bit package in a 0.1 sec. time frame.

Data received at either site is re-converted to parallel form for further processing.

Voice will normally come from the received transmission, but can be replaced by a telephone link if personal communication is needed between the two sites.

Transmission levels of voice and data can be adjusted in both directions by up to 40 dB to allow for losses in the telephone line. A block diagram of the overall data and voice sub-system is shown in Fig. 1.7.

### 1.7.2 Data Transmission

Data communications between the local and remote sites is accomplished using frequency shift keying (FSK) modulation within the 3 kHz limitation of a standard telephone line and by limiting the voice band to 2.3 kHz so that the data signals can be placed above the voice band on the line. One line is dedicated to each direction, so that the format and frequencies used in each direction can be identical.

All data to be transmitted should be in Binary or BCD format. A 32 stage Parallel-In/Serial-Out shift register converts the data to serial format and sends it to the FSK Modulator. The clock rate for the register is 416.67 Hz. This, and other critical frequencies, are derived from a 1.76 MHz crystal controlled master clock.

The data transmission is initiated by start pulse which comes once every 100 msec. Thus, the format of transmission is: 1 Start Bit + 30 Data Bits + 1 Stop Bit, or a total of 32 Bits sent within 80 msec., followed by a 20 msec. pause (to allow time for processing).

The FSK Modulator synthesizes a sine wave of 2573 Hz (Bit=0) or 2794 Hz (Bit=1) from the master clock. The synthesizer creates the sine wave in 18 steps, so that the clock frequency has to be 18 times the output frequency. This clock frequency is derived by dividing the master clock either by 38, or by 35, depending on whether the transmitted bit is a 0 or a 1. When no data is transmitted (e.g. during the 20 msec. pause), the synthesizer generates a steady signal of 2573 Hz.

Audio signals may be either from the received radio signals, or the optional telephone facility. These signals are passed through a 2.3 kHz low pass filter to eliminate unwanted harmonics which may interfere with the data band and the audio and data tones are combined in a mixer. A buffer amplifier provides the proper power levels and source impedance for the telephone line.

### 1.7.3 Data Recovery

At the receiving end of the link, the audio and data signals are separated again by low and high pass filters.

A carrier detector monitors the data tones to activate the System Alarm if these tones should be interrupted. The FSK Demodulator recovers the data in serial form and sends them on to the Serial-to-Parallel Converter. The Serial-to-Parallel Converter consists of a 32 stage Serial-In/Parallel-Out shift register whose clock is triggered by the reception of the Start Bit. Again, this clock is derived from the local master clock to guarantee its accuracy and stability.

When the Start Bit appears on stage 32, the circuit checks for the presence of the Stop Bit in stage 1 and then stops the register clock. Various strobes are now generated to initiate the appropriate processing and finally the register clock circuitry is reset to wait for the next Start Bit. If the Stop Bit is not found, the transmission is assumed to be in error, the data is cleared from the shift register, and no processing is initiated. Thus, checking for both the Start and the Stop Bits provides a primitive form of error detection to check the data stream for proper format. For most of the functions controlled by the data stream, this feature provides sufficient security since the information is updated every 1/10 of a second and an error in a display would be corrected in the next update causing, at worst, a slight flicker in the display.

Almost all the critical functions are at the Receiver Panel and since there was a considerable number of spare bit in the 'Operator-to-Receiver' direction, it was decided to use two bits (at different positions in the data stream) for each of the critical functions. The relevant bits are compared at the other end of the link and the new information will only be accepted if the status of these two bits is identical.

Functions which fall into this category are:

- Channel or Frequency Selection
- Remote Receiver Power ON/OFF
- System Test, and
- QDM/QDR Selection

In the Receiver-to-Operator path only the Emergency Reception needs to be secure since it could otherwise cause an erroneous switching to the Emergency Channel.

The Bit Assignment for the data stream is as follows:

## TABLE 1.7 : DATA BIT ASSIGNMENT

| Bit # | Function (Operator-to-Rx) | Function (Rx-to-Operator) |
|---|---|---|
| 1 | Start | Start |
| 2 | System Test ON/OFF (1) | Digit Position Bit 2 |
| 3 | System Test Position Bit 1 | Digit Position Bit 1 |
| 4 | System Test Position Bit 0 | Digit Position Bit 0 |
| 5 | Int. Const. Sel. Bit 1 | Digit Value Bit 3 |
| 6 | Int. Const. Sel Bit 0 | Digit Value Bit 2 |
| 7 | Key Pressed (1) | Digit Value Bit 1 |
| 8 | Digit Value Bit 3 (1) | Digit Value Bit 0 |
| 9 | Digit Value Bit 2 (1) | Bearing Hundreds Bit 1 |
| 10 | Digit Value Bit 1 (1) | Bearing Hundreds Bit 0 |
| 11 | Digit Value Bit 0 (1) | Bearing Tens Bit 3 |
| 12 | QDM/QDR Selector (1) | Bearing Tens Bit 2 |
| 13 | Rem. Rx Pwr ON/OFF (1) | Bearing Tens Bit 1 |
| 14 | Ant. Scan Freq. Bit 1 | Bearing Tens Bit 0 |
| 15 | Ant. Scan Freq. Bit 0 | Bearing Units Bit 3 |
| 16 | QDM/QDR Selector (2) | Bearing Units Bit 2 |
| 17 | Digit Value Bit 0 (2) | Bearing Units Bit 1 |
| 18 | Digit Value Bit 1 (2) | Bearing Units Bit 0 |
| 19 | Digit Value Bit 2 (2) | Bearing Tenths Bit 3 |
| 20 | Digit Value Bit 3 (2) | Bearing Tenths Bit 2 |
| 21 | Key Pressed (2) | Bearing Tenths Bit 1 |
| 22 | System Test ON/OFF (2) | Bearing Tenths Bit 0 |
| 23 | Rem. Rx Pwr ON/OFF (2) | Emergency Rx (1) |
| 24 | (spare) | Overhead Pass Indicator |
| 25 | (spare) | QDM/QDR Indicator |
| 26 | (spare) | Data Valid |
| 27 | (spare) | LOCAL/REMOTE Indicator |
| 28 | (spare) | System Alarm |
| 29 | (spare) | Emergency Rx (2) |
| 30 | (spare) | (spare) |
| 31 | (spare) | (spare) |
| 32 | Stop | Stop |

### 1.7.4 The Voice Link

The Voice Signal from the receiver Audio Channel is passed through a 2.3 kHz Low pass filter onto a mixer where it is combined with a Data signal. The combined voice and data signal is amplified in a buffer amplifier/driver connecting to the telephone line.

At the operator's control end the incoming signal is brought to a voice/data separation filter. The voice output is then amplified to drive the local loudspeaker, the volume control for which is provided on the front panel.

Two-to-four wire Hybrid modules are provided, one at each end to facilitate connection of standard 2-wire telephones to the voice link to allow communication between the local and remote sites for maintenance purposes.

## 1.8 OMNI-DIRECTIONAL MONITORING RECEIVERS

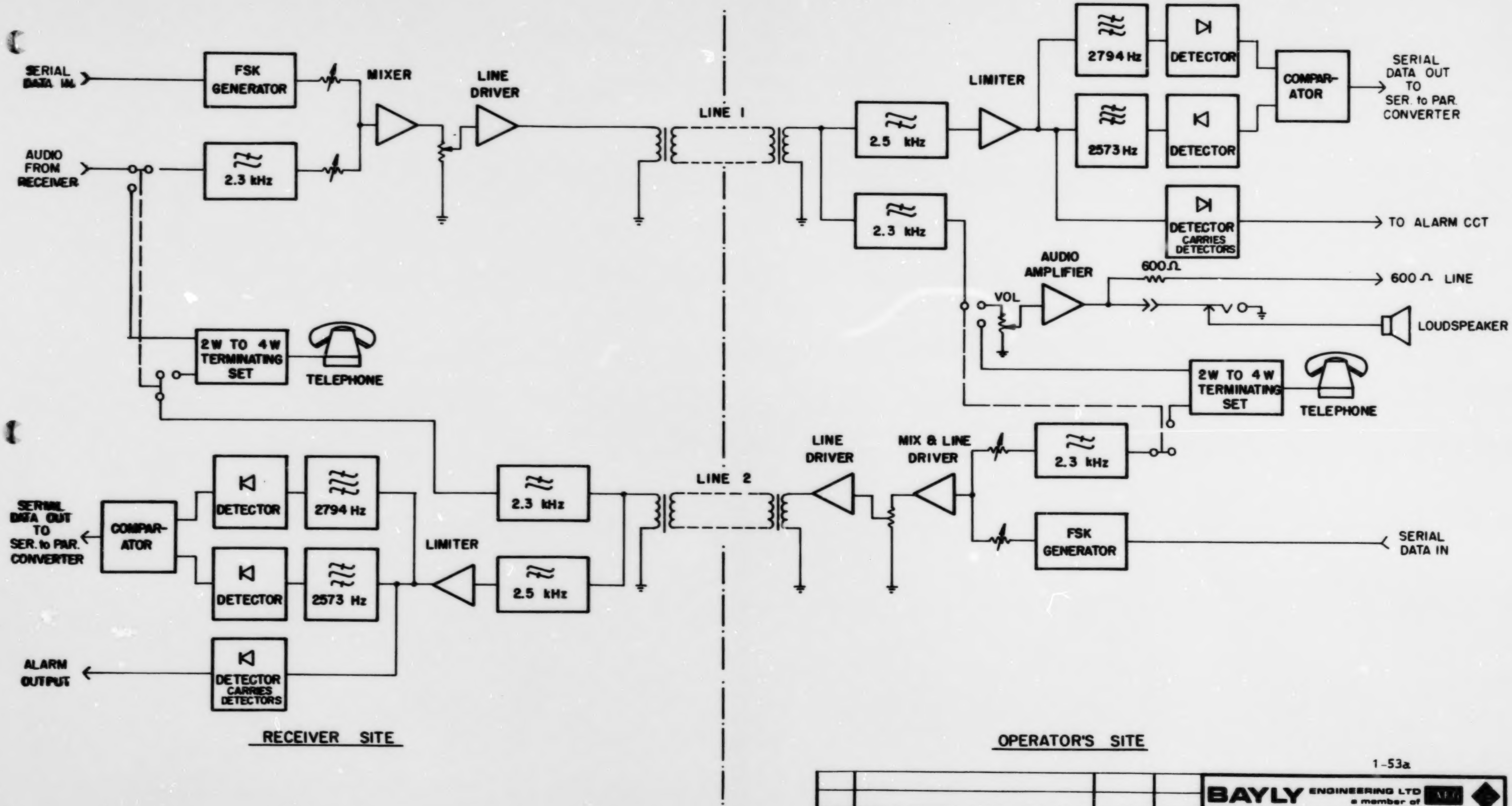
### 1.8.1 Requirement

In parallel with the task of obtaining a bearing on a radio target, the DF System may be required to pick up the audio intelligence of the incoming signal mainly for its identification with that received on the communications equipment. It may also be required to constantly monitor the emergency channel frequency and to alarm the operator when an emergency signal is detected.

These two functions (basically optional) are built into the present prototype with an additional facility of allowing the DF system to tune in automatically to the emergency signal and to indicate its bearing.

### 1.8.2 Configuration

The signals for the Audio and Emergency Sub-system are picked up from an omni-directional antenna providing an uninterrupted reception anywhere inside the entire input band. The RF signals are amplified in the broad band amplifier module (RF Omni-Channel) inside the Antenna Unit and then fed down the connecting cable to the Receiver Unit, Emergency Channel module. A power divider inside this module divides the signal into two paths feeding the Emergency Receiver and the Audio Receiver respectively.


SERIAL DATA IN
FSK GENERATOR
MIXER
LINE DRIVER
AUDIO FROM RECEIVER
2.3 kHz
LINE 1
2.5 kHz
LIMITER
2794 Hz
DETECTOR
2573 Hz
DETECTOR
COMPAR-ATOR
SERIAL DATA OUT TO SER. to PAR. CONVERTER
2.3 kHz
DETECTOR CARRIES DETECTORS
TO ALARM CCT
AUDIO AMPLIFIER
600Ω
600 Ω LINE
VOL
LOUDSPEAKER
2W TO 4W TERMINATING SET
TELEPHONE
2W TO 4W TERMINATING SET
TELEPHONE
LINE DRIVER
MIX & LINE DRIVER
2.3 kHz
FSK GENERATOR
SERIAL DATA IN
LINE 2
SERIAL DATA OUT TO SER. to PAR. CONVERTER
COMPAR-ATOR
DETECTOR
2794 Hz
DETECTOR
2573 Hz
LIMITER
2.3 kHz
2.5 kHz
ALARM OUTPUT
DETECTOR CARRIES DETECTORS
RECEIVER SITE
OPERATOR'S SITE

1-53a

**This drawing is the property of BAYLY ENGINEERING LIMITED and may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others without written permission.**

| REV NO | REVISION | DATE | APPR BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |

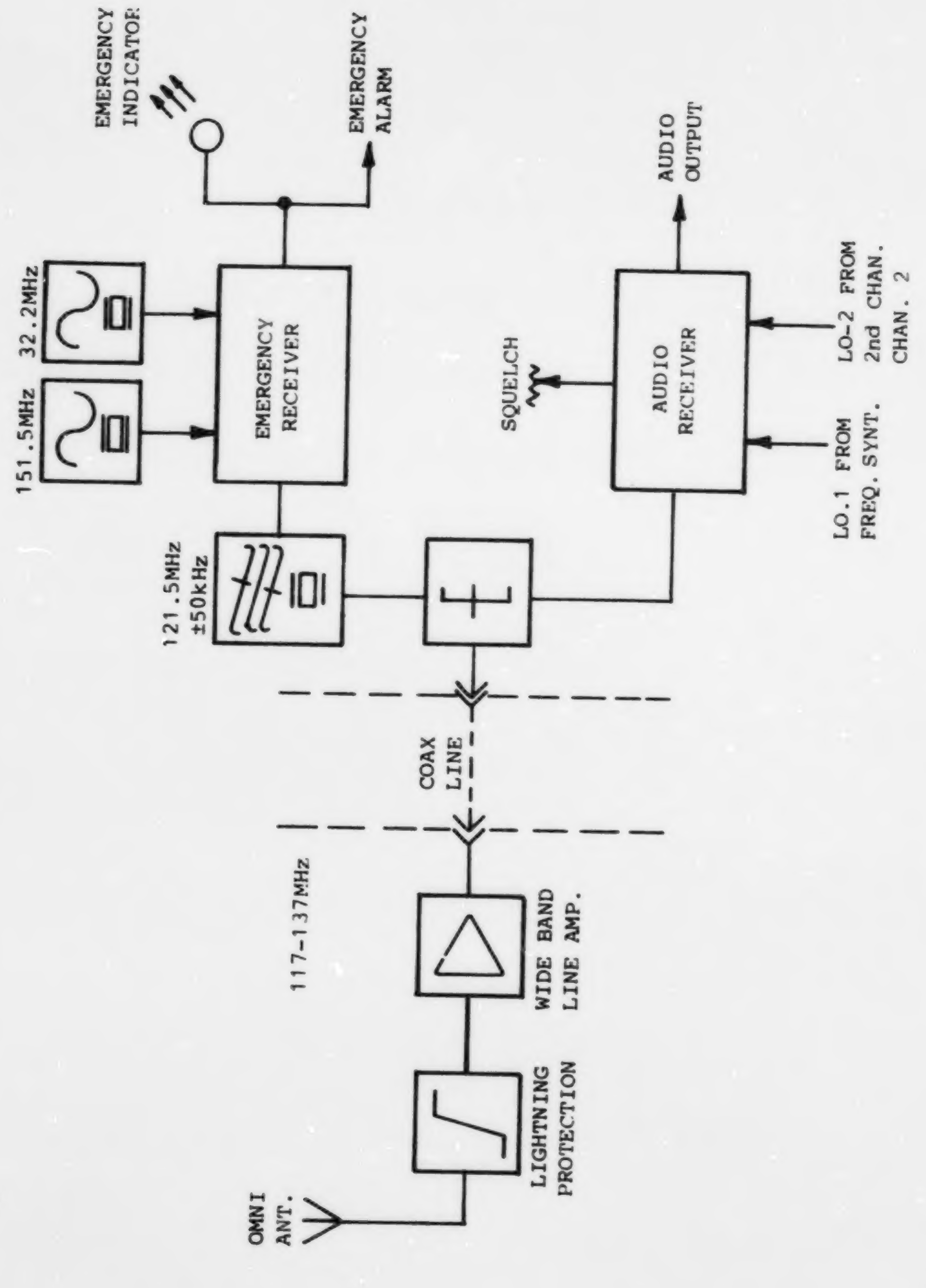
DRAWN BY AL
DATE APR.6, '83
CHECKED BY
APPR. BY ZAK 14.4.83

BAYLY ENGINEERING LTD a member of AEG

TITLE
DATA / VOICE TRANSMISSION
Functional Block Diagram

DWG NO. 066-0643.037 482.BD-B

1.8.3


EMERGENCY INDICATOR
EMERGENCY ALARM
AUDIO OUTPUT
151.5MHz
32.2MHz
EMERGENCY RECEIVER
SQUELCH
AUDIO RECEIVER
LO.1 FROM FREQ. SYNT.
LO-2 FROM 2nd CHAN. CHAN. 2
121.5MHz ±50kHz
COAX LINE
117-137MHz
WIDE BAND LINE AMP.
LIGHTNING PROTECTION
OMNI ANT.

| | | | |
|---|---|---|---|
| | | | |
| | | | |
| A | ORIGINATED | 83.05.25 | Zaak |
| REV. NO. | REVISION | DATE | APPR. BY |

DRAWN BY IC DATE May 25/83 CHECKED BY APPR. BY Zaak

BAYLY ENGINEERING LTD a member of

TITLE OMNI-DIRECTIONAL
MONITORING RECEIVERS
BLOCK DIAGRAM

DRAWING NO.

### 1.8.4 The Audio Channel

In the audio channel the signal is tuned in by means of the same 1st local oscillator as the DF receiver. Similarly, the 2nd conversion is made with the same 2nd local oscillator. There is no third conversion and the output of the second IF (2.2 MHz) is fed directly to the AM detector. An audio amplifier with volume control and an audio power stage to feed a loudspeaker, completes the circuit.

### 1.8.5 The Emergency Channel

The path of the emergency channel goes via a 121.5 MHz crystal filter in order to improve the adjacent channel selectivity for strong interfering signals. A crystal oscillator at 151.5 MHz provides the source of tuning in the first conversion stage. The second conversion and the remaining circuits are similar to the audio channel, except that the detector is d.c. type, providing a trigger output for emergency alarm or takeover, according to the position of thh AUTO/MAN switch. The emergency channel monitor remains on continuously.

### 1.8.6 Specification - Omni-directional Monitoring

| | | |
|---|---|---|
| Monitor Antenna | : | at centre of the DF array, omni-directional pattern |
| Frequency | : | RF input band 117.5 MHz - 136.5 MHz |
| Audio Channel Tuning | : | automatically tuned with the DF System |
| Monitoring Receiver Sensitivity (either channel) | : | NF 7 dB or better |
| Audio Detector | : | Amplitude Modulation (A1) up to 80% |
| Audio Channel Bandwidth | : | 15 kHz at 3 dB points |
| Audio Output | : | 0.5W into 8 Ohms (ext. loudspeaker) with front panel volume control |

| | |
|---|---|
| Aux. Output | : 50 mW at 600 Ohms on the Operator's Control/Display Unit |
| Squelch | : Provided on Receiver Unit |
| AGC | : Provided on Audio Channel |
| Emergency Receiver Tuning | : 125.5 MHz activated by a separate key |
| Emergency Detector | : Carrier presence above threshold, pre-set at the Receiver Unit |
| Emergency Bandwidth | : 15 kHz at the 3 dB points |
| Adjacent Channel Rejection | : 60 dB for interfering signals below 3 mV/m level |
| AGC | : Provided in the Emergency Channel |
| AUTO/MANUAL Control | : At both the Receiver and Operator's Control/Display Units |
| Alarm | : LED indicators at both the Receiver and Operator's Control/Display Units |
| DF Takeover | : Automatic on the appearance of an emergency signal in the AUTO position of the control |

## 1.9 POWER SUPPLY AND INTERCONNECTIONS

### 1.9.1 Power Distribution

The VHF Quasi-Doppler DF System is powered from a single phase AC line of 115V, 60 Hz. Separate 15A 3-pin plugs are provided for the Control/Display Units and a separate plug is used for the main Receiver-Antenna group. The latter is provided with a remote ON/OFF switch located on the front panel of the Operator's Control/Display Unit. In this way, both the Control/Display facilities continue operating without a break, whilst the Receiver/Antenna Group can be switched off when not in use (or while under maintenance).

The individual ControlDisplay Units have their power supplies incorporated in their rack structure in the form of detachable modules, which can be removed after the front panel is lowered.

The main receiver/antenna power supply is assembled on a rear chassis of the Receiver Unit enclosure, mounted on suitable supports to provide air flow for cooling. Its outputs are distributed to two terminal blocks: one for the receiver unit and one for the antenna unit. Power supplies for the antenna are carried over the multicore connecting cable to the Antenna Unit where they are further regulated in a Power Regulator module in order to compensate for the line drop.

All the individual power supply modules are bought-out items, obtained from the standard catalog of Lambda Electronics. They are all of the conventional regulator type. Switching power supplies are ruled out on account of radio interference.

### 1.9.2 Power Supplies for Control/Display Unit

The power supply modules for the Control/Display Units are described in section 2.6.1. They are constructed and wired in a manner providing a 100% safety to maintenance personnel when working on tests or troubleshooting with the front panel open.

### 1.9.3 The Power Supply Assembly of the Receiver/Antenna Group

The main power assembly provides stabilized d.c. power supplies of ±24V, ±15V and +5V. These are used for the receiver and bearing processor modules inside the Receiver Unit and also for the entire operation of the Antenna Unit. There are no 115V ac lines terminating inside the Antenna Unit, thus ensuring complete safety for any maintenance on top of the mast.

Note: Owing to the addition of some overflow breadboards in the back of the Receiver Unit, it has been necessary to add a cooling fan on the rear panel. The fan is not shown on the enclosed diagram as it will not be required after the final re-packaging.

### 1.9.4 Power Regulator for the Antenna Unit

This regulator provides stabilized d.c. power supplies to all the Antenna Unit Modules and to the Antenna Switch Assembly. A detailed description is given in para 2.2.5.

### 1.9.5 Unit Interconnections

The Doppler DF System is separated into equipment in 3 locations:

i The top of the mast mounted antenna array and antenna unit

ii The DF site cabin installed Receiver Unit, and

iii The Operator's Control/Display Unit in the Control Tower

Connections between the Antenna Unit and the Receiver Unit are made with 4 coaxial cables and one multi-core control cable. Two of the coaxial cables, feeding the DF receiver channels, are matched in phase to an accuracy of ±1° at 30 MHz. The coaxial cables are 50 Ohms , 0.5 inch diameter, terminated with N-type connectors at each end. The control cable is made up of twisted pairs of wire, in individual shields, terminating in military style multi-pin connectors, suitable for outdoor use.

The Receiver Unit connects to the Operator's Control/Display by means of a standard 4-wire telephone cable. The connections are made to terminal blocks accessible from the rear of the respective cabinets.

### 1.9.6 Internal Cabling

All the coaxial connections inside the Antenna Unit are of TNC type for ease of handling and reliable contacts in outdoor environment.

In the Receiver Unit, the SMA connectors are adopted as standard. There are no coaxial cables in the Control/Display Unit.

The rear-wiring of all the rack shelves is done by a wire-wrapping method which has been proved reliable in the telephone industry. The exception is power supply bus bars which are intended to carry substantial currents.

### 1.9.7 RFI Protection

In the existing prototype, a quantity of de-coupling capacitors has been added at the module or unit interfaces. This action was necessary to reduce radio frequency interference on the exposed sections of cables to the breadboard extensions. These decoupling elements will be incorporated into the appropriate modules in the future design.

## 2.0 UNIT AND MODULE DESCRIPTIONS

**Index**

2.1 Antenna Array

2.2 Antenna Modules

2.3 Receiver Modules

2.4 Bearing Processor Modules

2.5 Power Supply and Interconnections

2.6 Control and Display Modules

2.7 Audio and Data Transmission

## 2.1 Antenna Array

2.1.1 The DF antenna array comprises 16 vertical dipoles mounted at equal spacings of 22.5° around a circle at the outer points of a 16-arm star of a wire mesh activated ground plane, as shown on the illustration (2.1.3). The ground plane star is further extended by radial counterpoises extending outwards from each dipole base and intended to improve their rejection pattern of horizontal polarization. The ground plane wires are attached to the hub with constant tension springs which take care of maintaining rigidity and accuracy of the structure under varying environmental conditions. Coaxial cables from the dipoles to the Antenna Unit in the lower part of the mast and run along the ground wires in a symmetrical pattern so as to keep down any irregularities of internal reflections.

Each dipole can be exchanged for maintenance purposes by detaching the N-type coaxial connector and removing two screws on the outside of the array ring structure. The dipoles are connected with a set of 16 coaxial cables which are matched in phase at 128 MHz to an accuracy of ±1° electrical. This must be taken into account when replacing any damaged cables.

2.1.2 The configuration of a DF dipole is shown in 2.1.4. The illustration is self explanatory. Dipole replacement may be required in case of damage by lightning. Items most likely to be replaced are the balun transformer and the neon lamp. A visual inspection should be made to ensure that the insulating materials are not damaged by discharge tracks or cracking.

Note: Tests of dipole impedance or the phase matching tests for the dipole connecting cables must be done with the aid of 50 Ohm/75 Ohm impedance transformers.

2.1.3 An omni-directional antenna is mounted at the centre of the array, on top of the supporting mast. It has a form of a round basket which surrounds the base of the lightning conductor rod. The omni-directional antenna is tuned as a quarter-wave monopole to a frequency slightly above the RF band. It serves the purpose of supplying an uninterrupted signal to the audio channel receiver and to the emergency receiver.

## 2.2 ANTENNA MODULES

**Index**

2.2.1 Antenna Switch
2.2.2 Antenna Switch Driver
2.2.3 Scan Logic Control
2.2.4 Test Injection Module
2.2.5 Power Regulator

### 2.2.1 Antenna Switch

#### 2.2.1.1 Switch Assembly

The sixteen dipoles of the antenna array are each connected by a set of phase-matched coaxial cables to the antenna switch. The switch operating sequence is controlled by the 'scan logic' to scan (sample) the outputs of adjacent pairs of dipoles around the array. According to the switching sequence, the two outputs of the switch are routed via two coaxial cables to the two-channel receiver inputs.

The antenna switch is made up of three 'paddle-wheel' switch assemblies which are mounted on the back panel of the Antenna Unit.

Two of the paddle wheel assemblies each contain eight printed circuit board 'coax' switches. These boards are arranged on edge around a centre point like the spokes of a paddle wheel (hence, the name). The third paddle wheel has a similar arrangement of four coax switches. This method of construction reduces the effect of capacitive loading of the 'off' sections and allows for precise phase balance of all the dipole circuit paths.

Effectively, there are two switches in cascade at any time in a signal path, one in an eight-circuit paddle wheel (selecting dipoles 1-8 or 9-16 respectively) and one in the four-circuit paddle wheel, choosing which half of the array is in operation (see block diagram Fig. 1-3). The paddle wheel assemblies are provided with fly-lead connectors to plug into front panel sockets of the switch driver modules, four switches to a module.

TNC coaxial connectors are used for both the input and output r.f. lines.

#### 2.2.1.2 Coax Switch

The 'coax' switch can be compared to a single pole, three way switch, connecting the dipole to channel 1 or channel 2 of the DF receiver or to a dummy load of 75 Ohms. The receiver switching is performed by a pair of T-section PIN diode attenuators and the dummy load is connected by a single on/off PIN diode switch.

Two separate control lines originating in the switch drivers employ the 'soft switching' waveform to select either 'receiver bus 1', 'receiver bus 2' or a dummy load for the r.f. dipole input.

A circuit connection to a 'receiver bus' occurs when one of the 'control line' inputs involves the positive half of the 'soft switching' waveform while the other 'control line' input receives a constant -20 volts. Hence, when both 'control lines' are receiving -20 volts from the switch drivers the r.f. dipole input connects to the dummy load.

Five inductors ensure prevention of r.f. signal loss to the 'control lines'.

When both control line 1 and control line 2 are held -20 volts, D1, D4, D7 and D10 are reversed biased. The r.f. dipole signal is connected through D5 to the dummy load, consisting of two ½ watt, 150 Ohm resistors (forming a 75 Ohm load) and a PNP transistor with associated circuitry to connect D5 to -20 volts (keeping it forward biased). To ensure D4 and D7 stay reverse biased, and give the necessary isolation from the bus lines, D6 is used to clamp the voltage caused by the dc bias from the dummy load to ground potential.

When 'control line 1' is fed with the 'soft switching' waveform from the driver, holding 'control line 2' to -20 volts, the r.f. dipole input will be connected to 'receiver bus 1'. In this case, D1 and D4 are forward biased, D7 and D10 are reversed biased. The 'soft switching' waveform allows D1 and D4 to turn on and off very slowly, reducing the intermodulation products produced by the switching of the dipoles.

When 'control line 2' is fed with the 'soft switching' waveform and 'control line 1' is held -20 volts, the r.f. signal input from the dipole is connected to 'receiver bus 2'. Hence, D7 and D10 are forward biased and D1 and D4 are reversed biased.

The adjustable capacitors C4, C11 and C6 are used as required to change the phase of the input signal, and to match the switch impedance to the input and output cables.

### 2.2.1.3 Specifications

Insertion loss measured at 128 MHz (each paddle wheel):

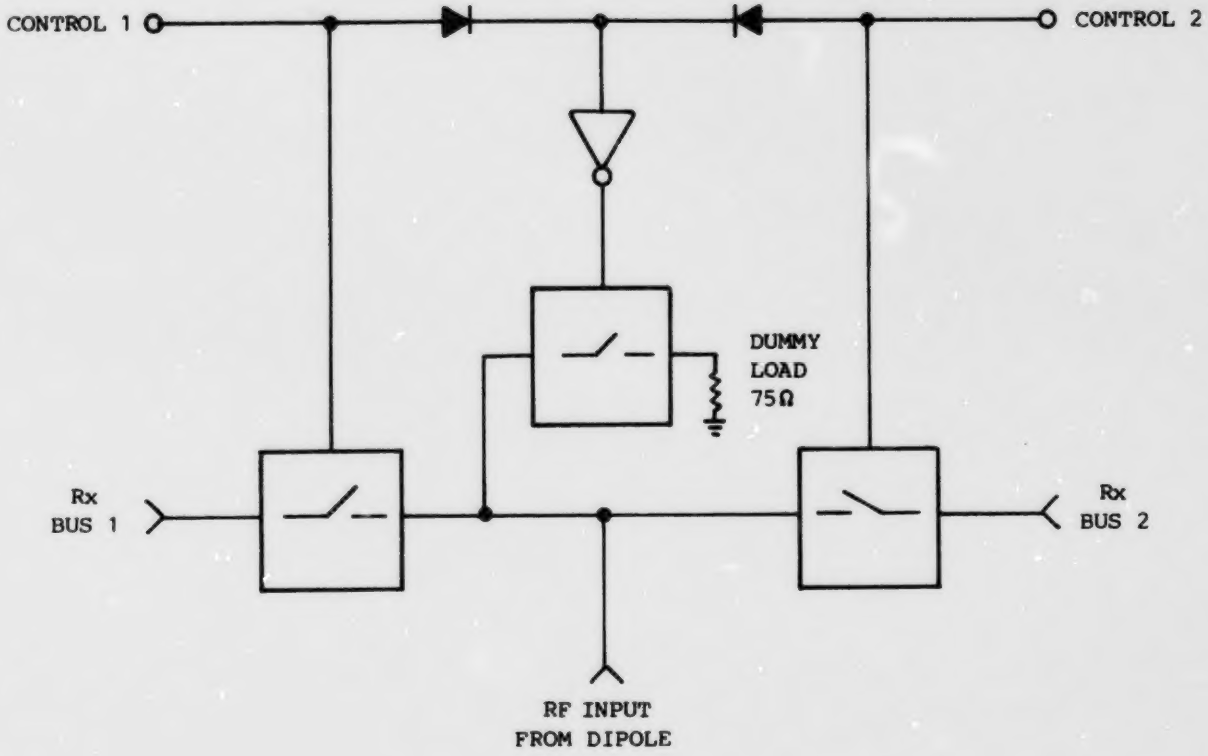
| Control Volts | Insertion Loss |
|---|---|
| -20V | 1 dB |
| +20V | -20 dB |

Impedance, measured at 128 MHz

Dipole input, bus 1 or bus 2 - 75 Ohms

Phase balance - adjust to ±1°

2.2.1.4


CONTROL 1
CONTROL 2
DUMMY
LOAD
75Ω
Rx
BUS 1
Rx
BUS 2
RF INPUT
FROM DIPOLE

TRUTH TABLE:

| CONTROL 1 | CONTROL 2 | DIPOLE TO: |
|---|---|---|
| + | - | Rx Bus 1 |
| - | + | Rx Bus 2 |
| - | - | Dummy Load |

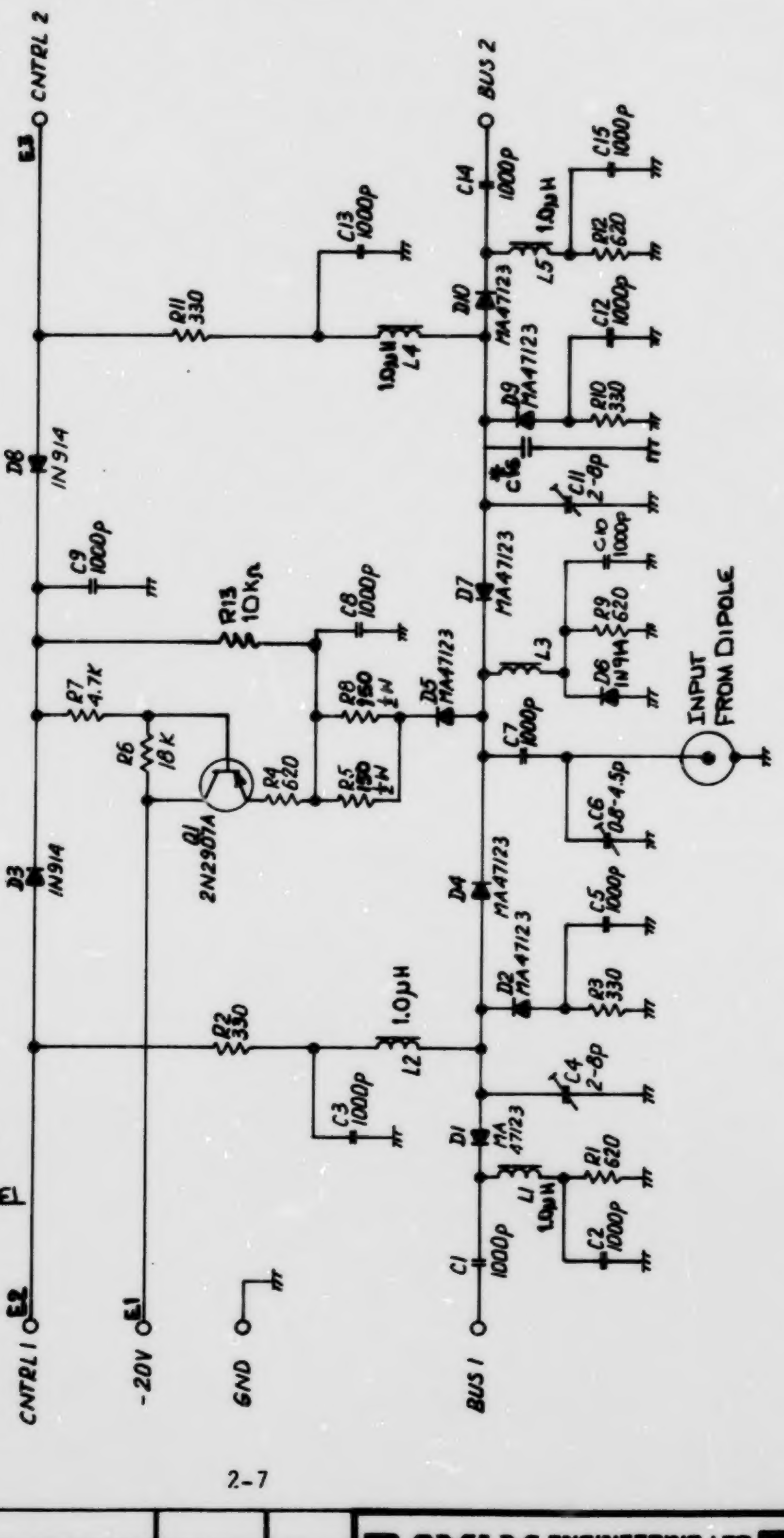
| | | | |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| A | Originated | 83.05.25 | |
| REV. NO. | REVISION | DATE | APPR. BY |

| | | | |
|---|---|---|---|
| DRAWN BY IC | DATE May 25/83 | CHECKED BY | APPR. BY |

**BAYLY** ENGINEERING LTD
a member of

TITLE
COAX SWITCH
BLOCK DIAGRAM

DRAWING NO. 067 0643.026 934 BD-A


CNTRL 2
E3
BUS 2
C14 1000p
C15 1000p
C13 1000p
R11 330
1.0µH L4
D10 MA47123
L5 1.0µH
R12 620
C12 1000p
D9 MA47123
R10 330
C16*
C11 2-8p
D8 IN914
C9 1000p
R13 10KΩ
C8 1000p
D7 MA47123
C10 1000p
R9 620
L3
D6 IN914
R7 4.7K
R8 150 1W
D5 MA47123
R6 18K
Q1 2N2907A
R4 620
R5 150 1W
C7 1000p
C6 0.8-4.5p
INPUT FROM DIPOLE
D3 IN914
D4 MA47123
C5 1000p
D2 MA47123
R3 330
R2 330
1.0µH L2
C4 2-8p
C3 1000p
D1 MA 47123
L1 1.0µH
R1 620
C2 1000p
C1 1000p
E2
E1
CNTRL 1
-20V
GND
BUS 1

NOTE:

1 * C16 MAY BE REQUIRED FOR PHASE MATCHING OF THE TWO RF BUS LINES IN APPLICATIONS WHERE MORE THEN 4 COAX SWITCHES ARE USED IN PARALLEL

| REV NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| 02 | REVISED SEE ECN 02976 | | |

DRAWN BY A. SMITH | DATE NOV. 3.80 | CHECKED BY RG | APPR. BY

BAYLY ENGINEERING LTD
a member of

TITLE SCHEMATIC DIAGRAM
COAX. SWITCH

DRAWING NO. 67-0643.026 934.CD-A 02

### 2.2.1.4 Paddle-Wheel Switch Assembly

### Connectors to Switch Drivers

1. **8-Switch Assembly**

| Switch # | Control 1 (orange wire, term. E2) | P1 Pin # | Control 2 (yellow wire, term. E1) | P2 Pin # |
|---|---|---|---|---|
| 1 | | 19 | | 19 |
| 2 | | 20 | | 20 |
| 3 | | 21 | | 21 |
| 4 | | 22 | | 22 |
| 5 | | ? | | 3 |
| 6 | | 4 | | 4 |
| 7 | | 5 | | 5 |
| 8 | | 6 | | 6 |

2. **4-Switch Assembly**

| Switch # | Control 1 (orange wire, term. E2) | Pin # | Control 2 (yellow wire, term. E1) | Pin # |
|---|---|---|---|---|
| 1 | | 19 | | 3 |
| 2 | | 20 | | 4 |
| 3 | | 21 | | 5 |
| 4 | | 22 | | 6 |

Note: power supply connections

-20V - blue wire
Ground - green wire

## 2.2.1.7 Alignment Procedure

The switch alignment is performed after assembling the coax switch printed circuit boards onto the paddle wheel assembly.

**Test Equipment**

- DC dual regulated power supply set to +20V and -20V
- Network analyzer set to measure return loss at 128 MHz using a 50 Ohm/75 Ohm transformer

**Procedure A**

- Connect all control lines of the coax switches to -20V dc
- terminate bus 1 and bus 2 into 75 Ohms
- Connect network analyzer to the input of the coax switch and set trimmer C6 for minimum return loss
- Repeat for the remaining switches

**Procedure B**

- Terminate all switch inputs to 75 Ohms
- Terminate bus 2 to 75 Ohms
- Connect network analyzer to bus 1
- Turn the first coax switch ON to bus 1 by connecting its control line 1 to +20V and control line 2 to -20V
- Turn all the remaining switches to dummy loads by connecting their control lines 1 and 2 to -20V
- Set trimmer C4 for minimum return loss
- Repeat for the remaining switches

**Procedure C**

- Proceed as in B, except that the network analyzer is connected to bus 1, and bus 2 is terminated in 75 Ohms
- Adjust trimmers C11 for minimum return loss

### 2.2.2 ANTENNA SWITCH DRIVER

Five 'Antenna Switch Drivers' are located in the Antenna Unit of the Doppler Radio Direction Finder.

The antenna switch drivers are used in unanimity with the scan logic control to select the coax switch configuration required at each sampling time of the Doppler DF System. The logic necessary for this selection is provided by the scan logic control.

The drivers also provide amplification of the 'soft switching' waveform developed by the scan logic control circuit.

The circuit consists of eight separate 741 operational amplifiers, each followed by a current amplification stage.

A 'control line', originating in the scan logic control circuit predetermines whether the drivers are to generate an amplified version of the 'soft switching' waveform or to output a constant -20 volt level.

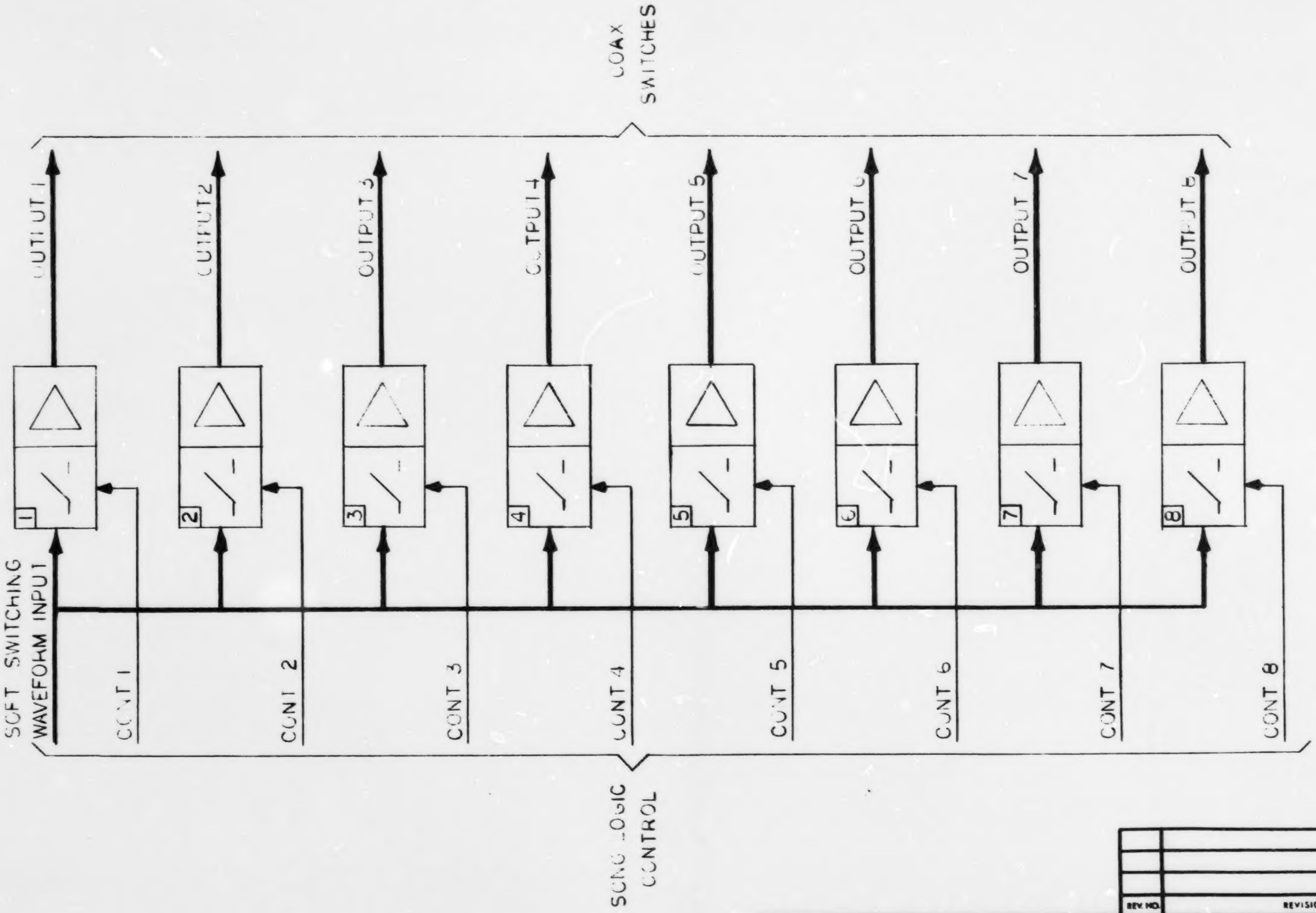
Each of the eight amplifiers are operationally identical. For the sake of simplification, the operation of only one operational amplifier is summarized.

The 'control line' (CNTRL 1) from the scan logic control normally at + 20 volts, is connected through a current limiting resistor to the inverting input of the operational amplifier.

The 'soft switching' waveform also originating in the scan logic control circuit is connected to the non-inverting input of the operational amplifier. With the control line at + 20 V, the output of the operational amplifier is clamped to the -20 volts rail.

The resulting output of the op-amp is fed into the current amplification stage, consisting of a class A-B amplifier, utilizing a pair of complementary transistors. The output of this stage is also clamped to -20 volts and is fed to the coax switch.

When the 'control line' drops to zero volts, meaning that the amplifier/switch combination has been selected by the scan logic control circuit, the op-amp acts as a non-inverting amplifier. The 'soft switching' waveform is amplified and fed into the current amplification stage; the current is then boosted to approximately 25 mA and sent to the coax switch.


COAX SWITCHES
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
OUTPUT 5
OUTPUT 6
OUTPUT 7
OUTPUT 8
1
2
3
4
5
6
7
8
SOFT SWITCHING WAVEFORM INPUT
CONT 1
CONT 2
CONT 3
CONT 4
CONT 5
CONT 6
CONT 7
CONT 8
SONG LOGIC CONTROL

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|

**BAYLY** ENGINEERING LTD a member of

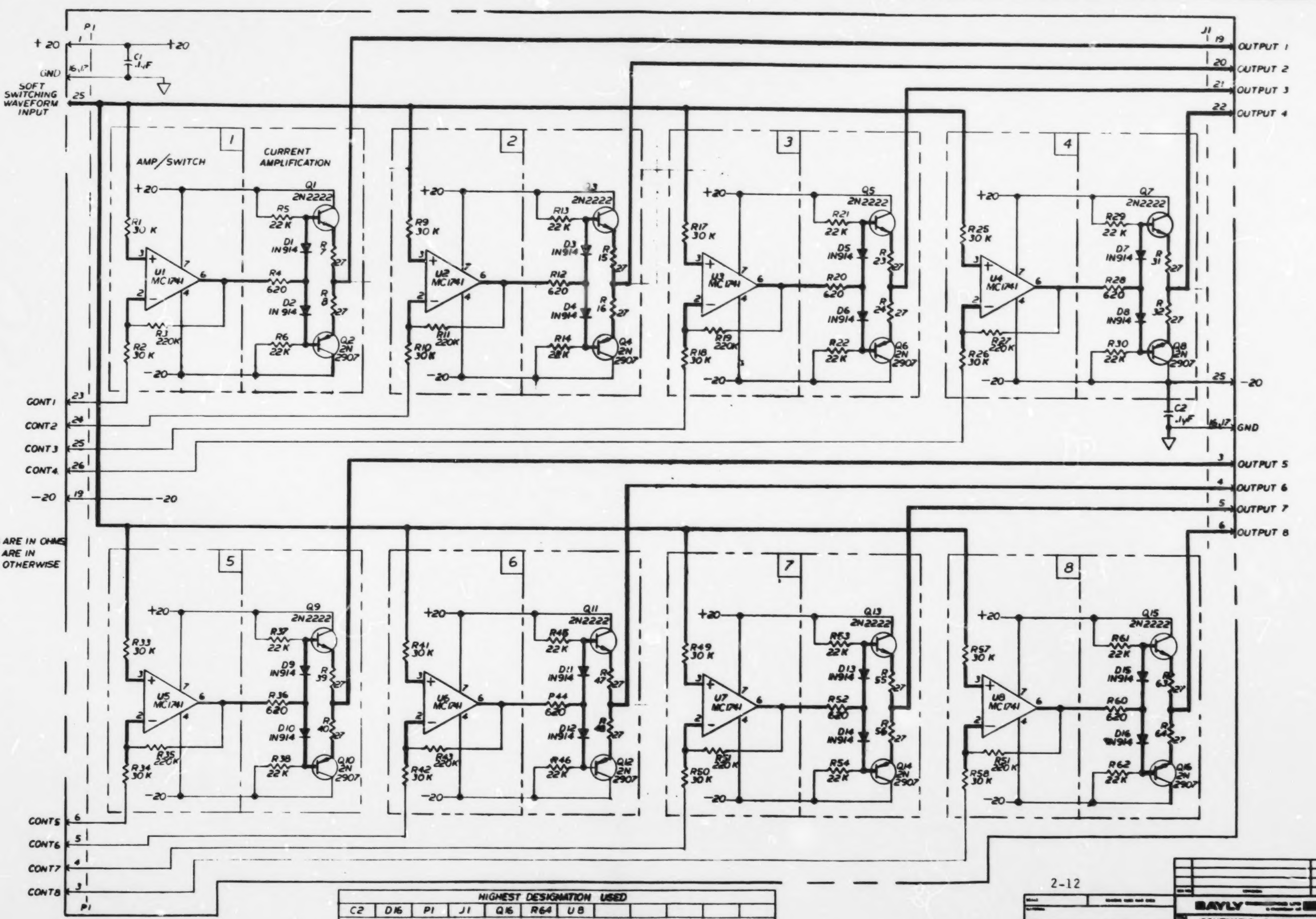
TITLE BLOCK DIAGRAM
SWITCH DRIVER

SCALE
REMOVE BURR MAX 010R
MATERIAL
FINISH

UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMALS ± ANGLES ± °

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| L.T. | 83-01-25 | L.A. |  | 67-0643.026 866.BD-B |

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.


+20
GND
SOFT SWITCHING WAVEFORM INPUT
P1
C1 .1μF
J1
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
OUTPUT 5
OUTPUT 6
OUTPUT 7
OUTPUT 8
CONT1
CONT2
CONT3
CONT4
CONT5
CONT6
CONT7
CONT8
−20
C2 .1μF
AMP/SWITCH
CURRENT AMPLIFICATION
1
2
3
4
5
6
7
8
U1 MC1741
U2 MC1741
U3 MC1741
U4 MC1741
U5 MC1741
U6 MC1741
U7 MC1741
U8 MC1741
Q1 2N2222
Q2 2N2907
Q3 2N2222
Q4 2N2907
Q5 2N2222
Q6 2N2907
Q7 2N2222
Q8 2N2907
Q9 2N2222
Q10 2N2907
Q11 2N2222
Q12 2N2907
Q13 2N2222
Q14 2N2907
Q15 2N2222
Q16 2N2907
R1 30 K
R2 30 K
R3 220K
R4 620
R5 22K
R6 22K
R7 27
R8 27
D1 IN914
D2 IN914
R9 30 K
R10 30K
R11 220K
R12 620
R13 22K
R14 22K
R15 27
R16 27
D3 IN914
D4 IN914
R17 30 K
R18 30K
R19 220K
R20 620
R21 22K
R22 22K
R23 27
R24 27
D5 IN914
D6 IN914
R25 30 K
R26 30K
R27 220K
R28 620
R29 22K
R30 22K
R31 27
R32 27
D7 IN914
D8 IN914
R33 30 K
R34 30K
R35 220K
R36 620
R37 22K
R38 22K
R39 27
R40 27
D9 IN914
D10 IN914
R41 30 K
R42 30K
R43 220K
R44 620
R45 22K
R46 22K
R47 27
R48 27
D11 IN914
D12 IN914
R49 30 K
R50 30K
R51 220K
R52 620
R53 22K
R54 22K
R55 27
R56 27
D13 IN914
D14 IN914
R57 30 K
R58 30K
R59 220K
R60 620
R61 22K
R62 22K
R63 27
R64 27
D15 IN914
D16 IN914

NOTES:
1- ALL RESISTOR VALUES ARE IN OHMS
2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

| HIGHEST DESIGNATION USED | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C2 | D16 | P1 | J1 | Q16 | R64 | U8 | | | | | |
| DESIGNATION NOT USED | | | | | | | | | | | |
| | | | | | | | | | | | |

BAYLY

SCHEMATIC DIAGRAM
SWITCH DRIVER

67-0643.026.866.CD -D

### 2.2.2.3 TEST

a Connect a ± 20V power supply.

b Connect a sinewave generator, at input line, adjusted at 1.6 KHz, 10 V P-P.

c Connect a load resistor to get 25 mA at 20V at the ouput of a driver. (800 Ω , 1W)

d With control at + 20V, the output is at -20 V.

e With control at GND, a sinewave is present at the output.

f Repeat c, d and e for each driver.

## 2.2.3 SCAN LOGIC CONTROL

The 'Scan Logic Control Card' is located in the Antenna Unit of the Doppler Radio Direction Finder.

The 'Scan Logic Control Card' is used to generate the control signals necessary to select the dipole configuration at each sampling time.

The circuit also produces the 'soft switching' waveform employed in the 'Coax Switches' and the 'Antenna Switch Drivers'.

The card consists of four memory circuits, two programmable synchronous count down couters, a reset circuit, a line driver, a plus and minus 12 volts voltage regulators and a 'soft switching' waveform generator.

The clock signals originating in the 'Timing Board' are received through a 75 ohm twisted line pair. The signals are then amplified to TTL levels. The output is supplied to control the logic circuitry and generate the basis for the 'soft switching' waveform.

By employing two operational amplifiers, a current amplification stage and a diode waveshaping network, along with the 'Timing Board' clock signal, a 'soft switching' waveform is generated. The first operational amplifier, used as an integrator, produces a symetrical triangle waveform from the TTL level clock signal. The triangle waveform is transmitted to a clipping amplifier, which flattens both the positive and negative waveform tips. This clipped waveform is then sent into the current amplification stage, consisting of a pair of complementary transistors, which act as a class A-B amplifier to boost the current and drive the low impedance 'diode waveshaper'. The 'diode waveshaper' reduces the slope of the clipped waveform as it crosses the zero axis by using breakpoints formed by the 'diode waveshaper' diodes and resistors. This, completes the 'soft switching" waveform cycle; it is now ready to be sent to the 'Switch Drivers'.

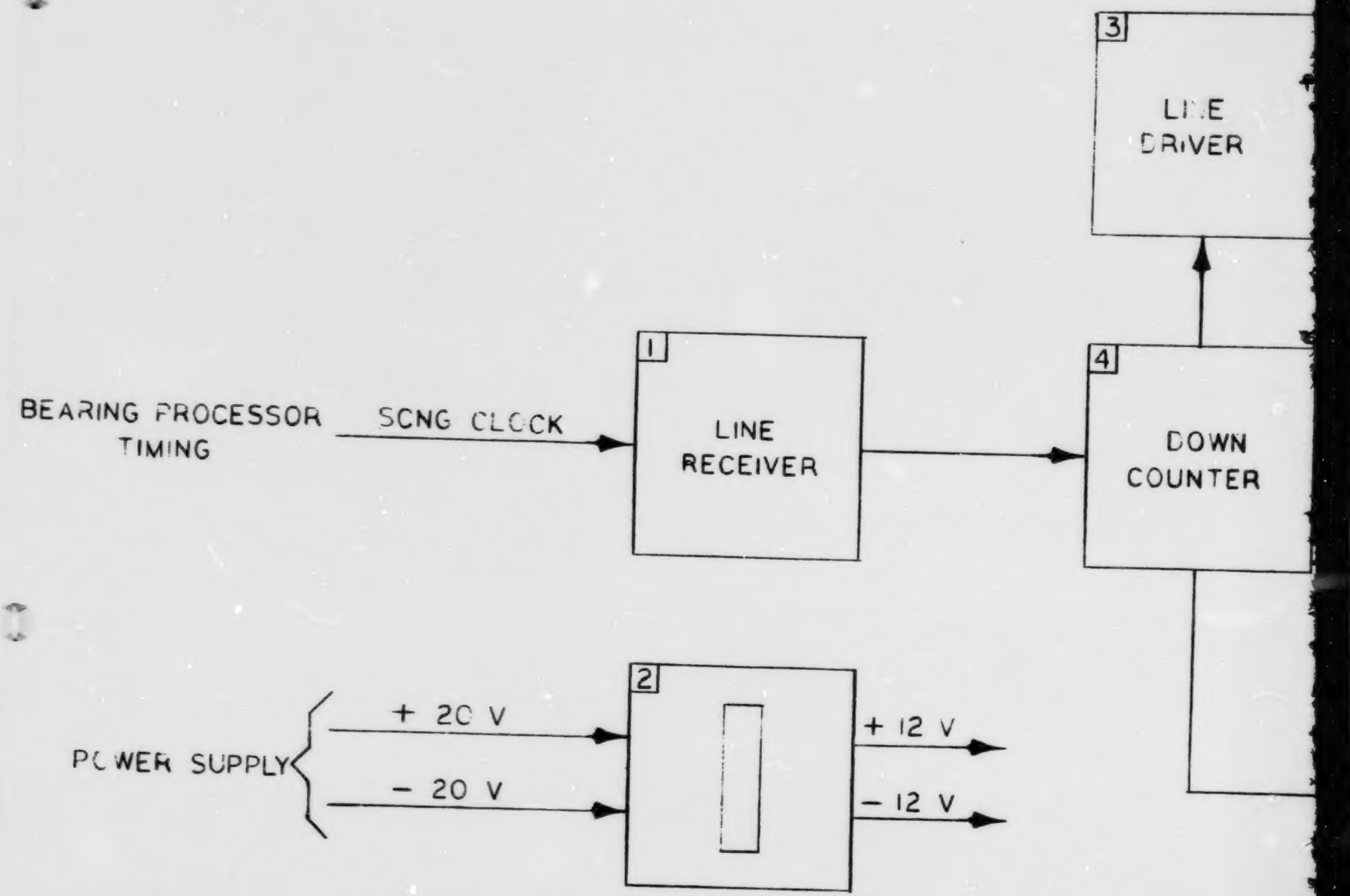
The logic circuitry consists of two programmable synchronous count down counters, four bipolar memories and a reset circuit. The couters, are used to generate the addresses for the PROM . They begin their initial count down to zero at 31 for the 16 dipole system with each 'Timing Board' clock pulse. When the counters reach zero, a ripple clock pulse is generated to the reset circuit from each counter. The reset circuit, in turn, produces a pulse which returns to the counters, loading them again to 31 and starting the count down back to zero. Note that each dipole pair is selected for two clock cycles.

When the counters reach zero, they produce a second pulse called the North Pulse indicating one complete count down cycle (beginning with the North dipole selected). This 'North' pulse is sent to the 'Timing Board' through a low level differential 'Line Driver'.

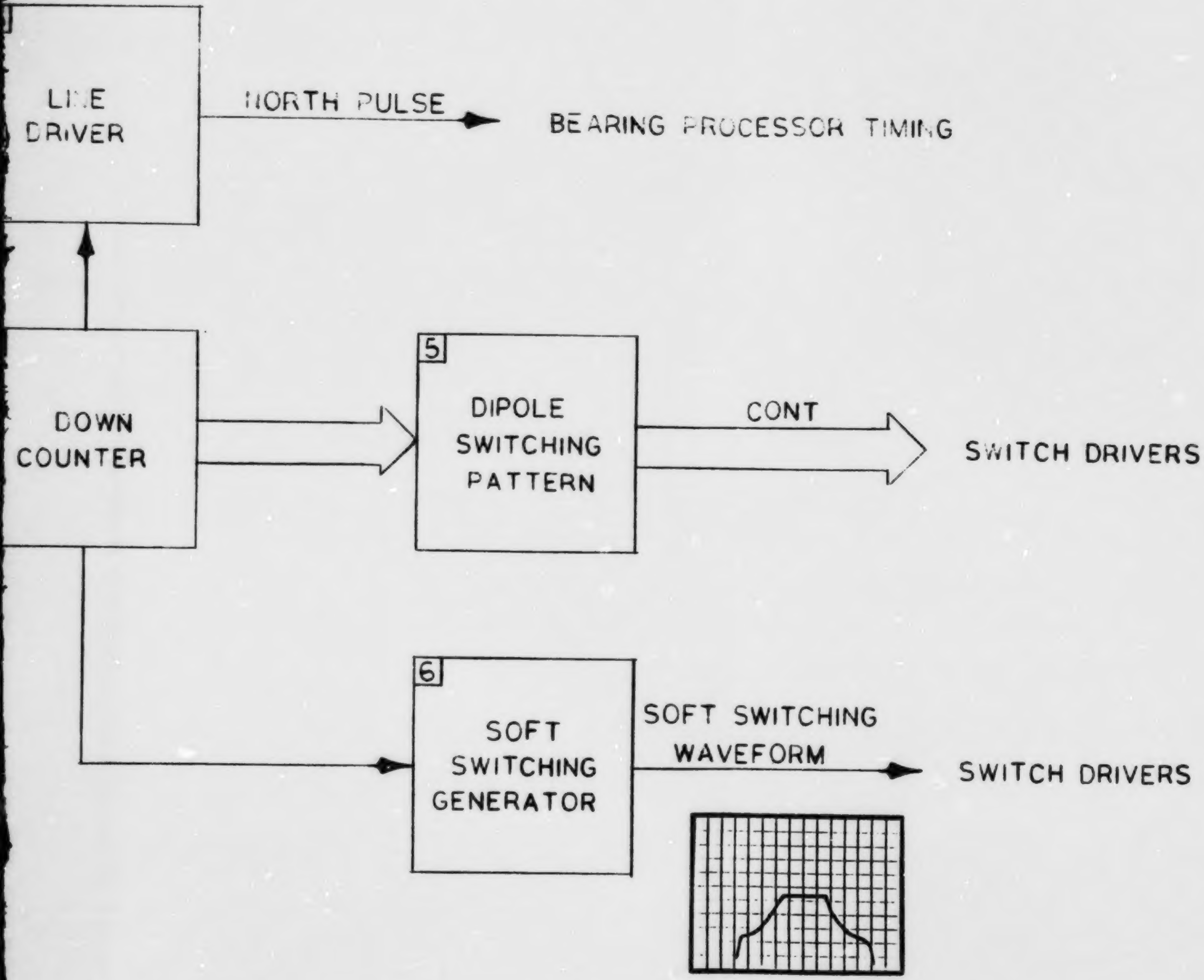
The 'Line Driver' is an integrated circuit, containing four matched NPN transistors, of which three are being used. The first transistor (Q3) is used to develop a 100mV pulse from the TTL level 'North' pulse it receives. The second transistor (Q4), inverts the same 'North' pulse and feeds it to the third transistor (Q5) which develops an inverted 100 mV pulse and sends this signal down one side of the line. The other side of the line carries the pulse generated by Q3. Both signals are very low in amplitude separately, but the combined differential is 200 mV at the pulse, which is enough to be recovered by a differential line receiver.

The output of the 'counters' are fed to the address lines of the four bipolar memory (PROM), containing the dipole switching pattern. There are 16 dipole switches split into two categories, — one being two '8-way paddle wheel switches' and the other being one '4-way paddle wheel switch'. The memory integrated circuits, U1 and U2, contain the switching patterns for each of the '8-way paddle wheel switches', while the memories, U3 and U4, contain the switching patterns for the '4-way paddle wheel switch'. The memory outputs are open collectors, each being pulled up to + 20 volts by a 10K resistor and then fed to the 'Switch Drivers'.

Two voltage regulators (+ 12 volts and -12 volts respectively) are incorporated and produce power for the 'soft switching' generation stages. The 'voltage regulators' also produce the + 12 volt voltage output used as the power source for the 'Test Injection' circuit.


3
LINE DRIVER
1
LINE RECEIVER
4
DOWN COUNTER
BEARING PROCESSOR TIMING
SCNG CLOCK
2
POWER SUPPLY
+ 20 V
- 20 V
+ 12 V
- 12 V

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.


LINE DRIVER
NORTH PULSE
BEARING PROCESSOR TIMING
DOWN COUNTER
5
DIPOLE SWITCHING PATTERN
CONT
SWITCH DRIVERS
6
SOFT SWITCHING GENERATOR
SOFT SWITCHING WAVEFORM
SWITCH DRIVERS

| REV NO | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE
REMOVE BURR MAX 010R
MATERIAL
FINISH

**BAYLY** ENGINEERING LTD
a member of

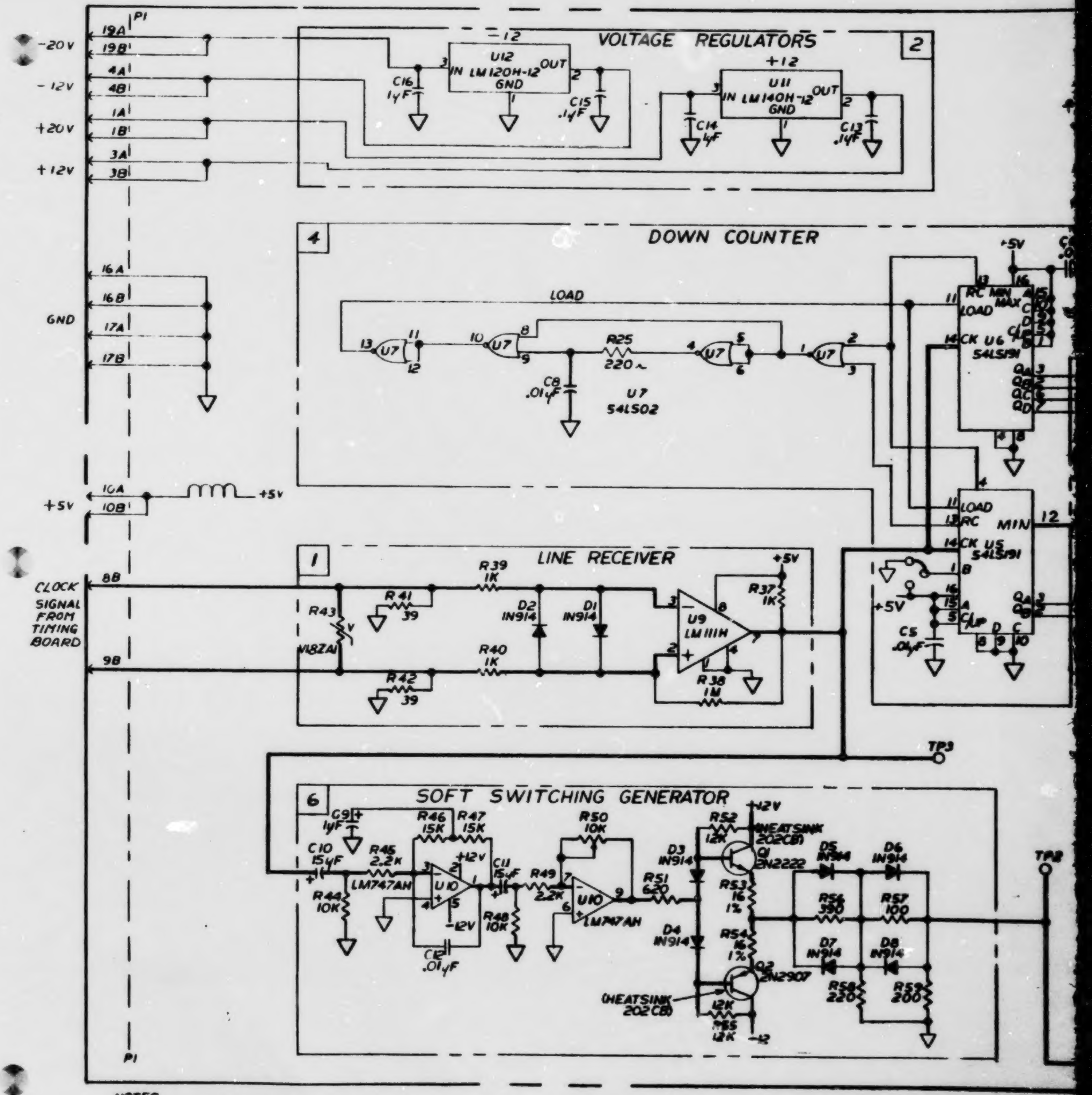
TITLE
BLOCK DIAGRAM
SCNG LOGIC CONTROL

consent of
, this document may be
r otherwise dealt with,

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| L.T. | 83-01-26 | LA | | 66-0643.027 312.BD-B |

Without prior written consent of
..Y ENGINEERING LIMITED, this document may be
..t sold, copied, reproduced or otherwise dealt with
..contents communicated to others.

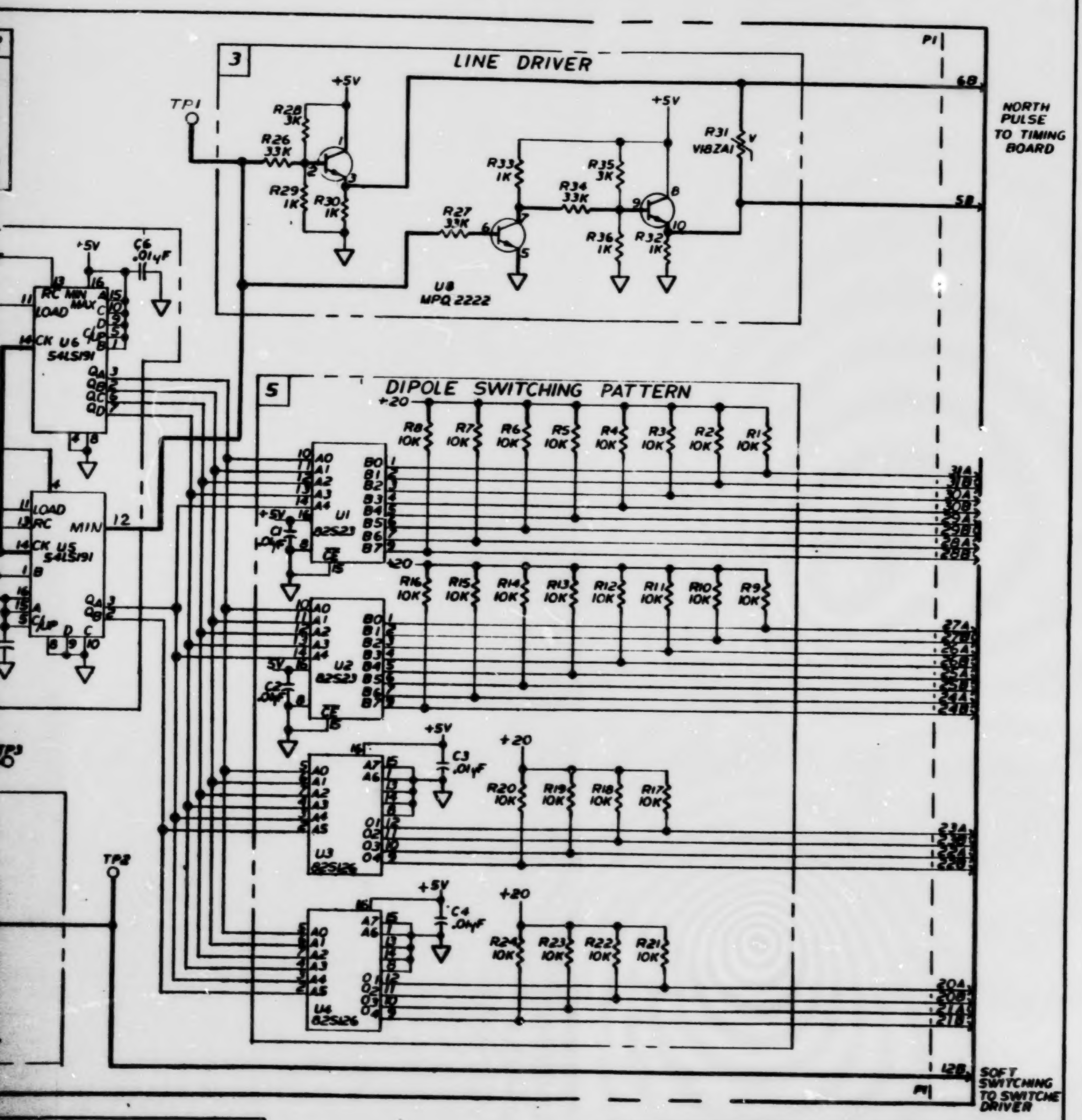

P1
-20v
19A
19B
-12v
4A
4B
+20v
1A
1B
+12v
3A
3B
VOLTAGE REGULATORS
2
-12
U12
IN LM120H-12 OUT
GND
C16
1μF
C15
.1μF
+12
U11
IN LM140H-12 OUT
GND
C14
1μF
C13
.1μF
4
DOWN COUNTER
GND
16A
16B
17A
17B
LOAD
U7
R25
220 Ω
C8
.01μF
U7
54LS02
+5V
RC MIN
MAX
LOAD
CK U6
54LS191
QA
QB
QC
QD
+5v
10A
10B
+5v
LOAD
RC
MIN
CK U5
54LS191
B
A
C/D
UP
D
C
C5
.01μF
1
LINE RECEIVER
CLOCK SIGNAL FROM TIMING BOARD
8B
9B
R43
V18ZA1
R41
39
R42
39
R39
1K
R40
1K
D2
1N914
D1
1N914
U9
LM111H
R37
1K
R38
1M
+5V
TP3
6
SOFT SWITCHING GENERATOR
C9
1μF
C10
15μF
R45
2.2K
R44
10K
LM747AH
U10
R46
15K
R47
15K
+12v
-12V
C12
.01μF
C11
15μF
R49
2.2K
R48
10K
R50
10K
U10
LM747AH
R51
620
D3
1N914
D4
1N914
+12V
R52
12K
HEATSINK
202CB)
Q1
2N2222
R53
16
1%
R54
16
1%
Q2
2N2907
(HEATSINK
202CB)
12K
R55
12K
-12
D5
1N914
D6
1N914
R56
390
R57
100
D7
1N914
D8
1N914
R58
220
R59
200
TP2

NOTES

1-ALL RESISTOR VALUES ARE IN OHMS

2-ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

| HIGHEST DESIGNATION USED | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| R61 | C16 | D8 | Q2 | U12 | P1 | | | | |
| DESIGNATION NOT USED | | | | | | | | | |
| | | | | | | | | | |


3
LINE DRIVER
TP1
+5V
R28 3K
R26 33K
R29 1K
R30 1K
R31 V V18ZA1
R33 1K
R35 3K
R34 33K
R27 33K
R36 1K
R32 1K
U8 MPQ 2222
P1
6B
5B
NORTH PULSE TO TIMING BOARD
C6 .01μF
RC MIN MAX
LOAD
CK U6 54LS191
CK U5 54LS191
QA QB QC QD
5
DIPOLE SWITCHING PATTERN
+20
R8 10K
R7 10K
R6 10K
R5 10K
R4 10K
R3 10K
R2 10K
R1 10K
U1 82S23
C1 .01μF
R16 10K
R15 10K
R14 10K
R13 10K
R12 10K
R11 10K
R10 10K
R9 10K
U2 82S23
C2 .01μF
U3 82S126
C3 .01μF
R20 10K
R19 10K
R18 10K
R17 10K
U4 82S126
C4 .01μF
R24 10K
R23 10K
R22 10K
R21 10K
31A 31B 30A 30B 29A 29B 28A 28B
27A 27B 26A 26B 25A 25B 24A 24B
23A 23B 22A 22B
20A 20B 21A 21B
TP2
TP3
12B
SOFT SWITCHING TO SWITCHE DRIVER

USED

BAYLY

SCAN LOGIC CONTROL

66-0643.027 312.CD D

## SCAN LOGIC CONTROL : PROM LISTING

| | | Data | | | |
|---|---|---|---|---|---|
| | Address | U1 | U2 | U3 | U4 |
| (31) | IF | FE | FD | D | E |
| | IE | FE | FD | D | E |
| | ID | FD | FB | D | E |
| | IC | FD | FB | D | E |
| | IB | FB | F7 | D | E |
| | 1A | FB | F7 | D | E |
| | 19 | F7 | EF | D | E |
| | 18 | F7 | EF | D | E |
| | 17 | EF | DF | D | E |
| | 16 | EF | DF | D | E |
| | 15 | DF | BF | D | E |
| | 14 | DF | BF | D | E |
| | 13 | BF | 7F | D | E |
| | 12 | BF | 7F | D | E |
| | 11 | 7F | FE | D | 7 |
| | 10 | 7F | FE | D | 7 |
| | 0F | FE | FD | B | 7 |
| | 0E | FE | FD | B | 7 |
| | 0D | FD | FB | B | 7 |
| | 0C | FD | FB | B | 7 |
| | 0B | FB | F7 | B | 7 |
| | 0A | FB | F7 | B | 7 |
| | 09 | F7 | EF | B | 7 |
| | 08 | F7 | EF | B | 7 |
| | 07 | EF | DF | B | 7 |
| | 06 | EF | DF | B | 7 |
| | 05 | DF | BF | B | 7 |
| | 04 | DF | BF | B | 7 |
| | 03 | BF | 7F | B | 7 |
| | 02 | BF | 7F | B | 7 |
| | 01 | 7F | FE | B | E |
| | 00 | 7F | FE | B | E |

### 2.2.3.3 TEST

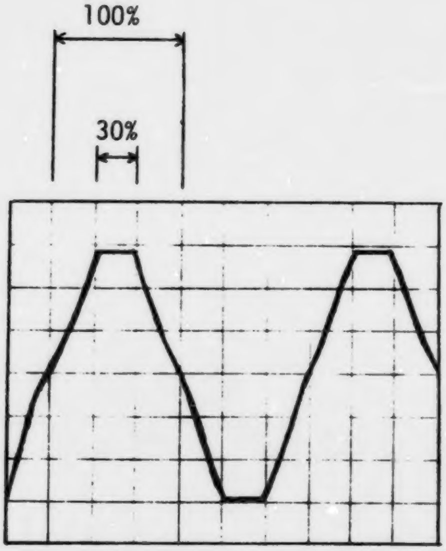
a Connect a + 20V, - 20V and + 5V power supplies.

b Check that + 12V is present at V11-2 and -12V at U12-2.

c Connect a sinewave generator, at scan clock input, adjusted at 1.6 KHz, 200 mV P-P. Check that a square wave (0-5V) is present at TP3.

d Check that counters count from 31 to 0 and that a north pulse is outputted at count 16 and 0. This pulse should be 200 mV P-P.

e Adjust R50 to get an approximate 30% flat portion of the waveform as shown on the following figure.



### 2.2.4 TEST INJECTION MODULE

TO BE SUPPLIED

## 2.2.5 Power Regulator

The Power Regulator is used in the Antenna Unit to reduce the voltages sent up from the main power supplies to the levels needed by the circuits in the antenna unit. This helps to compensate for any losses in voltage on the long cables from the power supplies to the antenna unit.

Three regulators are mounted on a single card:

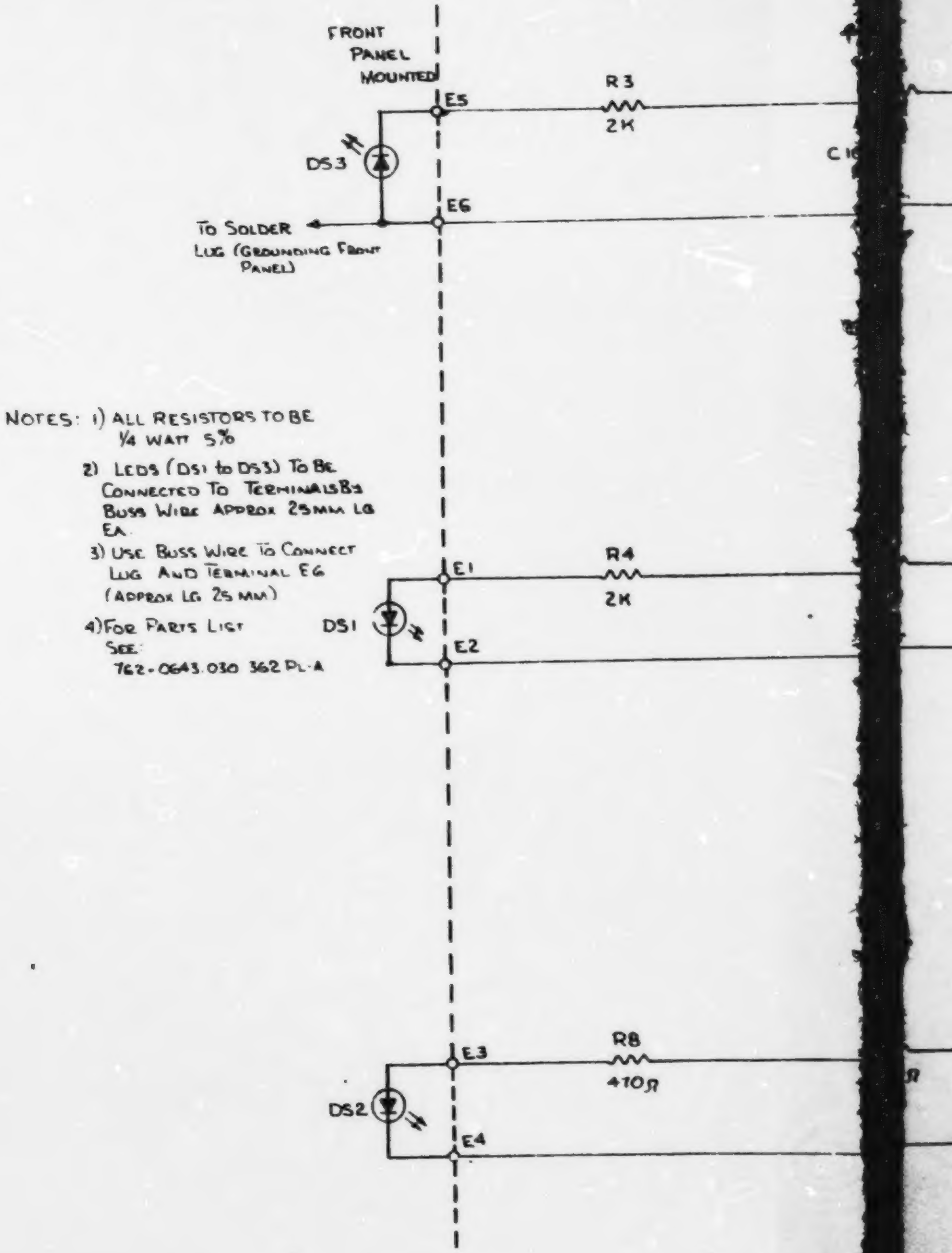
(a) D1 is a +5V 3-terminal regulator, fed from the +15V supply. DS2 is a green, front panel mounted status indicator for this section.

(b) D2 is an adjustable, positive output regulator which is set for 20V output using R2. DS1 is a green, front panel mounted status indicator for this section.

(c) D3 is an adjustable, negative output regulator, which is set for - 20V output using R1. DS3 is a green, front panel mounted status indicator for this section.

All three regulators are mounted on individual heatsinks for adequate heat dissipation.

| NAME | BOARD PIN # | COMPONENT PIN # |
|---|---|---|
| -24V | 12 A | D3-4 |
| -24V | 13 A | D3-4 |
| +24V | 3 A | D2-1 |
| +24V | 4 A | D2-1 |
| +15V | 8 A | D1-1 |
| +15V | 9 A | D1-1 |
| -20V | 19 A | D3-3 |
| -20V | 20 A | D3-3 |
| +20V | 1 A | D2-2 |
| +20V | 2 A | D2-2 |
| + 5V | 10 A | D1-2 |
| + 5V | 11 A | D1-2 |


FRONT
PANEL
MOUNTED
E5
R3
2K
DS3
C1
E6
To Solder
Lug (Grounding Front
Panel)
E1
R4
2K
DS1
E2
E3
R8
410Ω
DS2
E4

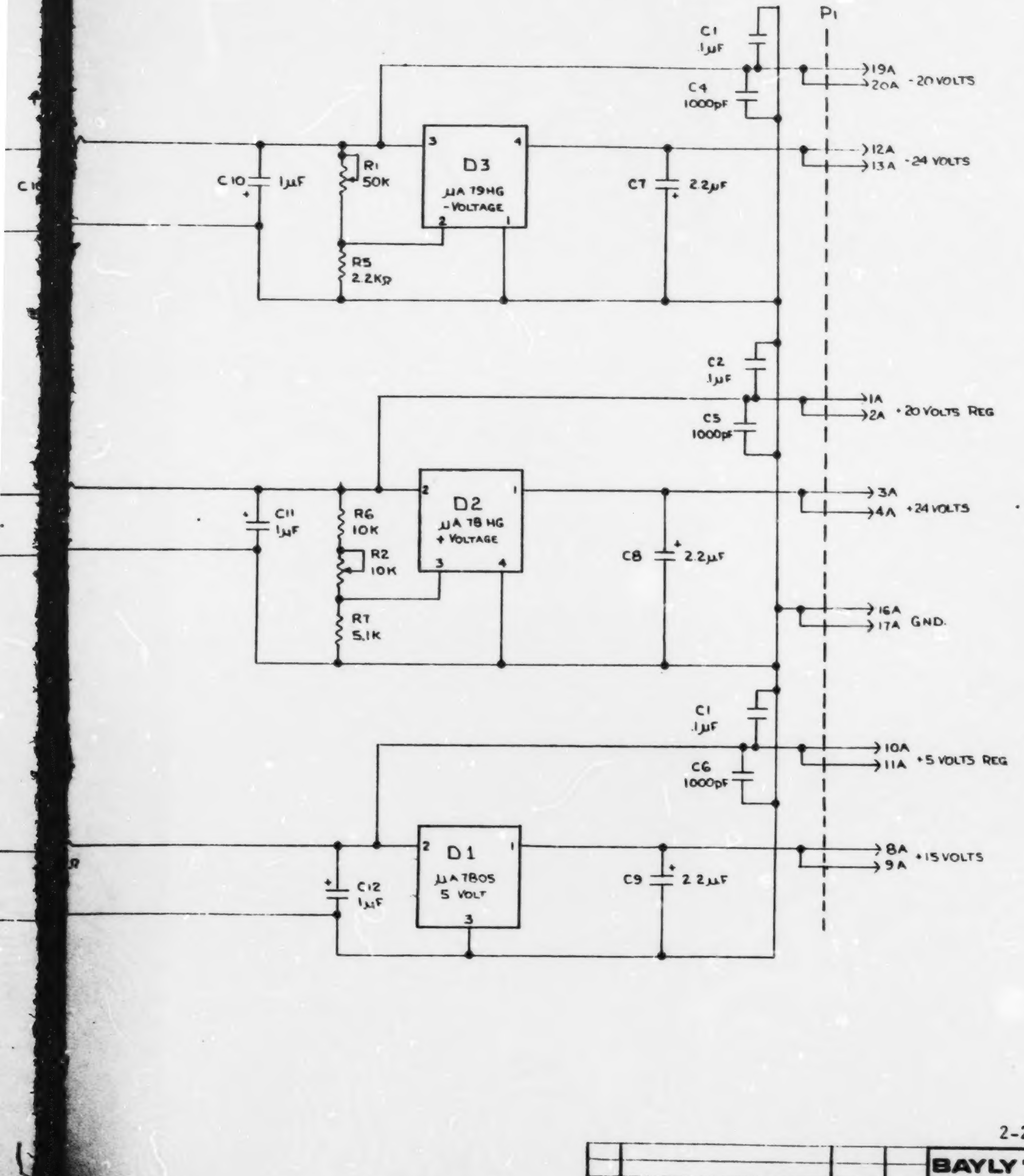
NOTES: 1) ALL RESISTORS TO BE
1/4 WATT 5%

2) LEDS (DS1 to DS3) To Be
Connected To Terminals By
Buss Wire Approx 25MM LG
EA.

3) Use Buss Wire To Connect
Lug And Terminal E6
(Approx LG 25 MM)

4) For Parts List
See:
762-0643.030 362 PL-A

762-0643.030 362 CDC



P1
C1 .1µF
C4 1000pF
19A
20A -20 VOLTS
12A
13A -24 VOLTS
C10 1µF
R1 50K
D3 µA 79HG -VOLTAGE
3
4
2
1
C7 2.2µF
R5 2.2KΩ
C2 .1µF
C5 1000pF
1A
2A +20 VOLTS REG
3A
4A +24 VOLTS
C11 1µF
R6 10K
R2 10K
R7 5.1K
D2 µA 78 HG + VOLTAGE
2
1
3
4
C8 2.2µF
16A
17A GND.
C1 .1µF
C6 1000pF
10A
11A +5 VOLTS REG
8A
9A +15 VOLTS
C12 1µF
D1 µA 7805 5 VOLT
2
1
3
C9 2.2µF

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

BAYLY ENGINEERING LTD a member of AEC

SCHEMATIC DIAGRAM
POWER REGULATOR

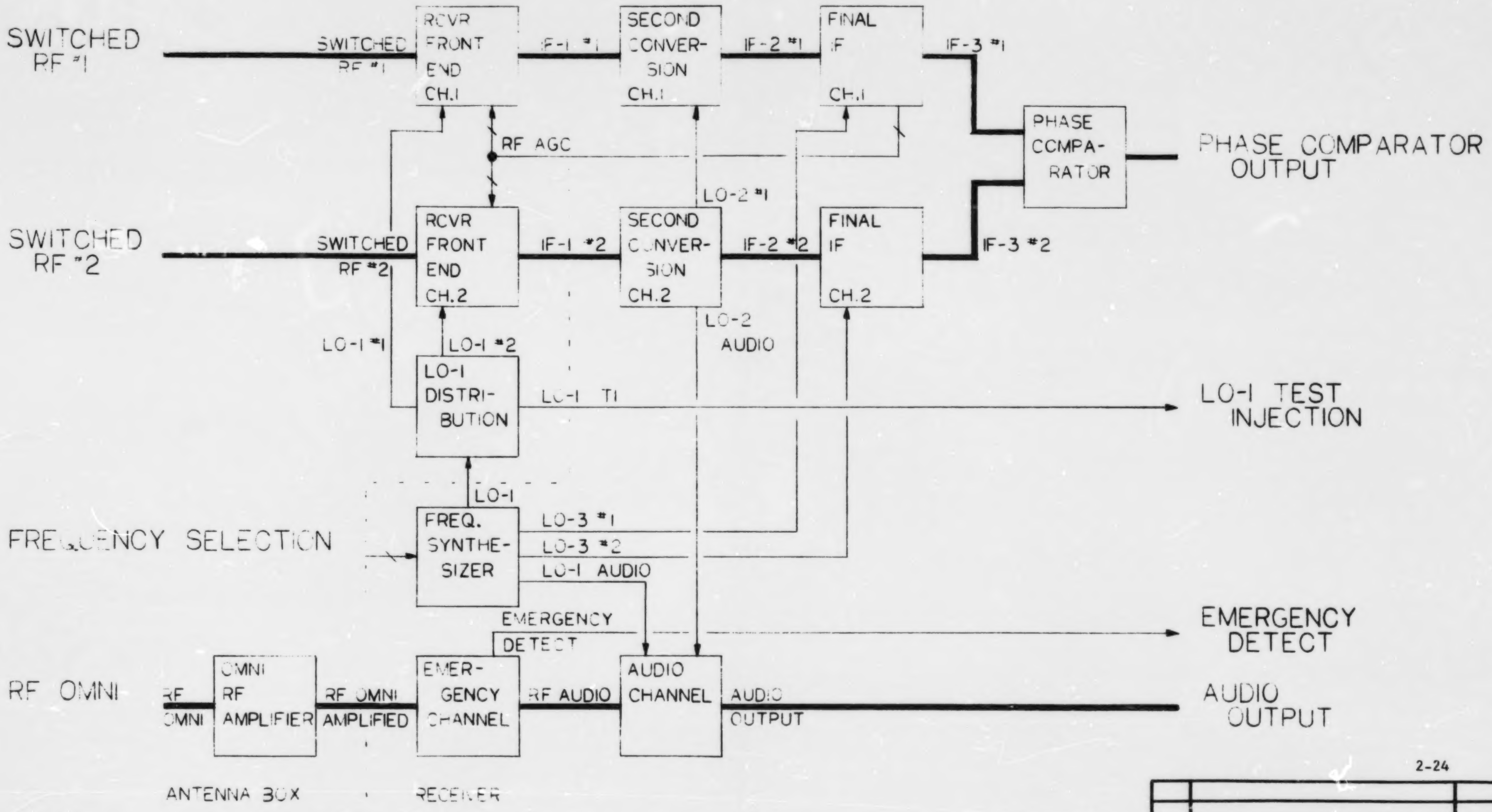
D SCOTT
1 SEPT 81
RV

DWG NO 762-0643.030 362 CD-C
01

## 2.3 RECEIVER MODULES

**Index**

2.3.1 DF Receiver Front End (Channel 1 and 2)
2.3.2 Omni RF Amplifier
2.3.3 LO-1 Distribution
2.3.4 Second Conversion - DF Channel 1
2.3.5 Second Conversion - DF Channel 2
2.3.6 Final IF - Channel 1
2.3.7 Final IF - Channel 2
2.3.8 Phase Comparator
2.3.9 Frequency Synthesizer
2.3.10 Audio Channel
2.3.11 Emergency Channel


SWITCHED RF #1
SWITCHED RF #1
RCVR FRONT END CH.1
IF-1 #1
SECOND CONVERSION CH.1
IF-2 #1
FINAL IF CH.1
IF-3 #1
RF AGC
PHASE COMPARATOR
PHASE COMPARATOR OUTPUT
LO-2 #1
SWITCHED RF #2
SWITCHED RF #2
RCVR FRONT END CH.2
IF-1 #2
SECOND CONVERSION CH.2
IF-2 #2
FINAL IF CH.2
IF-3 #2
LO-1 #1
LO-1 #2
LO-2 AUDIO
LO-1 DISTRIBUTION
LO-1 TI
LO-1 TEST INJECTION
LO-1
FREQUENCY SELECTION
FREQ. SYNTHESIZER
LO-3 #1
LO-3 #2
LO-1 AUDIO
EMERGENCY DETECT
EMERGENCY DETECT
RF OMNI
RF OMNI
OMNI RF AMPLIFIER
RF OMNI AMPLIFIED
EMERGENCY CHANNEL
RF AUDIO
AUDIO CHANNEL
AUDIO OUTPUT
AUDIO OUTPUT
ANTENNA BOX
RECEIVER

| REV NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

UNLESS OTHERWISE SPECIFIED
TOLERANCES DECIMALS ± ANGLES ± °

DRAWN BY S. B.
DATE 83-1-19
CHECKED BY
APPROVED BY

**BAYLY** ENGINEERING LTD a member of

TITLE BLOCK DIAGRAM RECEIVER MODULES

DRAWING NO. 66-0643.035 335.BD-B

## 2.3.1 DF RECEIVER FRONT END

a This module is located in the antenna box.

b Its main functions are :

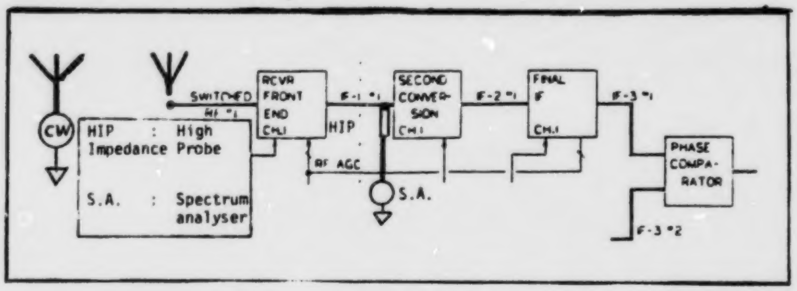
1. To convert the tuned frequency to 30 MHz.
2. To decrease the band-pass to 800 KHz.
3. To amplify the signal.

c On the block diagram, we illustrate the form of the signal at the module output as seen on the spectrum analyser.

1 Initial conditions :

Tuning : 118.250 MHz
Field strength : 1 mV/m
(received)

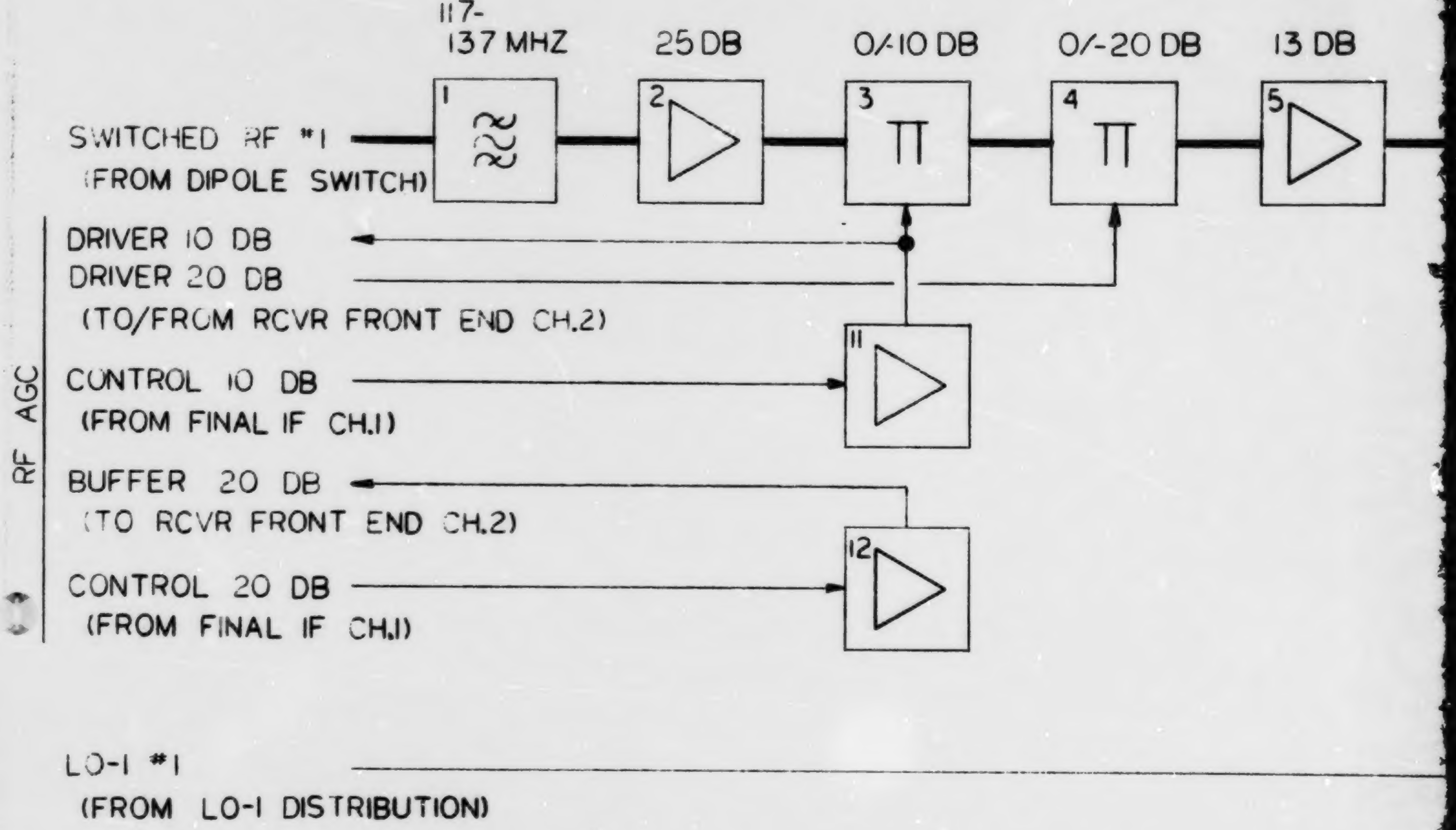
2 Set-up :


CW
SWITCHED RF #1
RCVR FRONT END CH.I
IF-1 #1
HIP
RF AGC
S.A.
SECOND CONVER-SION CH.I
IF-2 #1
FINAL IF CH.I
IF-3 #1
PHASE COMPA-RATOR
IF-3 #2
HIP : High Impedance Probe
S.A. : Spectrum analyser

Setting of spectrum analyser

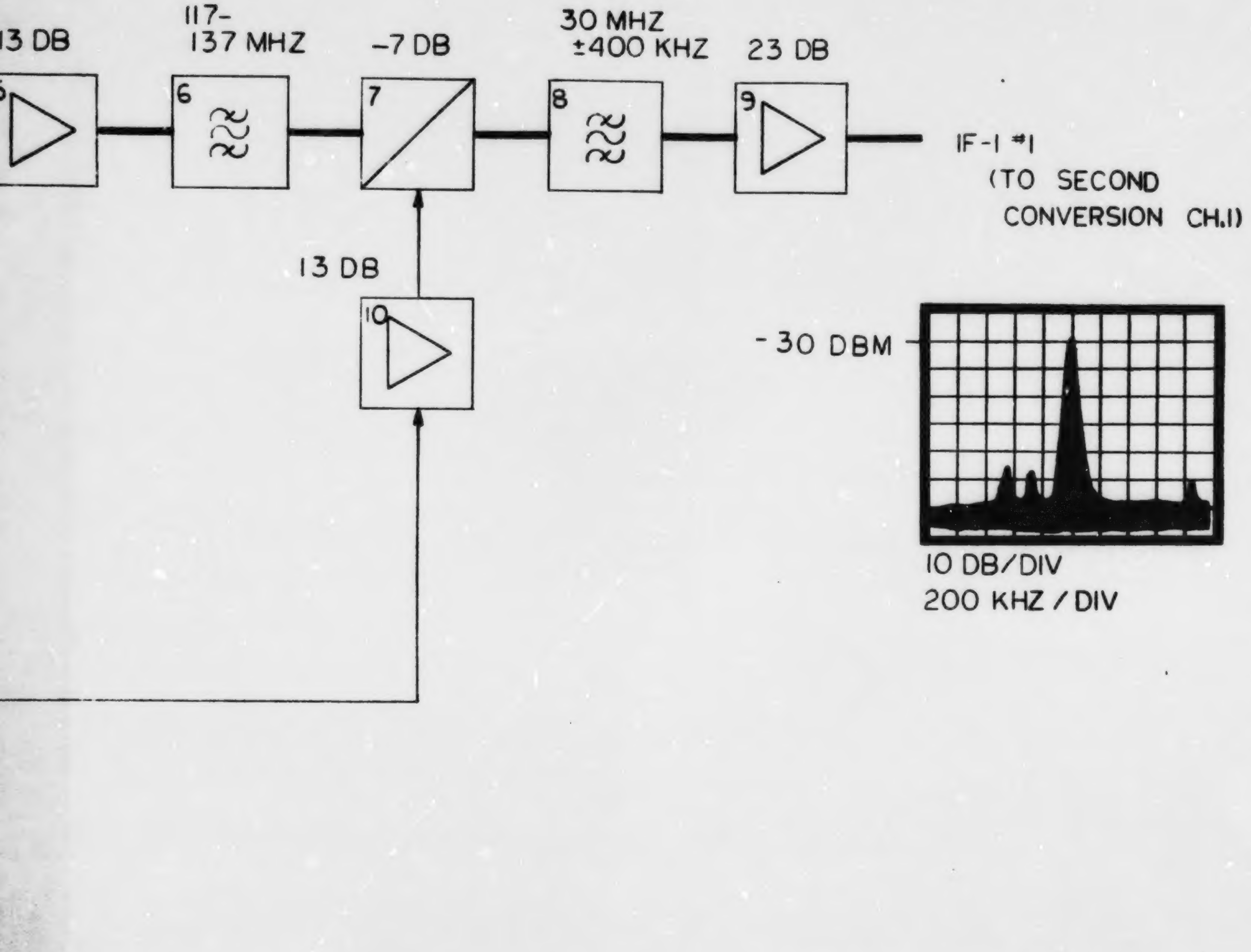
Bandwidth : 30 KHz
Scan width : 200 KHz/DIV
Attenuation : 0 dB
Scan time : 0.5 SEC/DIV
VIDEO FILTER : 10 KHz

Signal strength : - 30 dBm



117-137 MHZ
25 DB
0/-10 DB
0/-20 DB
13 DB
1
2
3
4
5
11
12
SWITCHED RF #1
(FROM DIPOLE SWITCH)
DRIVER 10 DB
DRIVER 20 DB
(TO/FROM RCVR FRONT END CH.2)
CONTROL 10 DB
(FROM FINAL IF CH.1)
BUFFER 20 DB
(TO RCVR FRONT END CH.2)
CONTROL 20 DB
(FROM FINAL IF CH.1)
RF AGC
LO-1 #1
(FROM LO-1 DISTRIBUTION)

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may
neither used, copied, reproduced or otherwise dealt with,
nor its contents communicated to others.


13 DB
117-
137 MHZ
-7 DB
30 MHZ
±400 KHZ
23 DB
5
6
7
8
9
IF-1 #1
(TO SECOND
CONVERSION CH.1)
13 DB
10
- 30 DBM
10 DB/DIV
200 KHZ / DIV

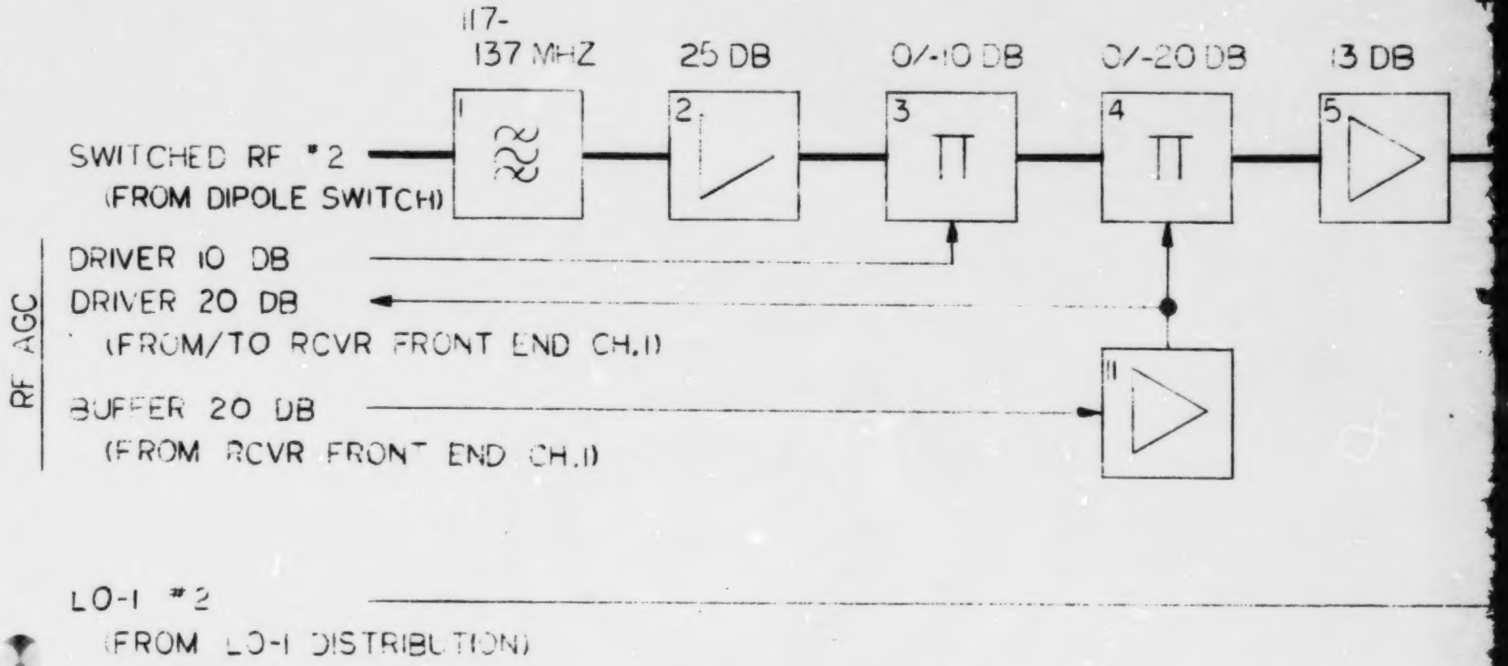
| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ±

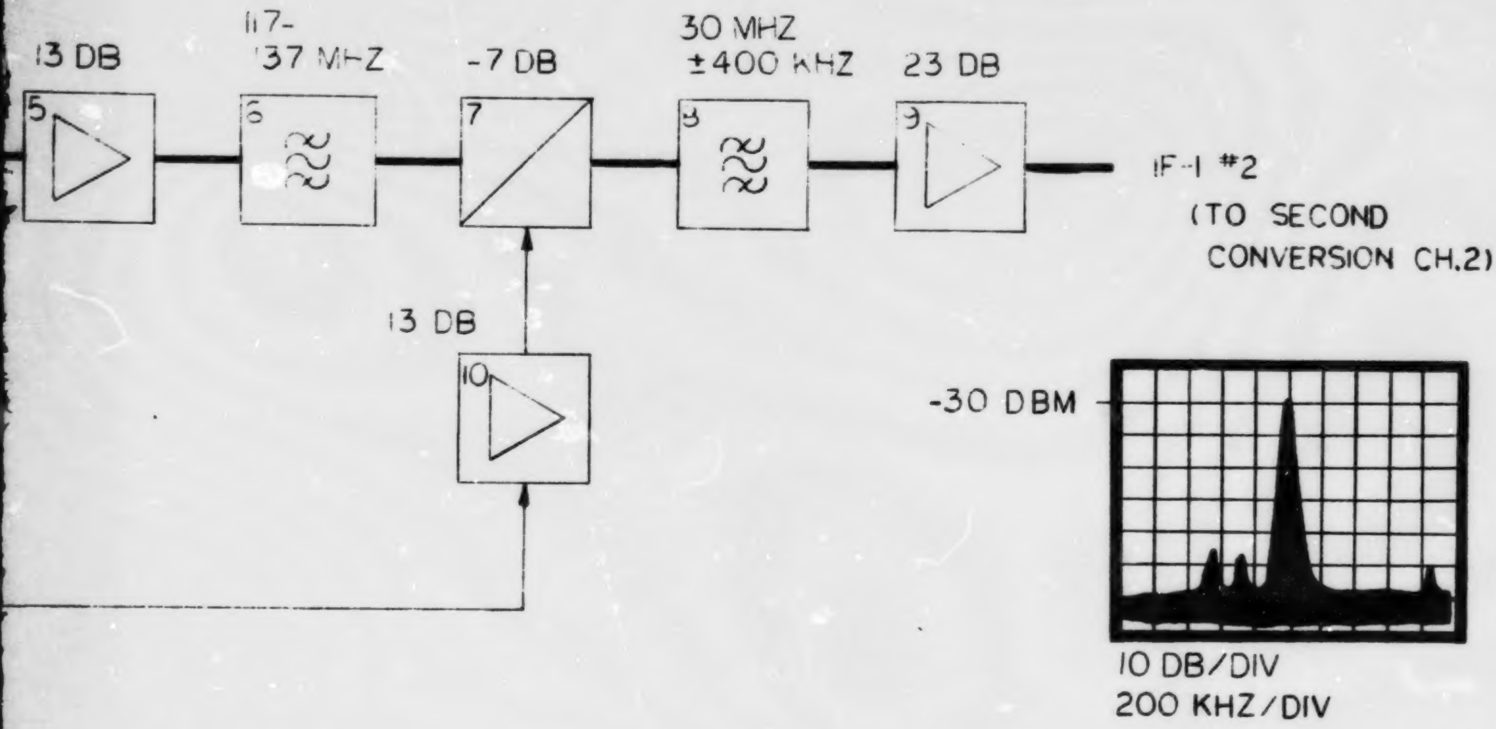
**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
RCVR FRONT END CH.I

DRAWN BY S. B.
DATE 83-1-20
CHECKED BY
APPROVED BY
DRAWING NO. 66-0643.027 388.BD-B


117-
137 MHZ
25 DB
0/-10 DB
0/-20 DB
13 DB
1
2
3
4
5
5
11
SWITCHED RF #2
(FROM DIPOLE SWITCH)
RF AGC
DRIVER 10 DB
DRIVER 20 DB
(FROM/TO RCVR FRONT END CH.1)
BUFFER 20 DB
(FROM RCVR FRONT END CH.1)
LO-1 #2
(FROM LO-1 DISTRIBUTION)

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may
neither used, copied, reproduced or otherwise dealt with
nor its contents communicated to others.



13 DB
117-
137 MHZ
-7 DB
30 MHZ
±400 KHZ
23 DB
5
6
7
8
9
IF-1 #2
(TO SECOND
CONVERSION CH.2)
13 DB
10
-30 DBM
10 DB/DIV
200 KHZ/DIV

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE

REMOVE BURR MAX .010R

MATERIAL

FINISH

may be
dealt with,

UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ± ANGLES ± °

DRAWN BY: S. B.

DATE: 83-1-20

CHECKED BY

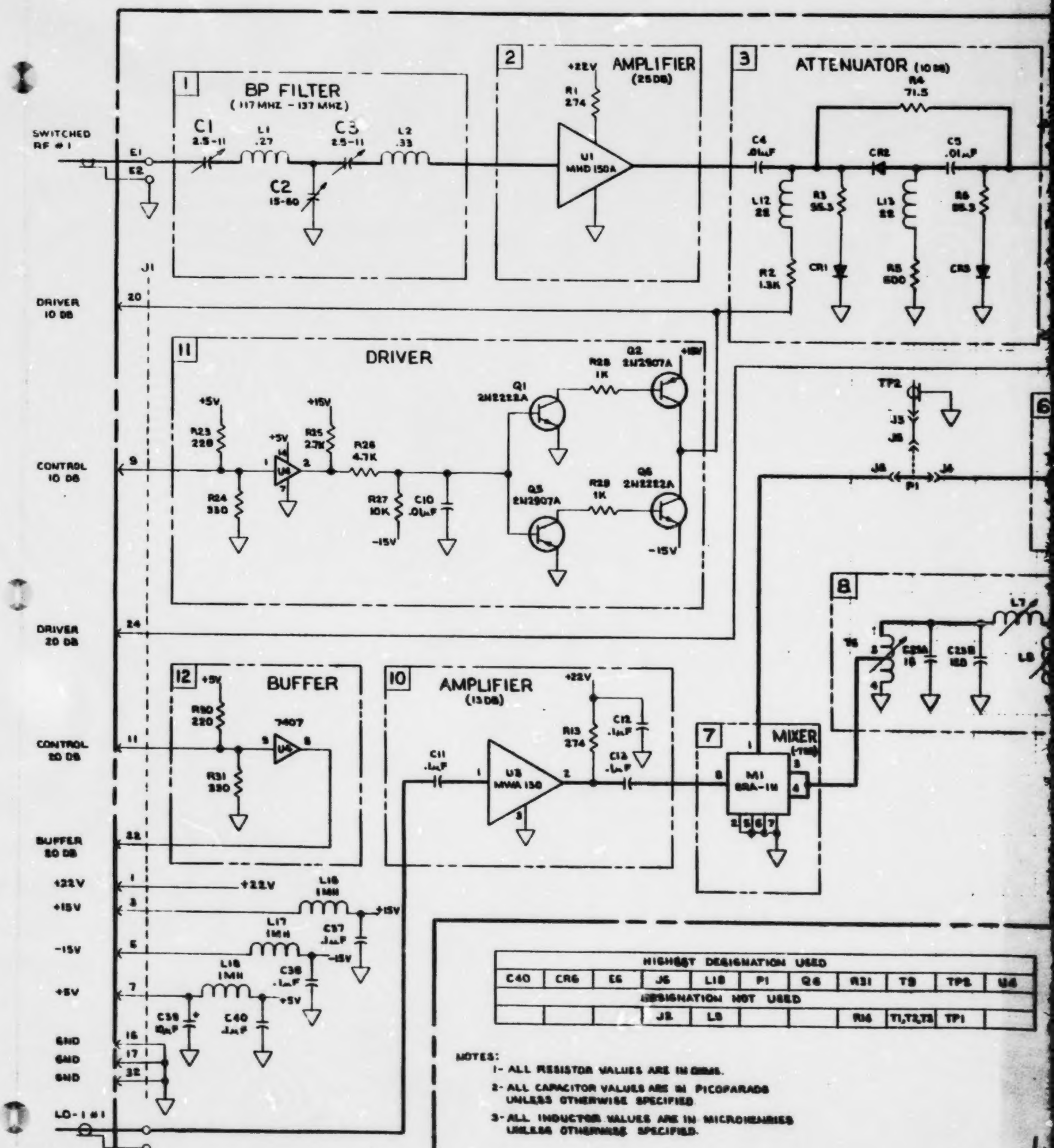
APPROVED BY

**BAYLY** ENGINEERING LTD
a member of

TITLE: BLOCK DIAGRAM
RCVR FRONT END CH.2

DRAWING NO. 66-0643.035 322.BD-B

Without prior written consent of
Y ENGINEERING LIMITED, this document may be
used, copied, reproduced or otherwise dealt with,
[illegible] communicated to others.


SWITCHED RF # 1
E1
E2
1
BP FILTER
( 117 MHZ - 137 MHZ )
C1
2.5-11
L1
.27
C3
2.5-11
L2
.33
C2
15-60
2
AMPLIFIER
(25DB)
+22V
R1
274
U1
MHD 150A
3
ATTENUATOR (10DB)
R4
71.5
C4
.01μF
CR2
C5
.01μF
L12
22
R3
95.3
L13
22
R6
95.3
R2
1.3K
CR1
R5
600
CR3
J1
DRIVER 10 DB
20
11
DRIVER
R28
1K
Q2
2N2907A
+15V
Q1
2N2222A
+5V
+15V
R23
220
+5V
14
R25
2.7K
R26
4.7K
CONTROL 10 DB
9
1
U4
2
7
R24
330
R27
10K
C10
.01μF
-15V
Q5
2N2907A
R29
1K
Q6
2N2222A
-15V
TP2
J5
J5
J6
P1
J4
6
8
L7
T5
1
2
4
C23A
15
C23B
180
L8
DRIVER 20 DB
24
12
+5V
BUFFER
R30
220
7407
9
U4
8
CONTROL 20 DB
11
R31
330
10
AMPLIFIER
(13DB)
+22V
R13
274
C12
.1μF
C11
.1μF
1
U3
MWA 130
2
3
C13
.1μF
7
MIXER
(-7DB)
1
3
8
M1
SRA-1H
4
2
5
6
7
BUFFER 20 DB
22
+22V
1
+22V
+15V
3
L16
1MH
+15V
-15V
5
L17
1MH
C37
.1μF
-15V
+5V
7
L18
1MH
C38
.1μF
+5V
C39
10μF
+
C40
.1μF
GND
16
GND
17
GND
32
LO-1 # 1

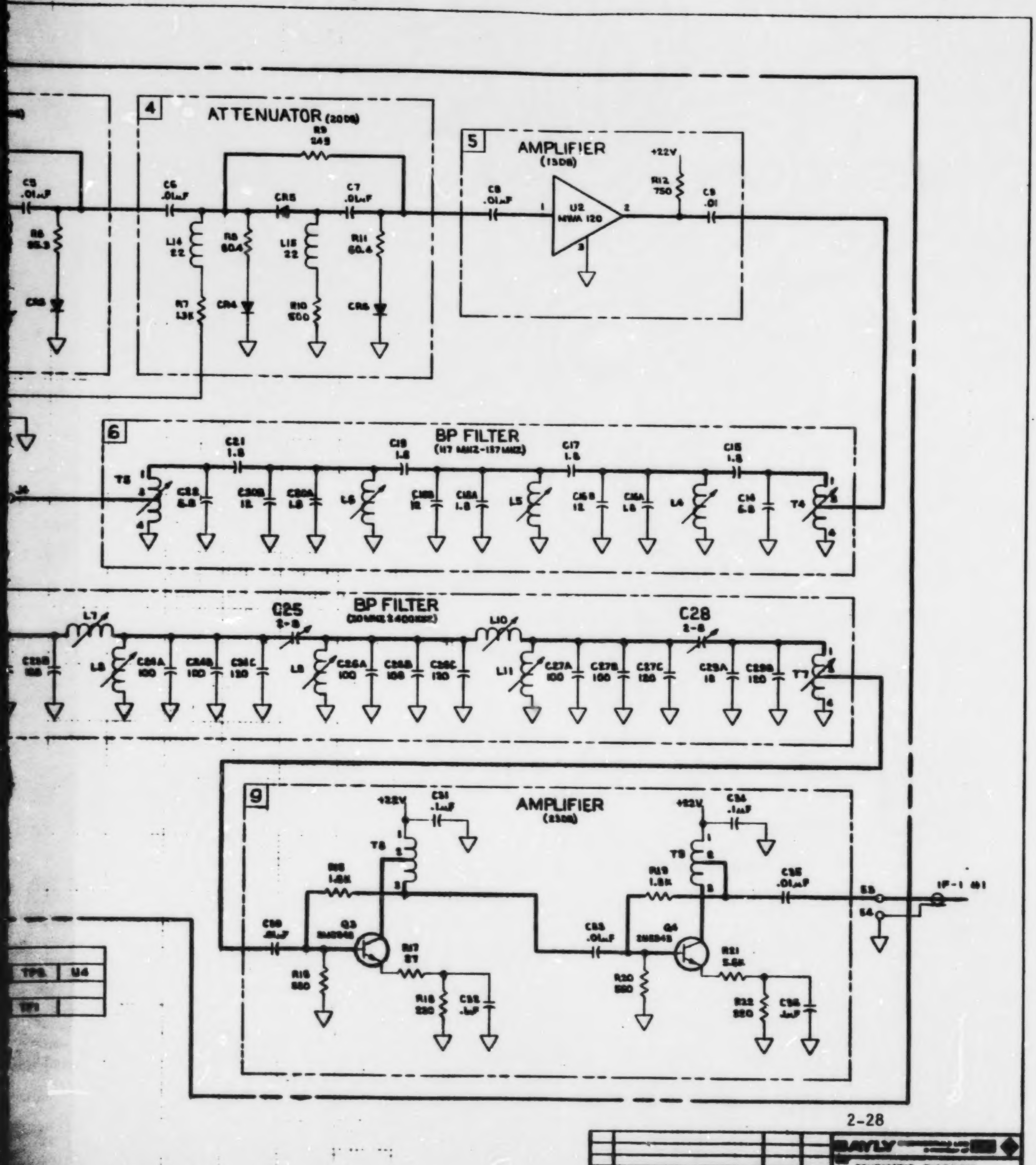
| HIGHEST DESIGNATION USED | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| C40 | CR6 | E6 | J6 | L18 | P1 | Q6 | R31 | T9 | TP2 | U4 |
| DESIGNATION NOT USED | | | | | | | | | | |
| | | | J2 | L8 | | | R16 | T1,T2,T3 | TP1 | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

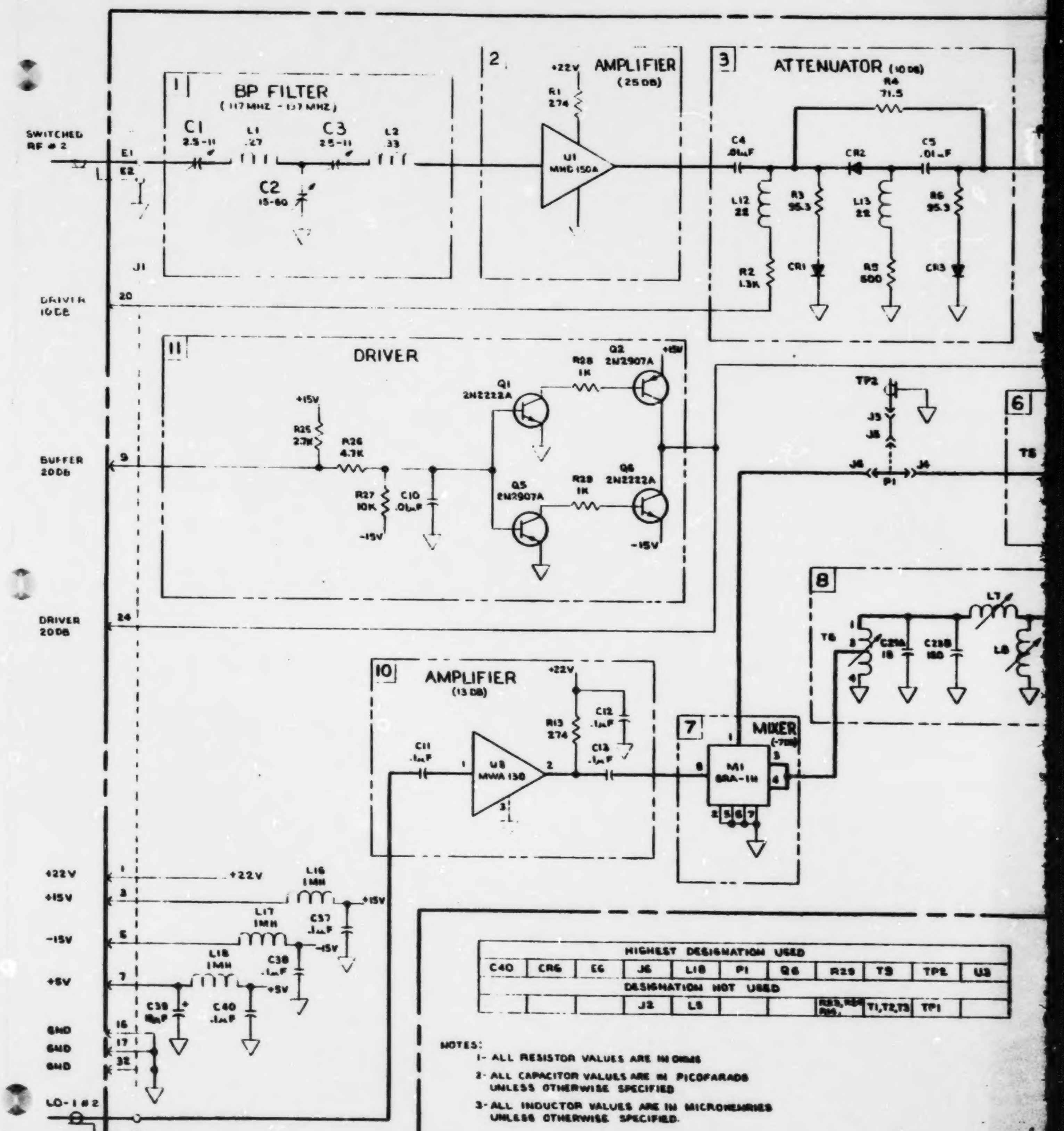
2- ALL CAPACITOR VALUES ARE IN PICOFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES UNLESS OTHERWISE SPECIFIED.



4
ATTENUATOR (20DB)
R9 249
C5 .01µF
R8 95.3
CR3
C6 .01µF
L14 22
R7 1.3K
R5 60.4
CR4
CR5
L15 22
R10 500
C7 .01µF
R11 60.4
CR6
5
AMPLIFIER (13DB)
C8 .01µF
U2 MWA 120
+22V
R12 750
C9 .01
6
BP FILTER (117 MHZ-137 MHZ)
C21 1.8
C19 1.8
C17 1.8
C15 1.8
T5
J4
C22 6.8
C20B 12
C20A 1.8
L6
C18B 12
C18A 1.8
L5
C16B 12
C16A 1.8
L4
C14 6.8
T4
BP FILTER
C25 2-8
C28 2-8
L7
L8
L9
L10
L11
C23B 100
C24A 100
C24B 100
C24C 120
C26A 100
C26B 100
C26C 120
C27A 100
C27B 100
C27C 120
C29A 18
C29B 120
T7
9
AMPLIFIER (23DB)
+22V
C31 .1µF
T8
R16 1.8K
C30 .01µF
Q3 2N5843
R15 560
R17 27
R18 220
C32 .1µF
+22V
C34 .1µF
T9
R19 1.8K
C33 .01µF
Q4 2N5843
R20 560
R21 5.6K
R22 220
C36 .1µF
C35 .01µF
E3
E4
IF-1 (1)
TP2
U4
TP1
SCHEMATIC DIAGRAM
RCVR FRONT END CHAN 1
86-0643.027 368.CD

[illegible]


1 BP FILTER
(117 MHZ - 137 MHZ)
C1 2.5-11
L1 .27
C3 2.5-11
L2 .33
C2 15-60
2 AMPLIFIER (25 DB)
+22V
R1 274
U1 MHD 150A
3 ATTENUATOR (10 DB)
R4 71.5
C4 .01µF
CR2
C5 .01µF
L12 22
R3 95.3
L13 22
R6 95.3
R2 1.3K
CR1
R5 500
CR3
SWITCHED RF # 2
E1
E2
J1
DRIVER 10 DB
20
11 DRIVER
+15V
R25 2.7K
R26 4.7K
R27 10K
C10 .01µF
-15V
Q1 2N2222A
R28 1K
Q2 2N2907A
+15V
Q5 2N2907A
R29 1K
Q6 2N2222A
-15V
BUFFER 20 DB
9
TP2
J5
J5
J6
P1
J4
6
T5
8
L7
T6
1
2
3
4
C23A 18
C23B 180
L8
DRIVER 20 DB
24
10 AMPLIFIER (13 DB)
+22V
R13 274
C12 .1µF
C11 .1µF
U3 MWA 130
C13 .1µF
1
2
3
7 MIXER (-7 DB)
M1 SRA-1H
1
8
3
4
2 5 6 7
+22V
+15V
-15V
+5V
GND
GND
GND
1
3
6
7
16
17
32
+22V
L16 1MH
+15V
L17 1MH
C37 .1µF
-15V
L18 1MH
C38 .1µF
+5V
C39 10µF
C40 .1µF
LO-1 # 2

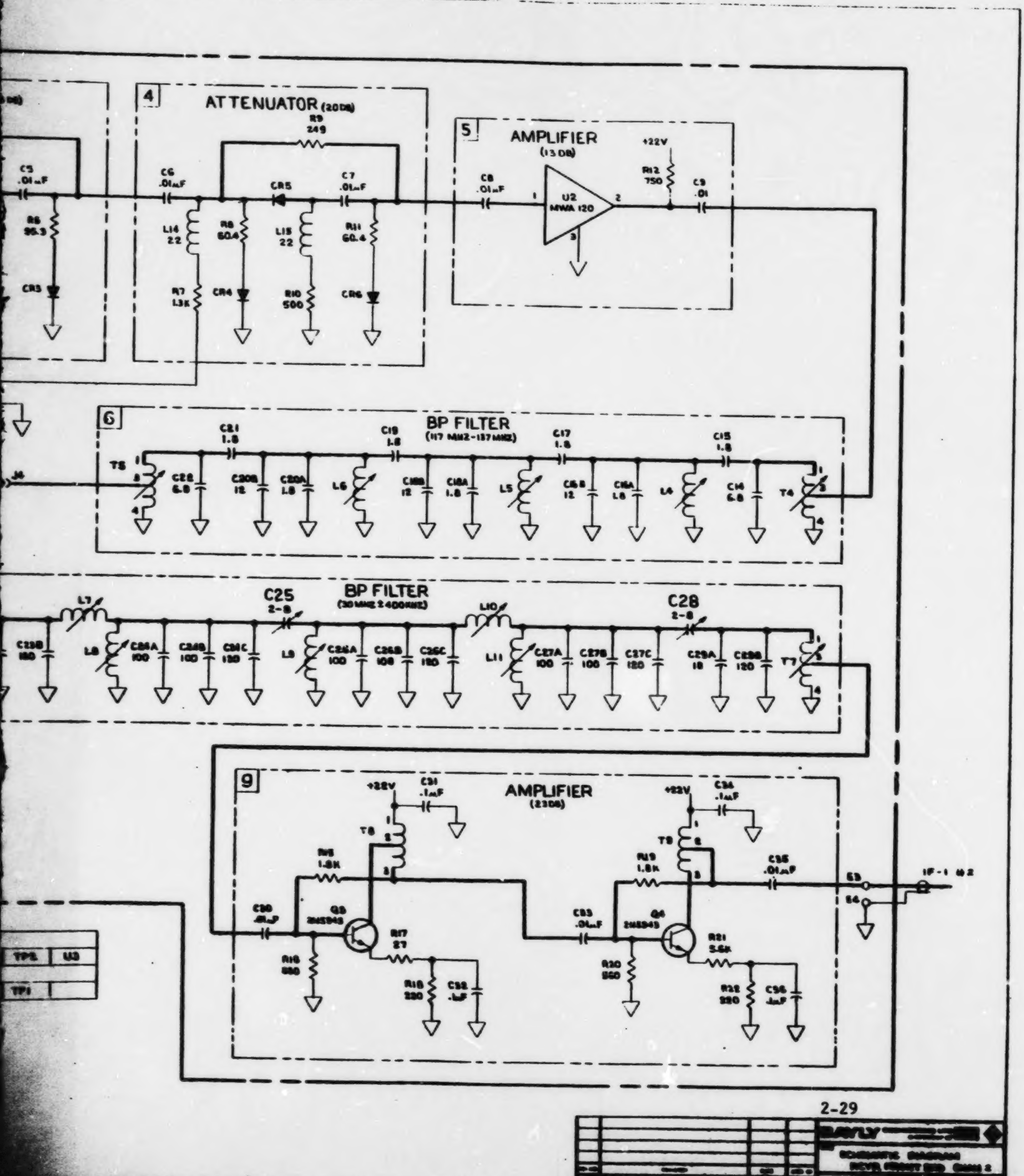
| HIGHEST DESIGNATION USED | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| C40 | CR6 | E6 | J6 | L18 | P1 | Q6 | R29 | T9 | TP2 | U3 |
| DESIGNATION NOT USED | | | | | | | | | | |
| | | | J2 | L5 | | | R23, R24<br>R10, | T1,T2,T3 | TP1 | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS

2- ALL CAPACITOR VALUES ARE IN PICOFARADS UNLESS OTHERWISE SPECIFIED

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES UNLESS OTHERWISE SPECIFIED.


4
ATTENUATOR (20DB)
R9 249
C5 .01µF
R6 95.3
CR3
C6 .01µF
L14 22
R7 1.3K
R8 60.4
CR4
CR5
L15 22
R10 500
C7 .01µF
R11 60.4
CR6
5
AMPLIFIER (13DB)
C8 .01µF
U2 MWA 120
+22V
R12 750
C9 .01
6
BP FILTER (117 MHZ-137 MHZ)
T5
J4
C21 1.8
C22 6.8
C20B 12
C20A 1.8
L6
C19 1.8
C18B 12
C18A 1.8
L5
C17 1.8
C16B 12
C16A 1.8
L4
C15 1.8
C14 6.8
T4
BP FILTER (30 MHZ ± 400 KHZ)
L7
C23B 180
L8
C24A 100
C24B 100
C24C 120
C25 2-8
L9
C26A 100
C26B 100
C26C 120
L10
L11
C27A 100
C27B 100
C27C 120
C28 2-8
C29A 18
C29B 120
T7
9
AMPLIFIER (23DB)
+22V
C31 .1µF
T8
R15 1.8K
C30 .01µF
Q3 2N5943
R16 560
R17 27
R18 220
C32 .1µF
C33 .01µF
Q4 2N5943
R20 560
+22V
C34 .1µF
T9
R19 1.8K
R21 5.6K
R22 220
C36 .1µF
C35 .01µF
E3
E4
IF-1 J12
TP2
U3
TP1
SCHEMATIC DIAGRAM

### 2.3.1.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 6 | 8 | | | | | |
| Adjusters | C1<br>C2<br>C3 | T4<br>T5<br>L4<br>L5<br>L6 | T6<br>T7<br>L7<br>L8<br>L9<br>L10<br>L11<br>C25<br>C28 | | | | | |

The alignment of Blocks # 1, # 6, # 8 (filters) is done according to specifications written in 2.3.1.4.

### 2.3.1.4 SPECIFICATIONS

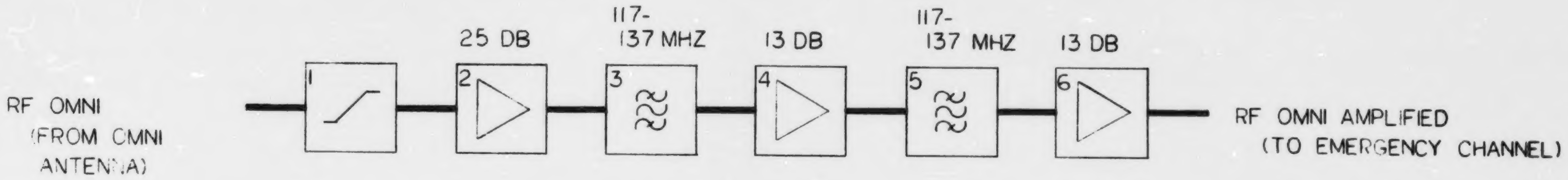
| | BLOCK # | | | | |
|---|---|---|---|---|---|
| | 1 | 6 | 8 | MODULE | |
| Impedance INPUT (ohms)<br>OUTPUT (ohms) | 50<br>50 | 50<br>50 | 50<br>50 | 50<br>50 | |
| Gain - Loss (dB) | | | | 40 | |
| Noise Figure (dB) | | | | 7 | |
| Band-Pass (1 dB) (MHz)<br>(3 dB) (MHz)<br>(40 dB) (MHz) | 117 @ 137<br>106 @ 1461<br>17 @ 535 | 117 @ 137 | 29.6 @ 30.4 | | |
| Insertion Loss (dB)<br>(Center Bandwidth) | -1 | -5 | -7 | | |
| | | | | | |

## 2.3.2 OMNI RF AMPLIFIER

a This module is located in the antenna box.

b Its main functions are :

1 To amplify the signal.
2 To limit the band-pass between 117 and 137 MHz.


RF OMNI
(FROM OMNI
ANTENNA)
1
25 DB
2
117-
137 MHZ
3
13 DB
4
117-
137 MHZ
5
13 DB
6
RF OMNI AMPLIFIED
(TO EMERGENCY CHANNEL)

| | | | |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| REV. NO. | REVISION | DATE | APPR. BY |

SCALE

REMOVE BURR MAX .010R

MATERIAL

FINISH

**BAYLY** ENGINEERING LTD
a member of

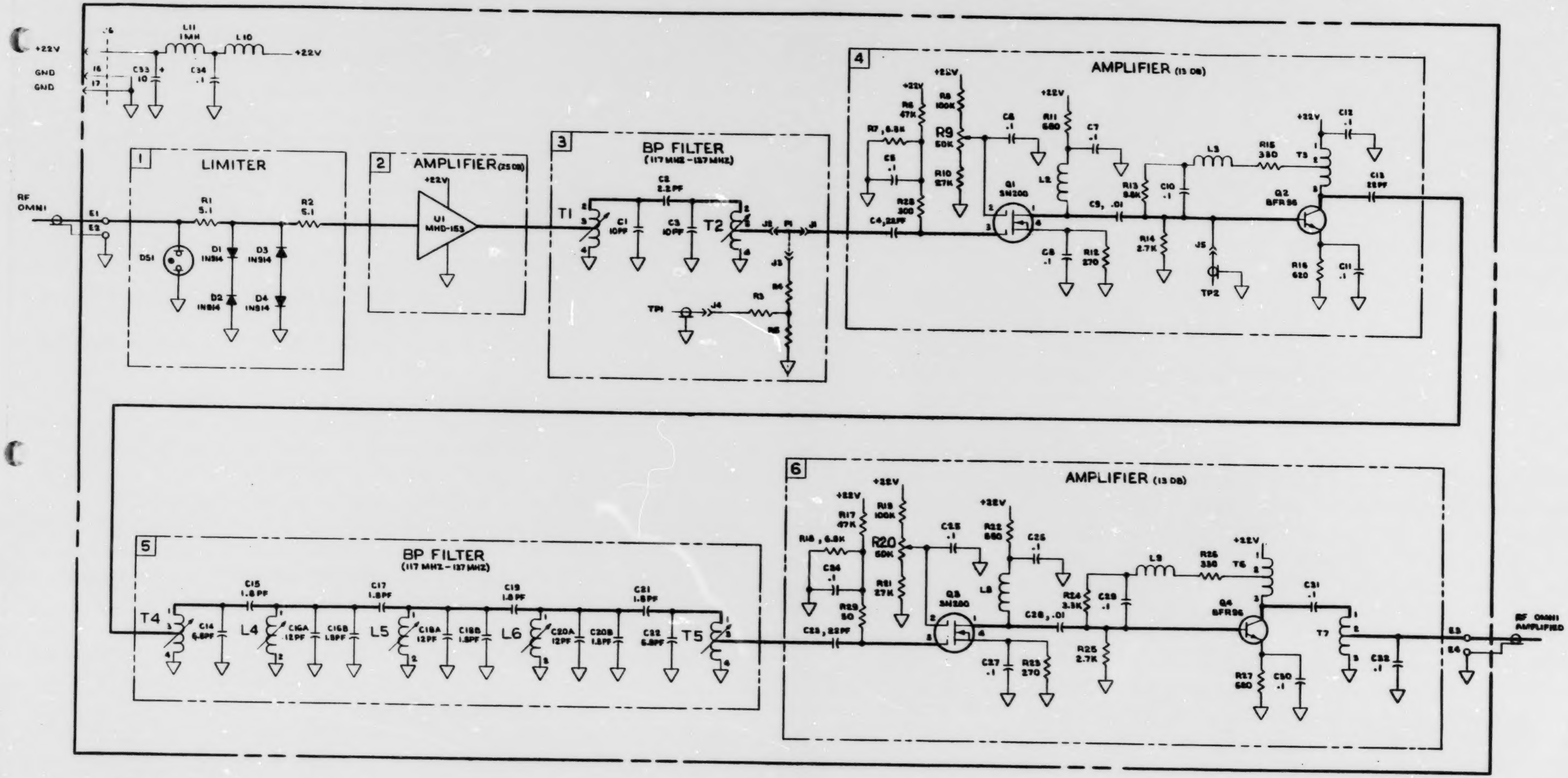
TITLE
BLOCK DIAGRAM
OMNI RF AMPLIFIER

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

UNLESS OTHERWISE SPECIFIED
TOLERANCES
DECIMALS ±
ANGLES
± °

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| S.B. | 83-1-20 | | | 66-0643.027 868.BD-B |

[illegible]


+22V
GND
GND
L11
1MH
L10
+22V
C33
10
C34
.1
RF
OMNI
E1
E2
1
LIMITER
R1
5.1
R2
5.1
DS1
D1
IN914
D2
IN914
D3
IN914
D4
IN914
2
AMPLIFIER(25DB)
+22V
U1
MHD-153
3
BP FILTER
(117MHZ-137MHZ)
T1
C1
10PF
C2
2.2PF
C3
10PF
T2
J2
P1
J1
J3
R4
R3
R5
J4
TP1
4
AMPLIFIER (13 DB)
+22V
R6
47K
R7, 6.8K
R8
100K
R9
50K
R10
27K
C5
.1
R28
300
C4, 22PF
C6
.1
R11
680
C7
.1
L2
Q1
3N200
C8
.1
R12
270
C9, .01
R13
6.8K
C10
.1
L3
R15
330
T3
C12
.1
C13
22PF
Q2
BFR96
R14
2.7K
J5
TP2
R16
620
C11
.1
5
BP FILTER
(117 MHZ-137 MHZ)
T4
C14
6.8PF
C15
1.8PF
L4
C16A
12PF
C16B
1.8PF
C17
1.8PF
L5
C18A
12PF
C18B
1.8PF
C19
1.8PF
L6
C20A
12PF
C20B
1.8PF
C21
1.8PF
C22
6.8PF
T5
6
AMPLIFIER (13 DB)
+22V
R17
47K
R18, 6.8K
R19
100K
R20
50K
R21
27K
C24
.1
R29
50
C23, 22PF
C25
.1
R22
680
C26
.1
L8
Q3
3N200
C27
.1
R23
270
C28, .01
R24
3.3K
C29
.1
L9
R26
330
T6
Q4
BFR96
R25
2.7K
C31
.1
T7
R27
680
C30
.1
C32
.1
E3
E4
RF OMNI
AMPLIFIED

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

| HIGHEST DESIGNATION USED | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C34 | D4 | DS1 | E4 | J6 | L11 | P1 | Q4 | R29 | T7 | TP2 | U1 |
| DESIGNATION NOT USED | | | | | | | | | | | |
| | | | | | L1, L7 | | | | | | |

BAYLY

SCHEMATIC DIAGRAM
RF OMNI AMPLIFIER

66-0640.067 000.CD

14-1-83

## 2.3.2.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 3 | 4 | 5 | 6 | | | | |
| Adjusters | T1<br>T2 | R9 | T4<br>T5<br>L4<br>L5<br>L6 | R20 | | | | |

The alignment of blocks 3, 5 (filters), 4 and 6 is done according to specifications written in 2.3.2.4.

2.3.2.4 SPECIFICATIONS

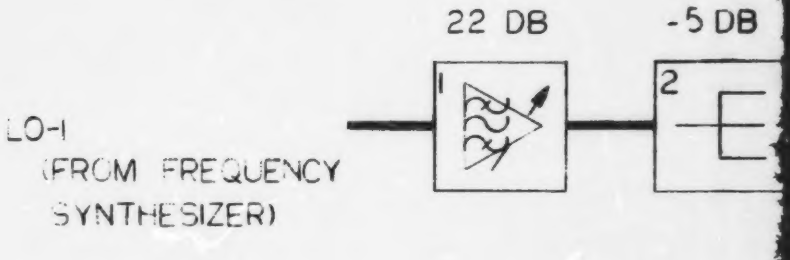
| | BLOCK # | | | | |
|---|---|---|---|---|---|
| | 3 | 4 | 5 | 6 | MODULE |
| Impedance INPUT (ohms) | 50 | 300 | 50 | 50 | 50 |
| OUTPUT (ohms) | 300 | 50 | 50 | 50 | 50 |
| Gain - Loss (dB) | | 13 | | 13 | 20 |
| Band-Pass (1 dB) (MHz) | 117 @ 137 | | 117 @ 137 | | |
| | | | | | |

### 2.3.3 LO-1 DISTRIBUTION

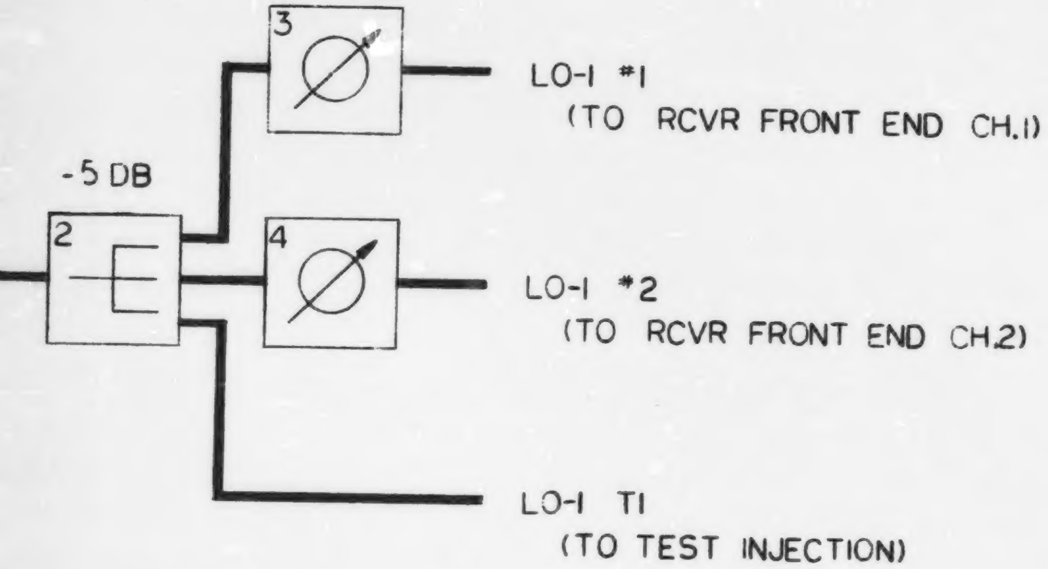
a This module is located in the antenna box.

b Its main functions are :

1. Amplification and distribution of the first local oscillator.
2. To adjust in phase the two local oscillators.


22 DB
-5 DB
1
2
LO-1
(FROM FREQUENCY
SYNTHESIZER)

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document
neither used, copied, reproduced or otherwise
nor its contents communicated to others.


3
LO-I #I
(TO RCVR FRONT END CH.I)
-5 DB
2
4
LO-I *2
(TO RCVR FRONT END CH.2)
LO-I TI
(TO TEST INJECTION)

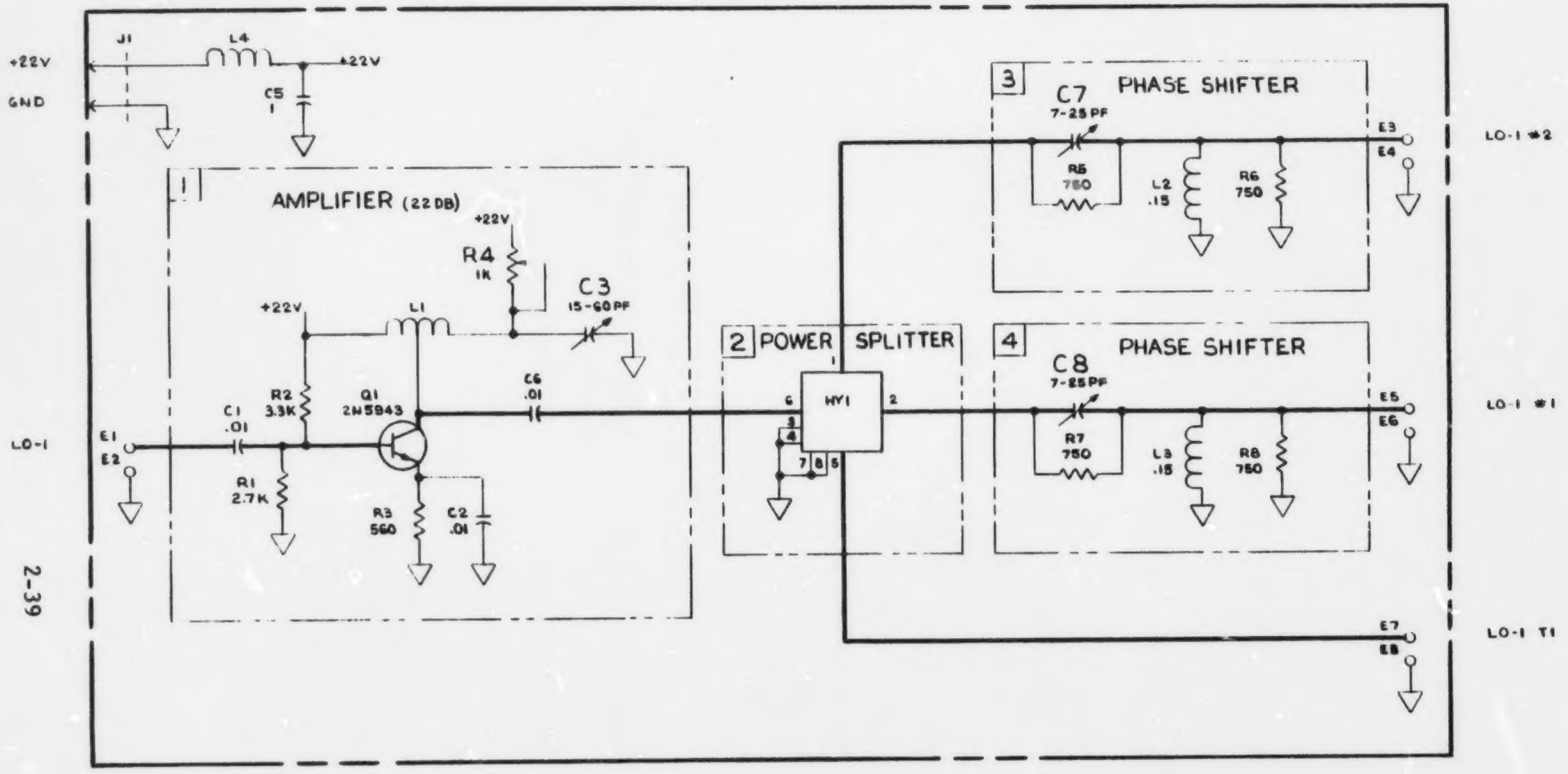
| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED
TOLERANCES DECIMALS ± ANGLES ± °
DRAWN BY S.B.
DATE 83-1-20
CHECKED BY
APPROVED BY

**BAYLY** ENGINEERING LTD
a member of

TITLE BLOCK DIAGRAM
LO-I DISTRIBUTION

DRAWING NO. 67-0643.030 618.BD-B


+22V
GND
J1
L4
+22V
C5
1
1
AMPLIFIER (22 DB)
+22V
R4
1K
C3
15-60PF
+22V
L1
C6
.01
LO-1
E1
E2
C1
.01
R2
3.3K
Q1
2N5943
R1
2.7K
R3
560
C2
.01
2 POWER SPLITTER
HY1
6
2
3
4
7
8
5
3
C7
7-25PF
PHASE SHIFTER
R5
750
L2
.15
R6
750
E3
E4
LO-1 #2
4
C8
7-25PF
PHASE SHIFTER
R7
750
L3
.15
R8
750
E5
E6
LO-1 #1
E7
E8
LO-1 T1

| HIGHEST DESIGNATION USED | | | | | | |
|---|---|---|---|---|---|---|
| C8 | E8 | J1 | HY1 | L4 | Q1 | R8 |
| DESIGNATION NOT USED | | | | | | |
| C4 | | | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES UNLESS OTHERWISE SPECIFIED

This drawing is the property of BAYLY ENGINEERING LIMITED and may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others without written permission.

BAYLY ENGINEERING LTD

SCHEMATIC DIAGRAM
LO-1 DISTRIBUTION

17-1-83

67-0643.030 618 .CD -C

### 2.3.3.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 3 | 4 | | | | | |
| Adjusters | C3 | C7 | C8 | | | | | |

a Block 3, 4

Adjust "C7", "C8" until the phase difference between LO-1 # 1 and LO-1 # 2 is close to zero.

b Block 1

1 Adjust the bandwidth (147 @ 167 MHz) with "C3".

2 Adjust the gain "R4" for the optimum insertion loss in the first conversion.

### 2.3.3.4 SPECIFICATIONS

| | MODULE | | | | |
|---|---|---|---|---|---|
| Impedance INPUT<br>OUTPUT (ohms) | 50<br>50 | | | | |
| | | | | | |

## 2.3.4 SECOND CONVERSION DF CHANNEL # 1

a This module is located in the receiver unit.

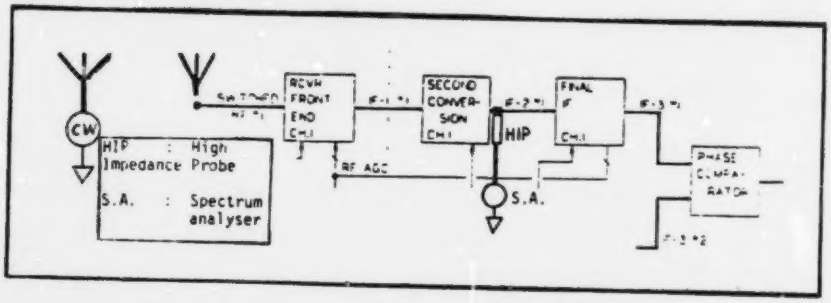
b Its main function is to convert the frequency from 30 MHz to 2.2 MHz.

c On the block diagram, we illustrate the form of the signal at the module output as seen on the spectrum analyser.

1 Initial conditions :

Tuning : 118.250 MHz
Field strength : 1 mV/m
(received)

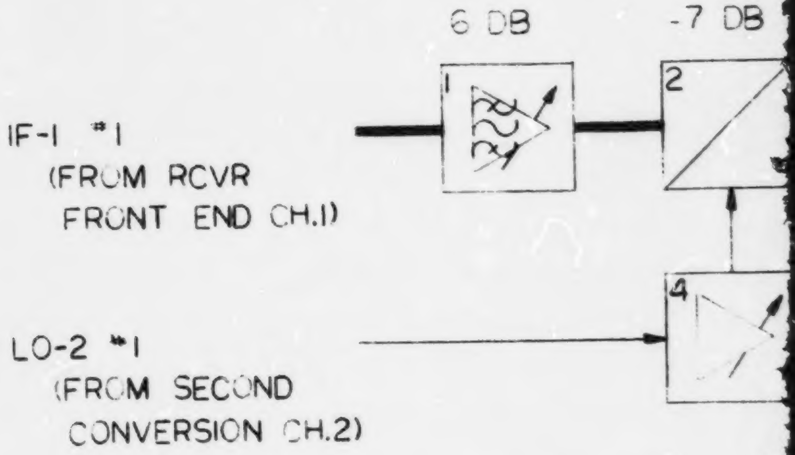
2 Set-up :


CW
SWITCHED RF #1
RCVR FRONT END CH.1
IF-1 #1
SECOND CONVER-SION CH.1
IF-2 #1
HIP
FINAL IF CH.1
IF-3 #1
RF AGC
S.A.
PHASE COMPA-RATOR
IF-3 #2
HIP : High Impedance Probe
S.A. : Spectrum analyser

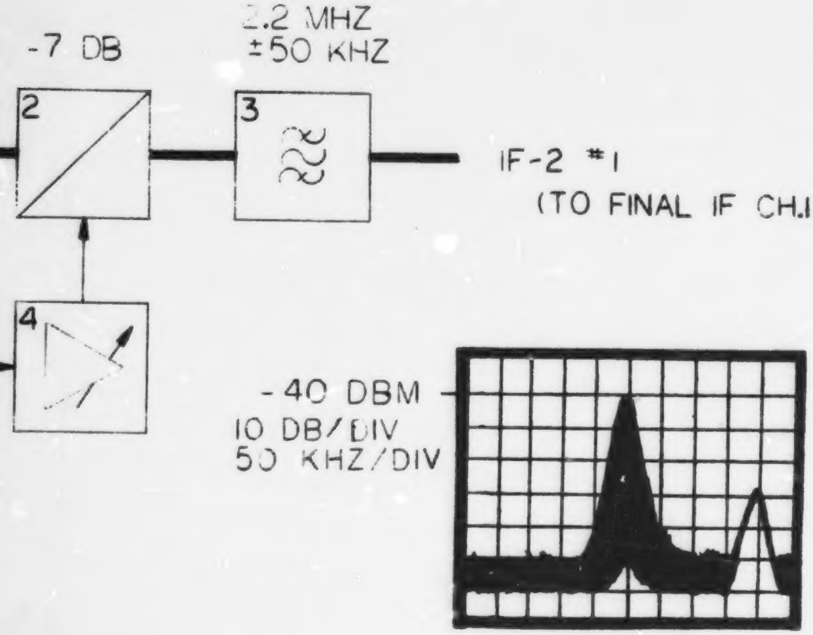
Setting of spectrum analyser

Bandwidth : 10 KHz
Scan width : 50 KHz/DIV
Attenuation : 0 dB
Scan Time : 0.5 SEC/DIV
VIDEO FILTER : 10 KHz

Signal strength : - 40 dBm


6 DB
-7 DB
1
2
4
IF-1 #1
(FROM RCVR
FRONT END CH.1)
LO-2 #1
(FROM SECOND
CONVERSION CH.2)

Without prior written consent of
BAYLY ENGINEERING LIMITED, this docum
neither used, copied, reproduced or otherwise dis
nor its contents communicated to others.


-7 DB
2.2 MHZ
±50 KHZ
2
3
4
IF-2 #1
(TO FINAL IF CH.I)
-40 DBM
10 DB/DIV
50 KHZ/DIV

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

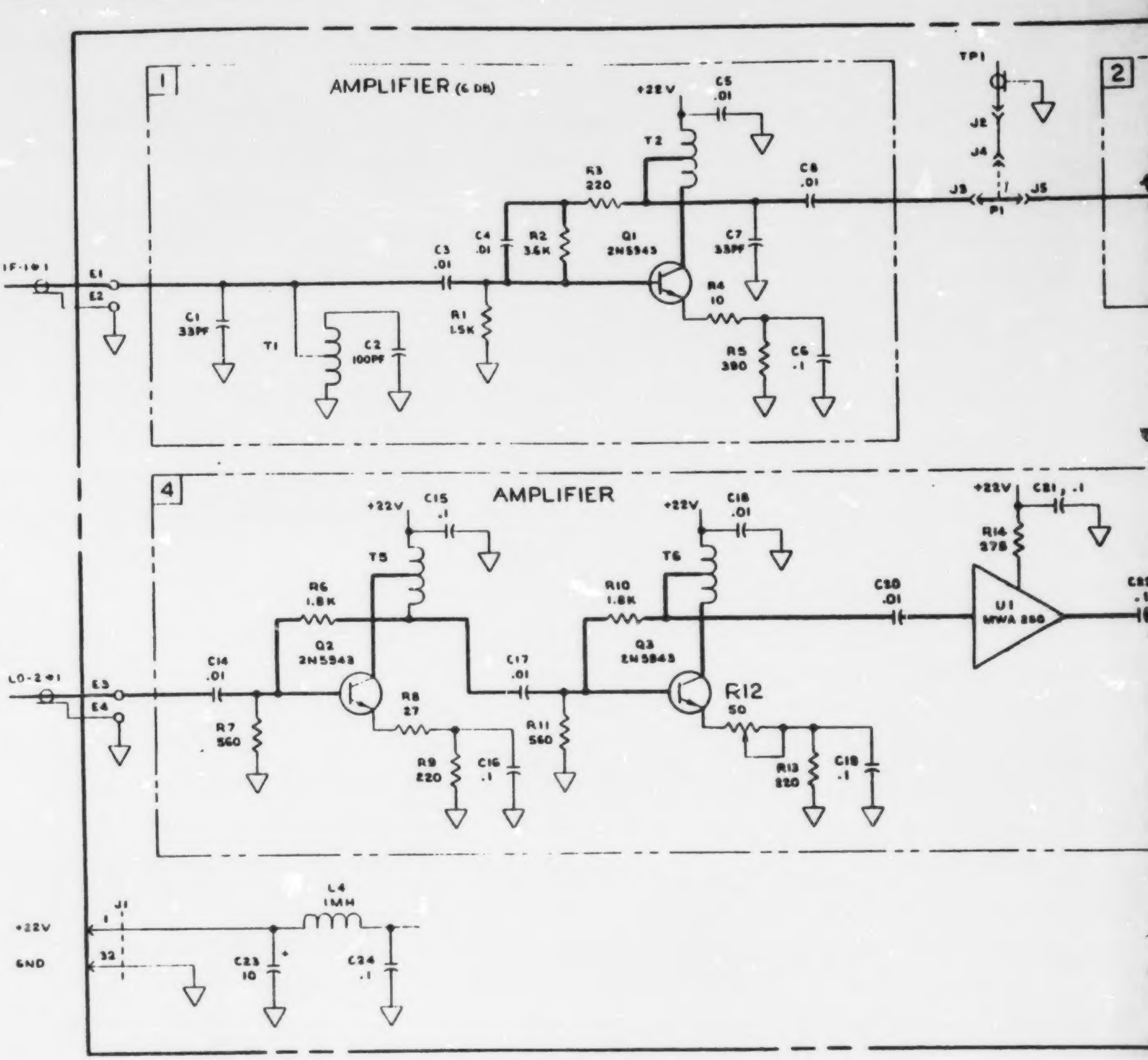
...t of
...ocument may be
...ise dealt with,

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| S.B. | 83-1-20 |  |  | 66-0643.028 372.BD-B |

**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
SECOND CONVERSION CH.I

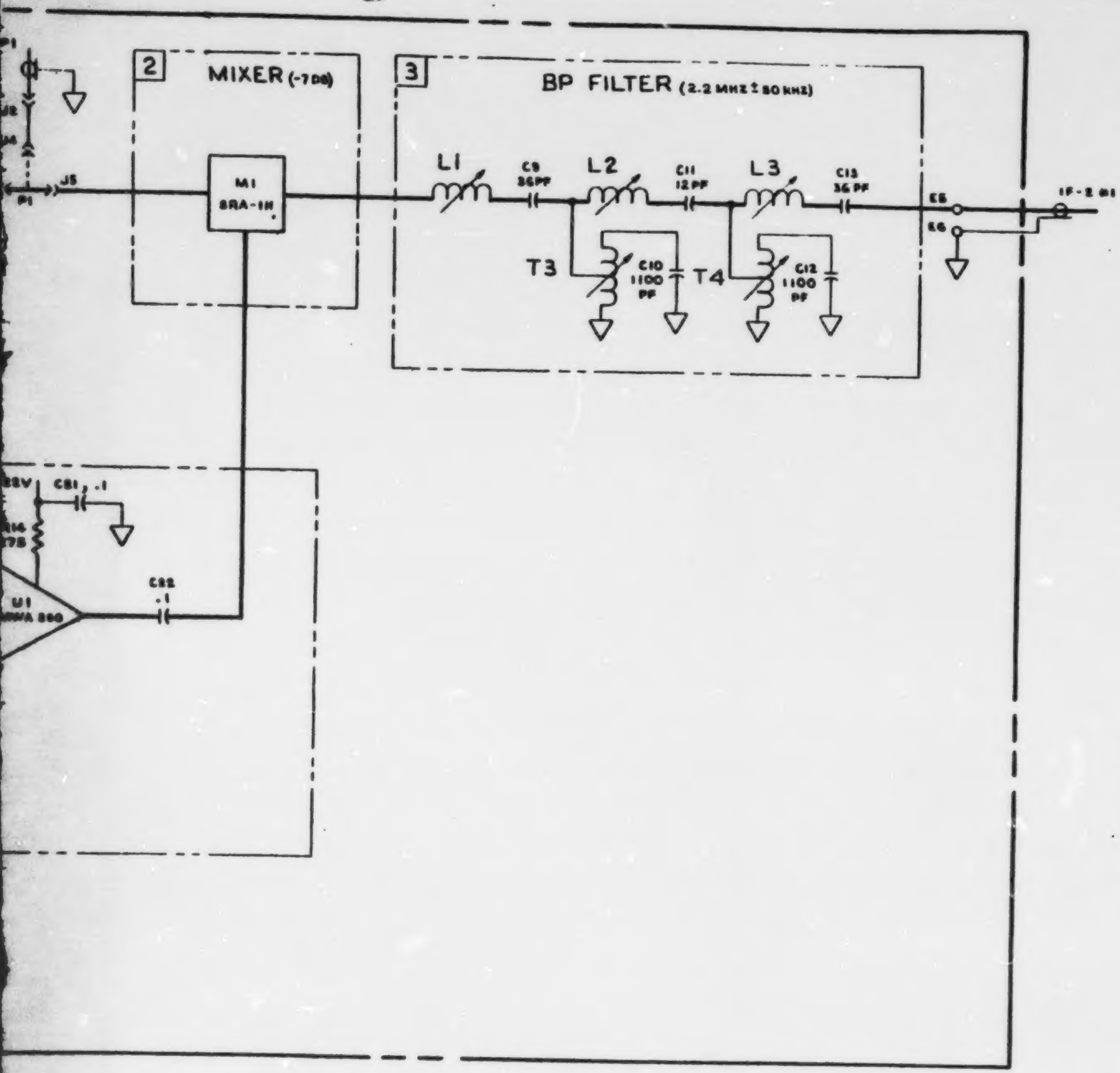

1
AMPLIFIER (6 DB)
+22V
C5
.01
T2
R3
220
C8
.01
C4
.01
R2
3.6K
Q1
2N5943
C7
33PF
C3
.01
R4
10
IF-1#1
E1
E2
C1
33PF
T1
C2
100PF
R1
1.5K
R5
390
C6
.1
TP1
J2
J4
J3
J5
P1
2
4
AMPLIFIER
+22V
C15
.1
T5
R6
1.8K
Q2
2N5943
C14
.01
LO-2#1
E3
E4
R7
560
R8
27
R9
220
C16
.1
C17
.01
R11
560
+22V
C18
.01
T6
R10
1.8K
Q3
2N5943
R12
50
R13
220
C19
.1
C20
.01
+22V
C21
.1
R14
275
U1
MWA 230
+22V
GND
J1
1
32
L4
1MH
C23
10
+
C24
.1

| HIGHEST DESIGNATION USED | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| C24 | E6 | J5 | L4 | M1 | P1 | Q3 | R14 | T6 | U1 |
| DESIGNATION NOT USED | | | | | | | | | |
| | | | | | | | | | |

NOTES:

1- ALL RESISTOR VALUES

2- ALL CAPACITOR VALUES
UNLESS OTHERWISE


P1
J2
J4
J5
P1
2
MIXER (-7DB)
M1
SRA-1H
3
BP FILTER (2.2 MHZ ± 80 KHZ)
L1
C9
36PF
L2
C11
12 PF
L3
C13
36 PF
T3
C10
1100
PF
T4
C12
1100
PF
E5
E6
IF-2 W1
22V
C81, .1
R16
75
U1
WA 860
C82
.1

ISTOR VALUES ARE IN OHMS.

PACITOR VALUES ARE IN MICROFARADS
OTHERWISE SPECIFIED.

BAYLY

SCHEMATIC DIAGRAM
SECOND CONVERSION CHAN. 1

## 2.3.4.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 3 | 4 | | | | | | |
| Adjusters | T3<br>T4<br>L1<br>L2<br>L3 | R12 | | | | | | |

a Block 3

The alignment is done according to specifications written in 2.3.4.4.

b Block 4

Adjust the gain "R12" for the optimum insertion loss in the second conversion.

### 2.3.4.4 SPECIFICATIONS

| | BLOCK # | | | | |
|---|---|---|---|---|---|
| | 3 | MODULE | | | |
| Impedance INPUT (ohms)<br>OUTPUT (ohms) | 50<br>50 | 50<br>50 | | | |
| Gain - Loss | | -10 | | | |
| Band-Pass (1 dB) (MHz) | 2.150 @ 2.250 | | | | |
| Insertion Loss (dB) (Center Bandwidth) | -5 | | | | |
| | | | | | |

## 2.3.5 SECOND CONVERSION DF CHANNEL # 2

a This module is located in the receiver unit.

b Its main functions are :

1 To convert the frequency from 30 MHz to 2.2 MHz.

2 To generate a LOCAL OSCILLATOR of 32.2 MHz.

c On the block diagram, we illustrate the form of the two signals on the spectrum analyser.

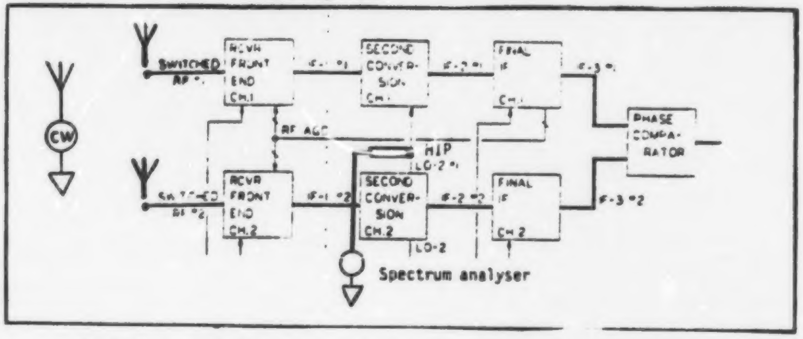
1 Photo IF-2 # 2 Refer to 2.3.4.

2 Photo LO-2 # 1

1 Initial conditions :

None

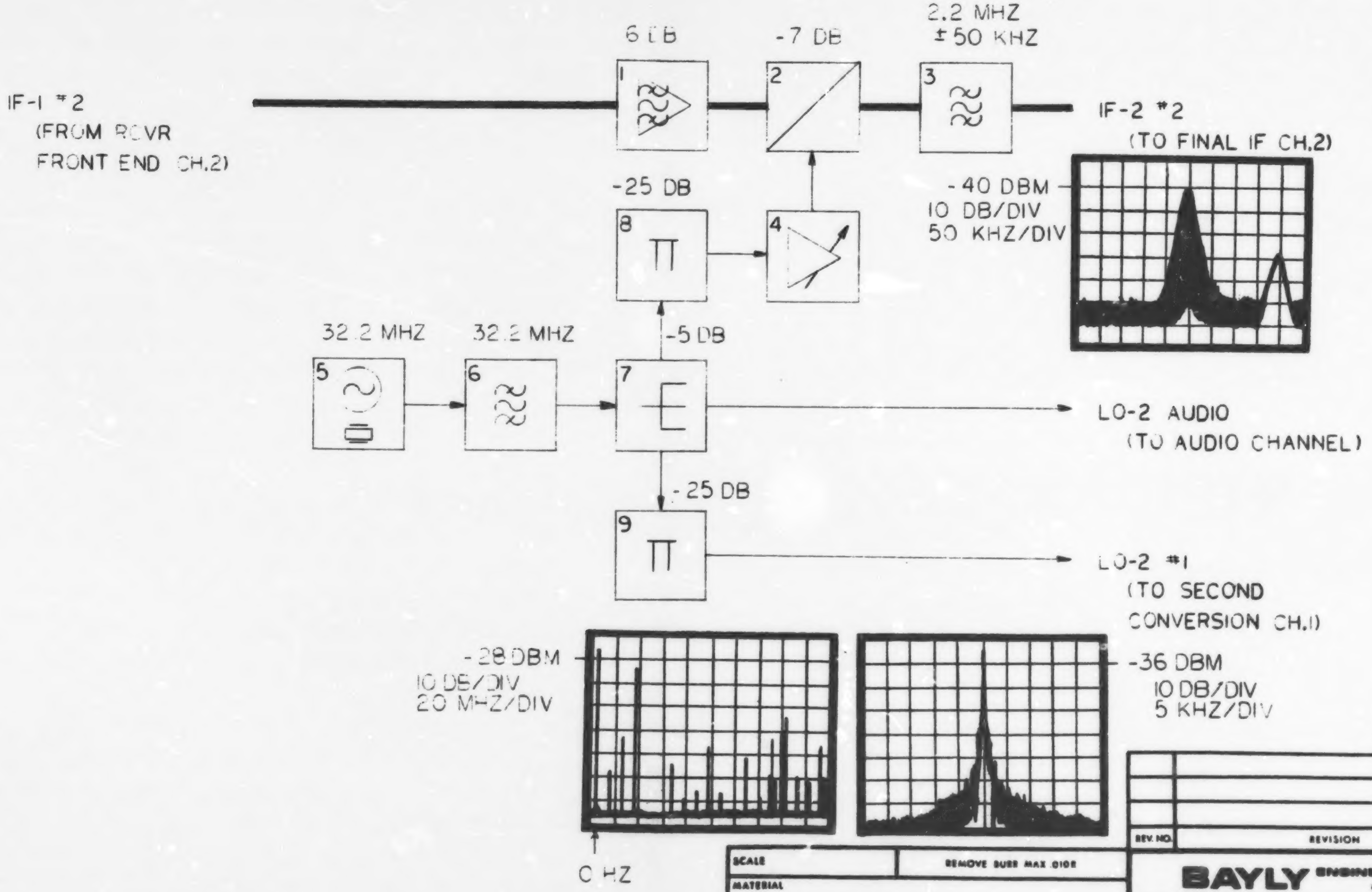
2 Set-up :


CW
SWITCHED RF #1
RCVR FRONT END CH.1
IF-1 #1
SECOND CONVER-SION CH.1
IF-2 #1
FINAL IF CH.1
IF-3 #1
RF AGC
HIP
LO-2 #1
PHASE COMPA-RATOR
SWITCHED RF #2
RCVR FRONT END CH.2
IF-1 #2
SECOND CONVER-SION CH.2
IF-2 #2
FINAL IF CH 2
IF-3 #2
LO-2
Spectrum analyser

Setting of Spectrum analyser for photo LO2-2 # 1

Bandwidth : 300 Hz
Scan width : 5 KHz/DIV
Attenuation : 0 dB
Scan time : 0.2 SEC/DIV
Video filter : 10 KHz
Signal strength : - 24 dBm

Bandwidth : 100 KHz
Scan width : 20 MHz
Attenuation : 0 dB
Scan time : 0.1 SEC/DIV
Video filter : 10 KHz
Signal strength fundamental : - 24 dBm


IF-1 #2
(FROM RCVR
FRONT END CH.2)
6 DB
-7 DB
2.2 MHZ
± 50 KHZ
1
2
3
IF-2 #2
(TO FINAL IF CH.2)
-25 DB
8
4
-40 DBM
10 DB/DIV
50 KHZ/DIV
32.2 MHZ
32.2 MHZ
-5 DB
5
6
7
LO-2 AUDIO
(TO AUDIO CHANNEL)
-25 DB
9
LO-2 #1
(TO SECOND
CONVERSION CH.1)
-28 DBM
10 DB/DIV
20 MHZ/DIV
-36 DBM
10 DB/DIV
5 KHZ/DIV
0 HZ

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE

REMOVE BURR MAX .010R

MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

DRAWN BY S.B.

DATE 83-1-20

CHECKED BY

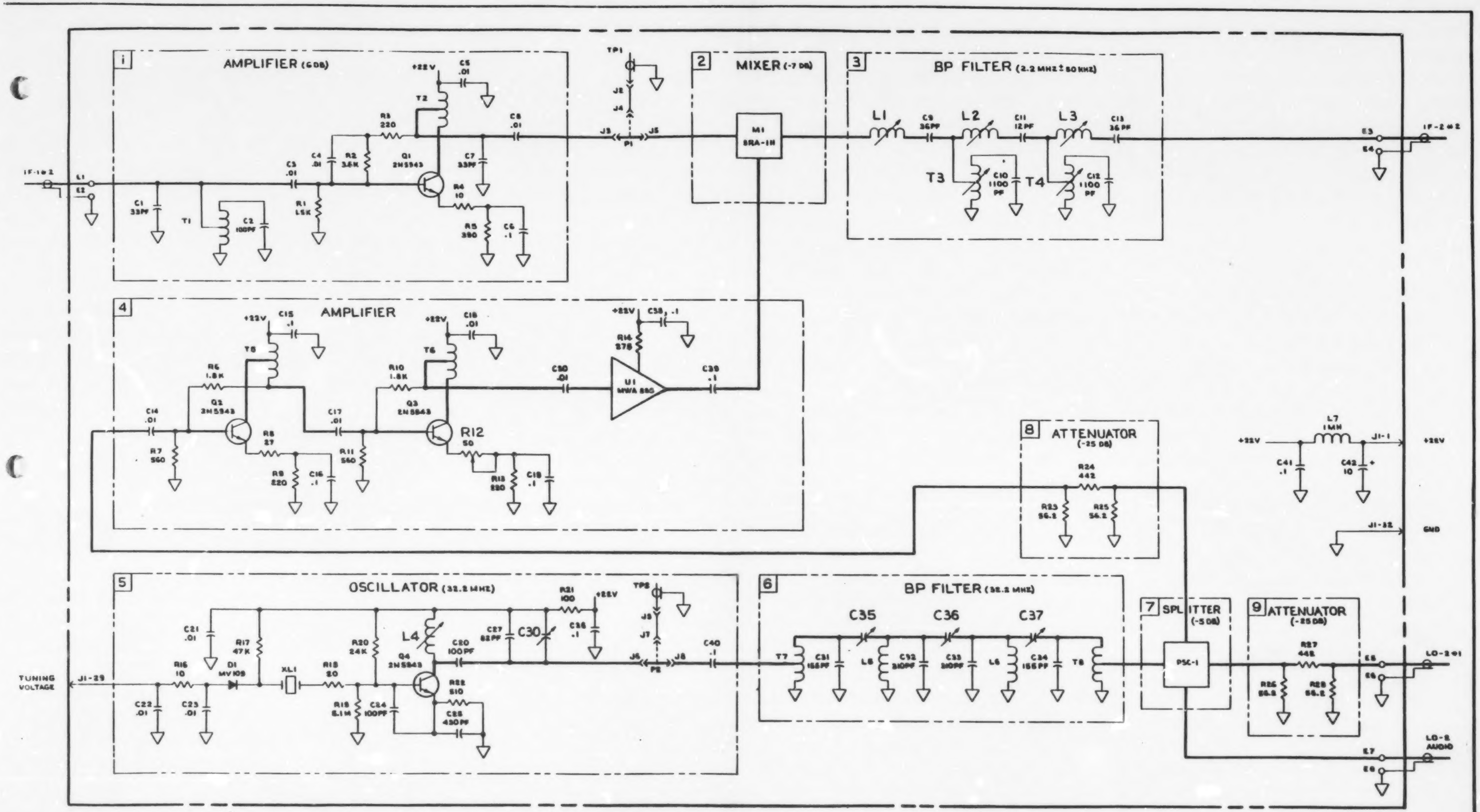
APPROVED BY

**BAYLY** ENGINEERING LTD
a member of

TITLE BLOCK DIAGRAM
SECOND CONVERSION CH.2

DRAWING NO 66-0643.028 516.BD-B

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.


1 AMPLIFIER (6 DB)
2 MIXER (-7 DB)
M1 SRA-1H
3 BP FILTER (2.2 MHZ ± 50 KHZ)
4 AMPLIFIER
U1 MWA 520
5 OSCILLATOR (32.2 MHZ)
6 BP FILTER (32.2 MHZ)
7 SPLITTER (-5 DB)
PSC-1
8 ATTENUATOR (-25 DB)
9 ATTENUATOR (-25 DB)
IF-1 #2
IF-2 #2
LO-2 #1
LO-2 AUDIO
TUNING VOLTAGE
J1-29
J1-1
J1-32
+22V
GND
TP1
TP2
Q1 2N5943
Q2 2N5943
Q3 2N5943
Q4 2N5943
D1 MV109
XL1
L1
L2
L3
L4
L7 1MH
T3
T4
R12 50
C30
C35
C36
C37

| HIGHEST DESIGNATION USED | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C41 | D1 | E8 | J8 | L7 | M1 | P2 | PSC 1 | Q4 | R28 | T8 | U1 | XL1 |
| DESIGNATION NOT USED | | | | | | | | | | | | |
| | | | | | | | | | R16 | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

2-49

BAYLY

SCHEMATIC DIAGRAM
SECOND CONVERSION CHAN. 2

56-0643.028 SIS.CD

### 2.3.5.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 3 | 4 | 5 | 6 | | | | |
| Adjusters | L1 | | L4 | C35 | | | | |
| | L2 | R12 | | C36 | | | | |
| | L3 | | C30 | C37 | | | | |
| | T3 | | | | | | | |
| | T4 | | | | | | | |

a The alignment of Block # 3 and # 6 (filters) is done according to specifications written in 2.3.5.4.

b Block 4

Adjust the gain "R12" for the optimum insertion loss in that second conversion.

c Block 5

Adjust the Tuning elements (L4, C30) for maximum amplitude (32.2 MHz) at the output of Block 5.

### 2.3.5.4 SPECIFICATIONS

| | BLOCK | | | | |
|---|---|---|---|---|---|
| | 3 | 6 | | | |
| Impedance INPUT (ohms)<br>OUTPUT (ohms) | 50<br>50 | 50<br>50 | | | |
| Band-Pass (3 dB) (KHz) | ± 50 | About ± 400 | | | |
| Insertion Loss (dB) (Center Bandwidth) | -5 | -10 | | | |
| Center Frequency (MHz) | 2.2 | 32.2 | | | |
| | | | | | |

## 2.3.6 FINAL IF CHANNEL 1

a This module is located in the receiver unit, and is partially located outside the front part of the receiver.

b Its main functions are :

1 To convert the frequency from 2.2 MHz to 200 KHz.

2 To filter the "Frequency Spectrum" to a 15 KHz band.

3 To maintain a constant amplitude of the signal at the output.

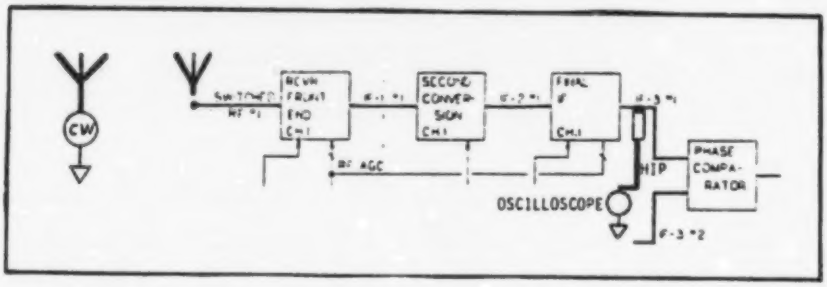
4 To give the information to feed the "RF Pads".

c On the block diagram, we illustrate the form of the signal at the module output as seen on the oscilloscope.

1 Initial conditions :

Tuning : 118.250 MHz
Field strength : 1 mV/m
(received)

2 Set-up :

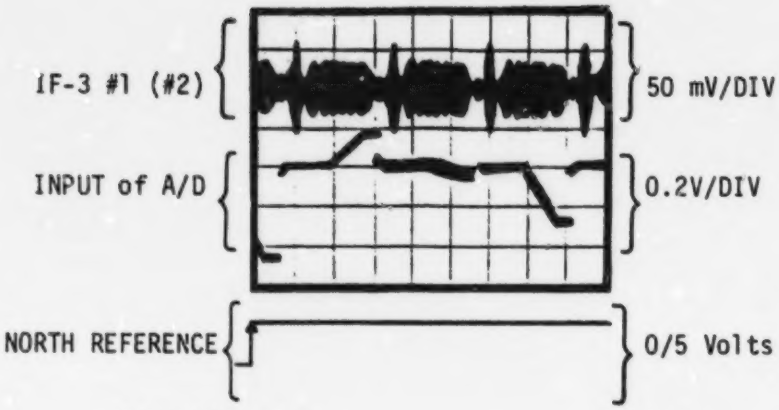

CW
SWITCHED RF #1
RCVR FRONT END CH1
IF-1 #1
SECOND CONVERSION CH1
IF-2 #1
FINAL IF CH.1
IF-3 #1
RF AGC
HIP
PHASE COMPARATOR
OSCILLOSCOPE
IF-3 #2

Setting of spectrum analyser

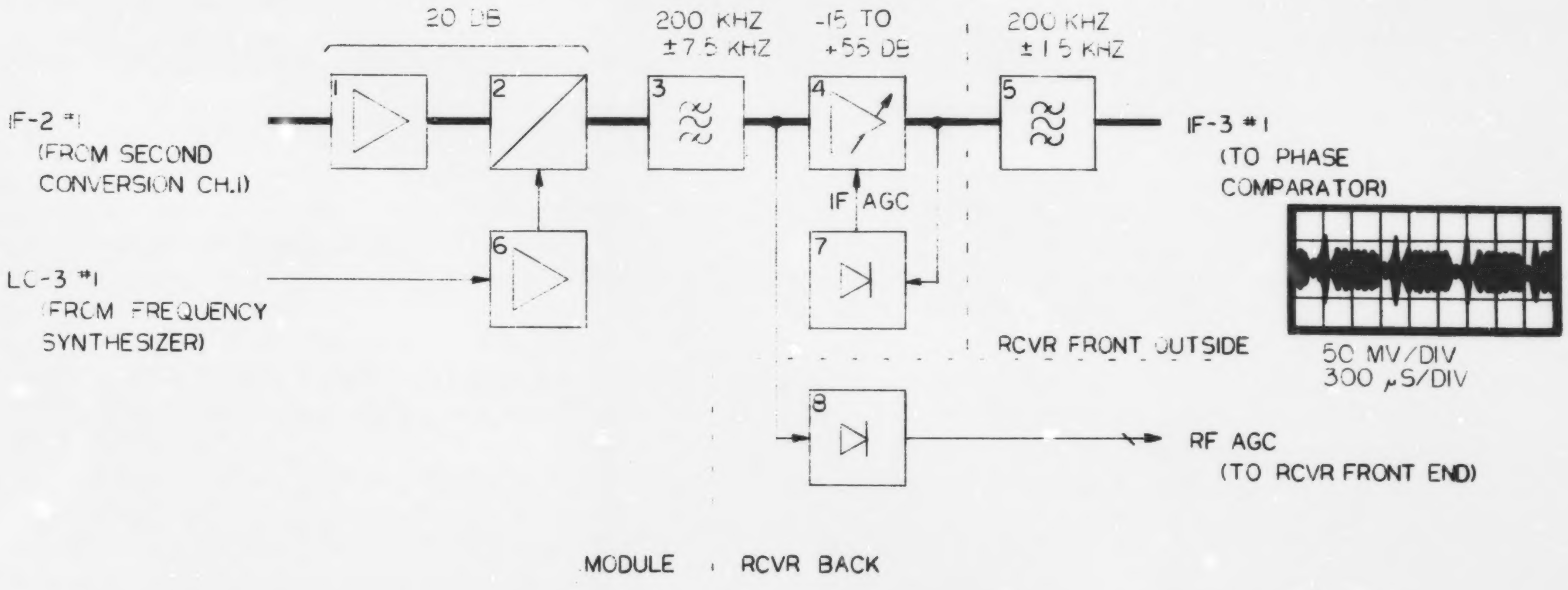
SETTING OF OSCILLOSCOPE

Horizontal : 300 us/DIV
Vertical : 50 mV/DIV
Signal strength : 40 mV Peak
External trigger : North reference

d Timing between IF-3 # 1, North Reference
(# 2)
and INPUT DFA/D converter.


IF-3 #1 (#2)
INPUT of A/D
NORTH REFERENCE
50 mV/DIV
0.2V/DIV
0/5 Volts

| Identification | Location |
|---|---|
| IF-3 # 1 (#2) | OUTPUT FINAL IF CH1<br>(CH2) |
| INPUT A/D | On data acquisition board at the input of A/D converter Pin 14. |
| NORTH REFERENCE | On front panel of timing board "North Reference" or TP4 of the P.C.B. |


20 DB
200 KHZ
±7.5 KHZ
-15 TO
+55 DB
200 KHZ
±1.5 KHZ
1
2
3
4
5
IF-2 #1
(FROM SECOND
CONVERSION CH.1)
IF-3 #1
(TO PHASE
COMPARATOR)
IF AGC
6
7
LO-3 #1
(FROM FREQUENCY
SYNTHESIZER)
RCVR FRONT OUTSIDE
50 MV/DIV
300 μS/DIV
8
RF AGC
(TO RCVR FRONT END)
MODULE
RCVR BACK

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

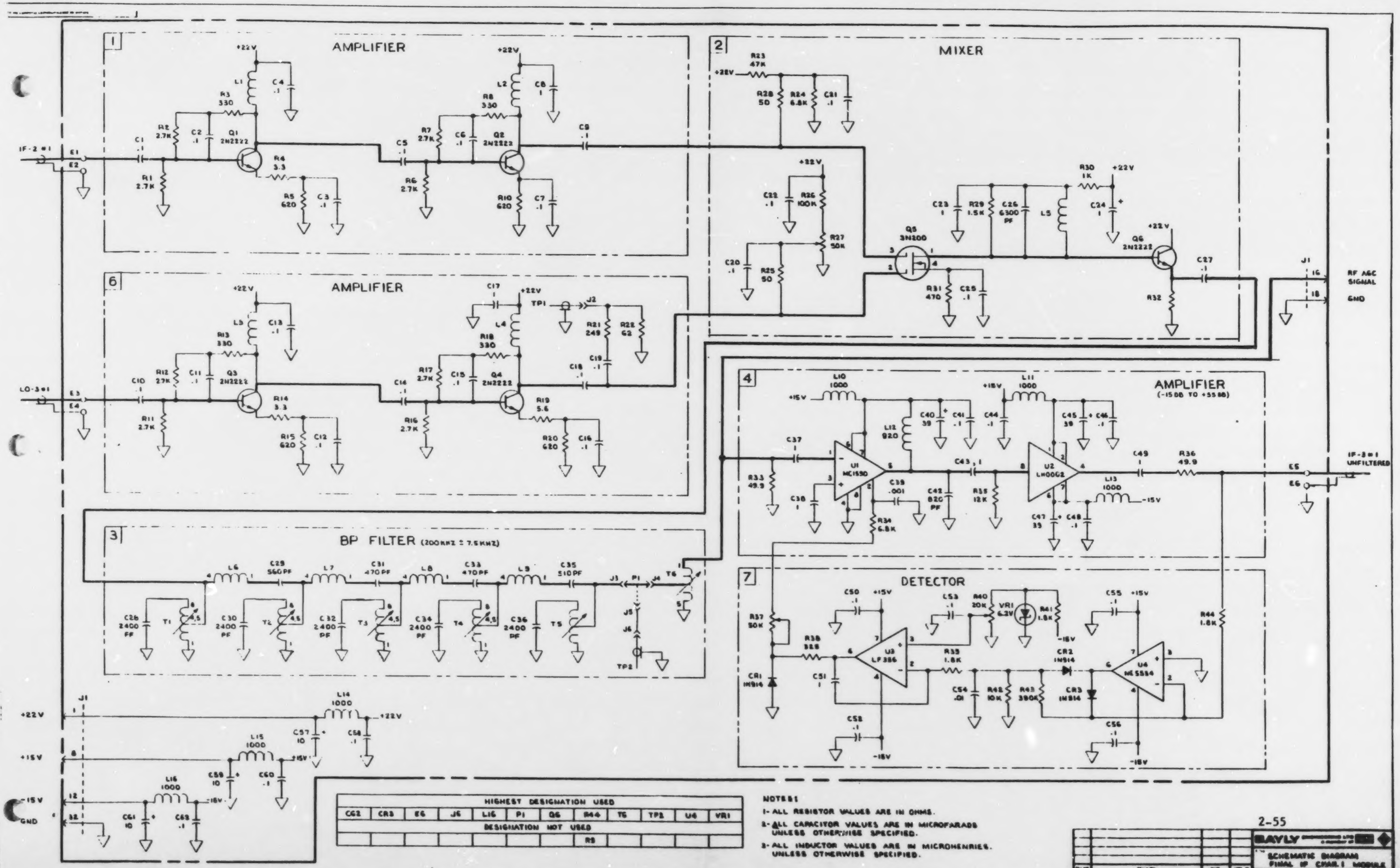
SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
FINAL IF CH.1

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMALS ± ANGLES ± ° | DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|---|
| | S.B. | 83-1-20 | | | 66-0643.028 95.BD-B |


1
AMPLIFIER
+22V
L1
C4 .1
R3 330
R2 2.7K
C2 .1
Q1 2N2222
IF-2 #1
E1
E2
C1 .1
R1 2.7K
R4 3.3
R5 620
C3 .1
L2
C8 1
R8 330
R7 2.7K
C6 .1
Q2 2N2222
C5 .1
R6 2.7K
R10 620
C7 .1
C9 .1
2
MIXER
R23 47K
+22V
R28 50
R24 6.8K
C21 .1
C22 .1
R26 100K
R27 50K
C20 .1
R25 50
Q5 3N200
R31 470
C25 .1
C23 1
R29 1.5K
C26 6300 PF
L5
R30 1K
C24 1
Q6 2N2222
C27 .1
R32
J1
16 RF AGC SIGNAL
18 GND
6
AMPLIFIER
L3
C13 .1
R13 330
R12 2.7K
C11 .1
Q3 2N2222
LO-3 #1
E3
E4
C10 .1
R11 2.7K
R14 3.3
R15 620
C12 .1
C17 1
TP1
J2
R21 249
R22 62
L4
R18 330
R17 2.7K
C15 .1
Q4 2N2222
C14 .1
R16 2.7K
C18 .1
C19 .1
R19 5.6
R20 620
C16 .1
3
BP FILTER (200KHZ ± 7.5KHZ)
L6
C29 560PF
L7
C31 470PF
L8
C33 470PF
L9
C35 510PF
J3
P1
J4
T6
C28 2400 PF
T1
C30 2400 PF
T2
C32 2400 PF
T3
C34 2400 PF
T4
C36 2400 PF
T5
J5
J6
TP2
4
AMPLIFIER (-15DB TO +55DB)
L10 1000
+15V
L12 820
C40 39
C41 .1
C44 .1
L11 1000
C45 39
C46 .1
C37
U1 MC1590
R33 49.9
C38 1
C39 .001
R34 6.8K
C43 .1
C42 820 PF
R35 12K
U2 LH0062
C47 39
C48 .1
L13 1000
-15V
C49 1
R36 49.9
E5
E6
IF-3 #1 UNFILTERED
7
DETECTOR
C50 .1
R37 50K
R38 332
U3 LF356
CR1 1N914
C51 1
C52 .1
-15V
L53 .1
R40 20K
VR1 6.2V
R41 1.8K
R39 1.8K
CR2 1N914
C54 .01
R42 10K
R43 390K
CR3 1N914
C55 .1
U4 NE5534
C56 .1
R44 1.8K
J1
+22V
L14 1000
C57 10
C58 .1
+15V
L15 1000
C59 10
C60 .1
-15V
L16 1000
C61 10
C62 .1
GND
32

| HIGHEST DESIGNATION USED | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C62 | CR3 | E6 | J6 | L16 | P1 | Q6 | R44 | T6 | TP2 | U4 | VR1 |
| DESIGNATION NOT USED | | | | | | | | | | | |
| | | | | | | | R9 | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

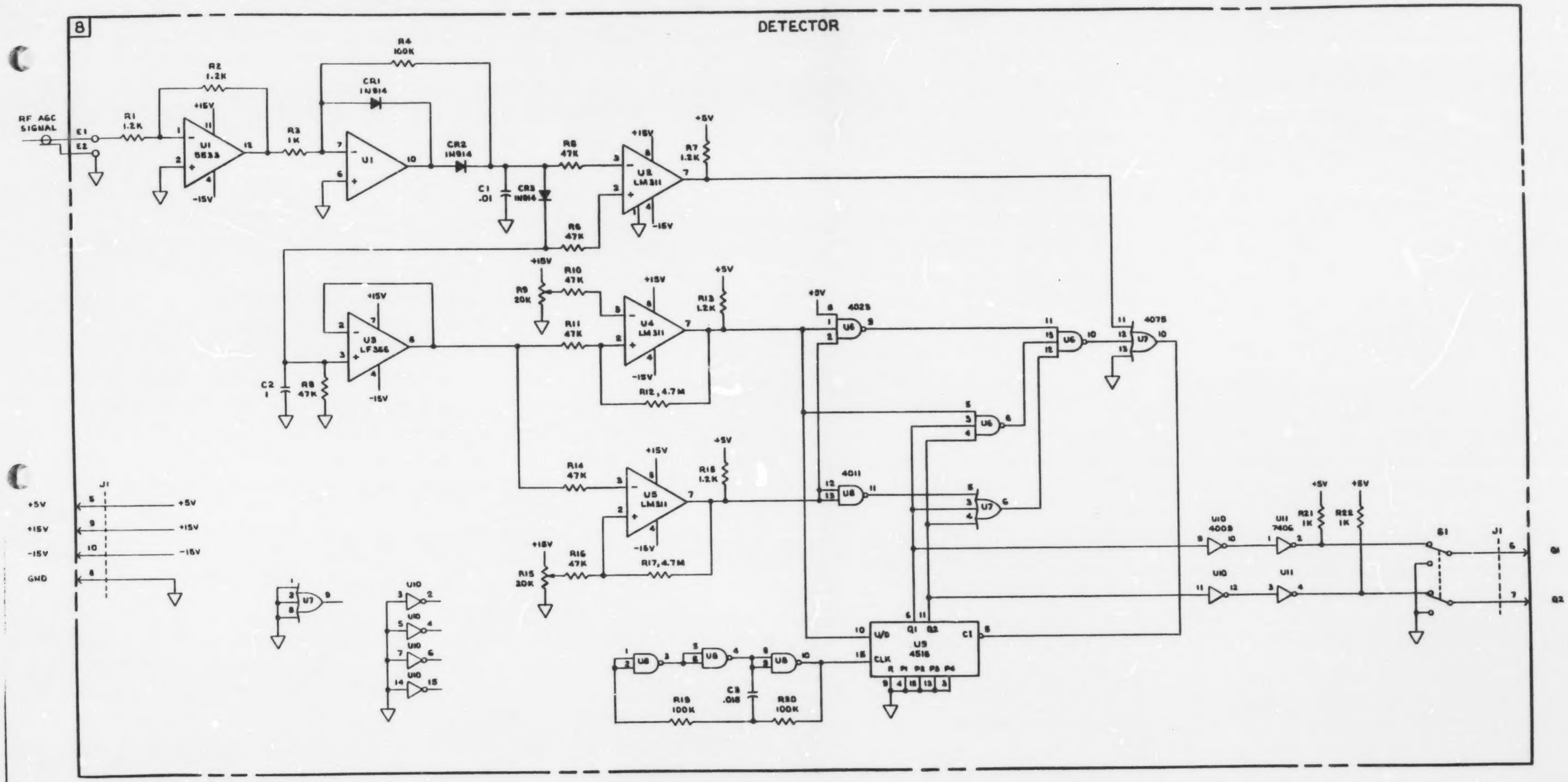
2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES. UNLESS OTHERWISE SPECIFIED.

BAYLY

SCHEMATIC DIAGRAM
FINAL IF CHAN.1 MODULE

56-0849-088 195.C0


8
DETECTOR
RF AGC SIGNAL
E1
E2
R1 1.2K
R2 1.2K
U1 5533
+15V
-15V
R3 1K
R4 100K
CR1 1N914
U1
CR2 1N914
C1 .01
CR3 1N914
R5 47K
R6 47K
U2 LM311
+5V
R7 1.2K
U3 LF356
C2 1
R8 47K
R9 20K
R10 47K
R11 47K
U4 LM311
R12, 4.7M
R13 1.2K
U6 4023
U6
U7 4075
U6
U8 4011
U7
R14 47K
U5 LM311
R15 20K
R16 47K
R17, 4.7M
R18 1.2K
J1
+5V
+15V
-15V
GND
U7
U10
U10 4009
U11 7406
R21 1K
R22 1K
S1
Q1
Q2
U9 4516
U/D
CLK
Q1 Q2
CI
R P1 P2 P3 P4
U8
R19 100K
C3 .018
R20 100K

| IC'S SUPPLY DISTRIBUTION | | |
|---|---|---|
| DESIGNATION | GND | +5V |
| U6, U7, U8, U11 | PIN 7 | PIN 14 |
| U9 | PIN 8 | PIN 16 |
| U10 | PIN 8 | PIN 1 + 16 |

| HIGHEST DESIGNATION USED | | | | | | |
|---|---|---|---|---|---|---|
| C3 | CR3 | E2 | J1 | R22 | S1 | U11 |
| DESIGNATION NOT USED | | | | | | |
| | | | | | | |

NOTES:

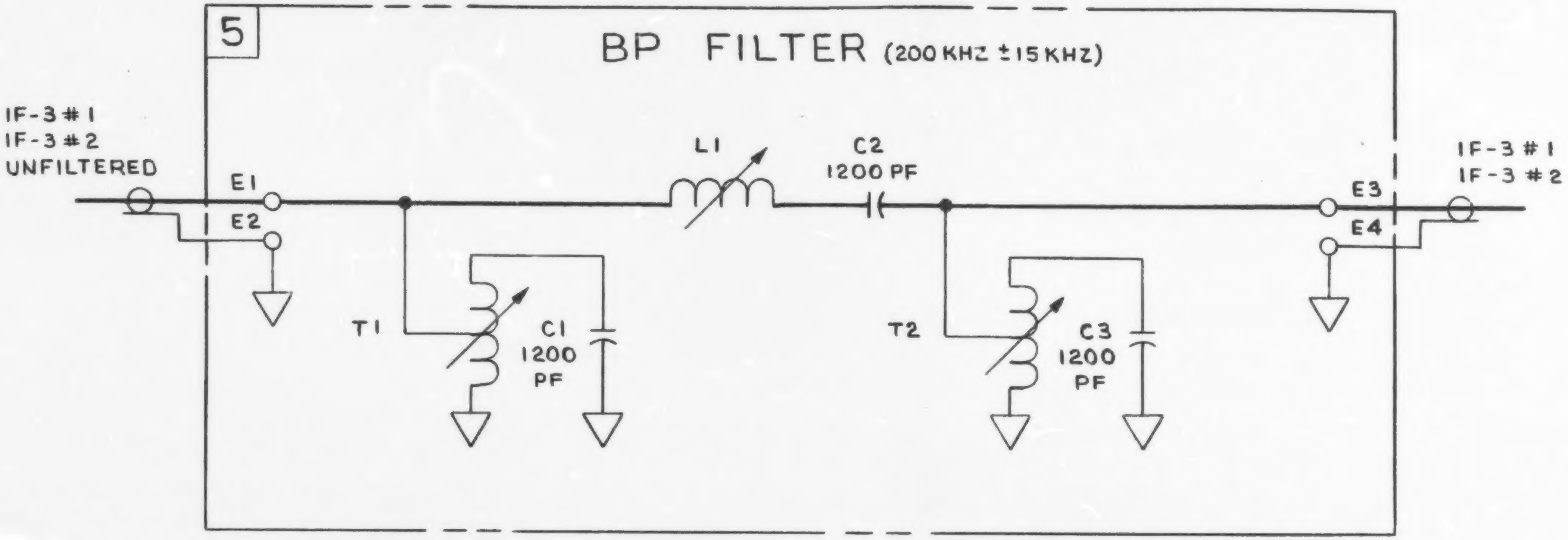
1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

BAYLY

SCHEMATIC DIAGRAM
FINAL IF CHAN I RCVR BACK

DWG NO 66-0648.888 23/ CD


5
BP FILTER (200 KHZ ±15 KHZ)
IF-3 #1
IF-3 #2
UNFILTERED
E1
E2
L1
C2
1200 PF
E3
E4
IF-3 #1
IF-3 #2
T1
C1
1200
PF
T2
C3
1200
PF

| REV NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE
REMOVE BURR MAX 010R
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS : :
DRAWN BY
DATE 83-01-02
CHECKED BY
APPROVED BY

**BAYLY** ENGINEERING LTD a member of AEG

TITLE SCHEMATIC DIAGRAM
FINAL IF CHAN 1+2 (RCVR FRONT OUTSIDE)

DRAWING NO. 66-0643.035 327.CD -B

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

## 2.3.6.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 5 | 7 | 8 | | | |
| Adjusters | | T1 | T1 | | | | | |
| | R27 | T2 | T2 | | | | | |
| | | T3 | L1 | | | | | |
| | | T4 | | R40 | R10 | | | |
| | | T5 | | R37 | R16 | | | |
| | | T6 | | | | | | |

a The alignment of block # 3 and # 5 (filters) is done according to specifications written in 2.3.6.4.

b Block 2

Adjust the gain "R27" for the optimum insertion loss in that conversion.

c Block 7

1 Adjust the output level (output of block 4) at - 20 dBm with R40.

2 Adjust the dynamic range of the AGC with R37.

d Block 8

1 Inject at the input of "Second Conversion CH. 1" (IF-1#1) a signal CW of - 40 dBm.

Adjust the upper threshold for the RF AGC "R16" to get a level "1" (Edge of "0" and "1") at Pin 7 (output) of its own comparator.

2 Inject at the input of "Second Conversion CH. 1" (IF-1#1) a signal CW of - 55 dBm.

Adjust the lower threshold for the RF AGC "R10" to get a level "0" (Edge of "1" and "0") at pin 7 (output) of its own comparator.

## 2.3.6.4 SPECIFICATIONS

| | BLOCK # | | | | |
|---|---|---|---|---|---|
| | 3 | 5 | | | |
| Impedance INPUT (ohms) | 50 | 50 | | | |
| OUTPUT (ohms) | 50 | 50 | | | |
| Band-Pass (1 dB) (KHz) | | ± 11 | | | |
| (3 dB) (KHz) | ± 7.5 | ± 15 | | | |
| (50 dB) (KHz) | | 114 @ 328 | | | |
| (80 dB) (KHz) | ±18 | | | | |
| Insertion Loss (Center Bandwidth) | 4 | 1 | | | |
| Center Frequency | 200 | 200 | | | |
| | | | | | |

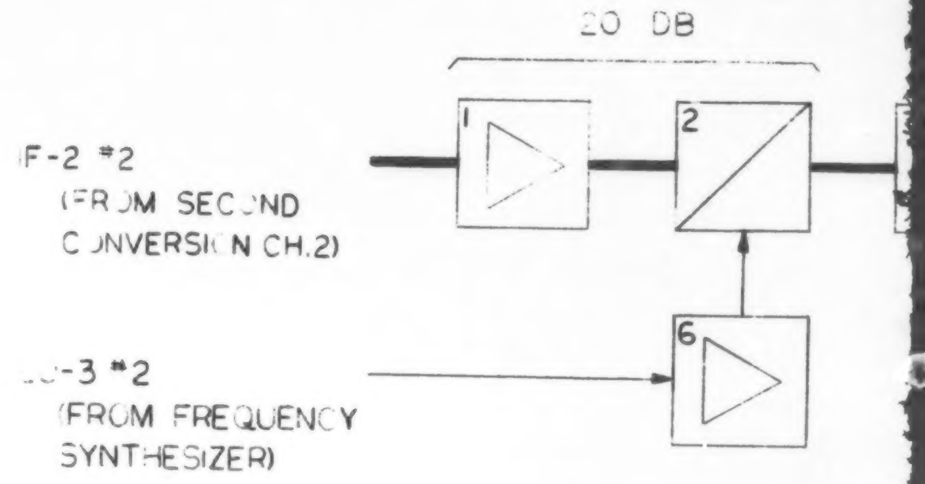
### 2.3.7 FINAL IF CHANNEL 2

a This module is located in the receiver unit, and is partially located outside the front part of the receiver.

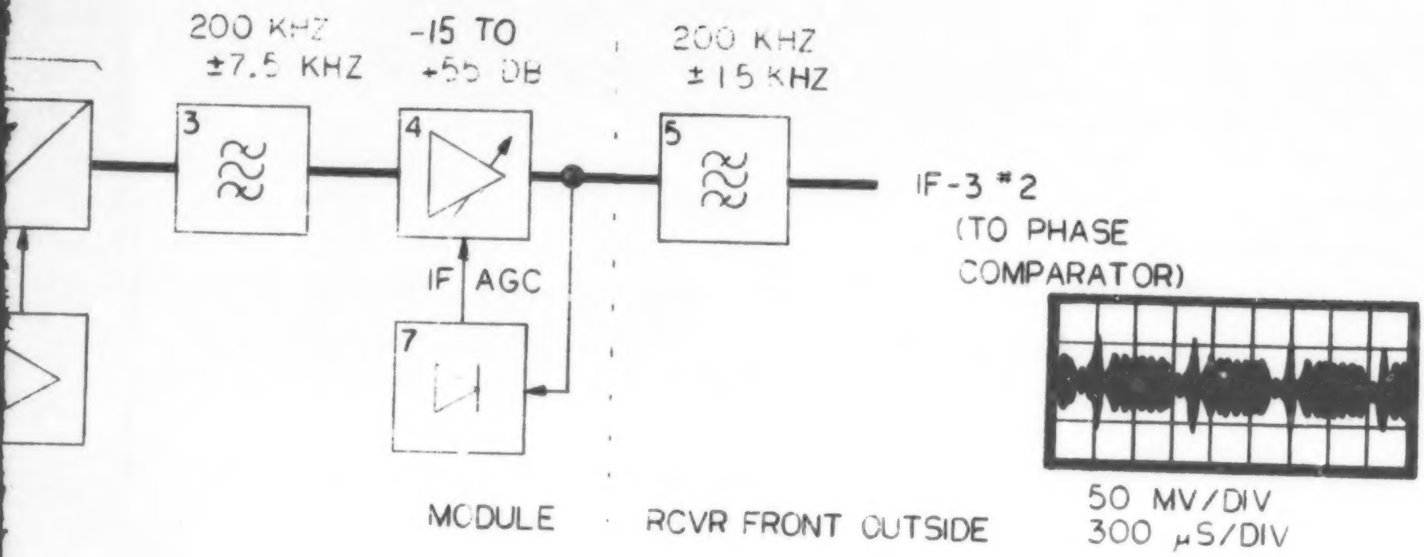
b Its main functions are :

1. To convert the frequency from 2.2 MHz to 200 KHz.
2. To filter the "frequency Spectrum" to a 15 KHz band.
3. To maintain a constant amplitude at the output.

c On the block diagram, we illustrate the form of the signal at the module output as seen on an oscilloscope. Refer to 2.3.6 c for the initial conditions and set-up.


20 DB
1
2
6
IF-2 #2
(FROM SECOND
CONVERSION CH.2)
-3 #2
(FROM FREQUENCY
SYNTHESIZER)

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document
neither used, copied, reproduced or otherwise dea
nor its contents communicated to others.


200 KHZ
±7.5 KHZ
-15 TO
+55 DB
200 KHZ
±15 KHZ
3
4
5
7
IF AGC
IF-3 #2
(TO PHASE
COMPARATOR)
MODULE
RCVR FRONT OUTSIDE
50 MV/DIV
300 μS/DIV

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

**BAYLY** ENGINEERING LTD
a member of

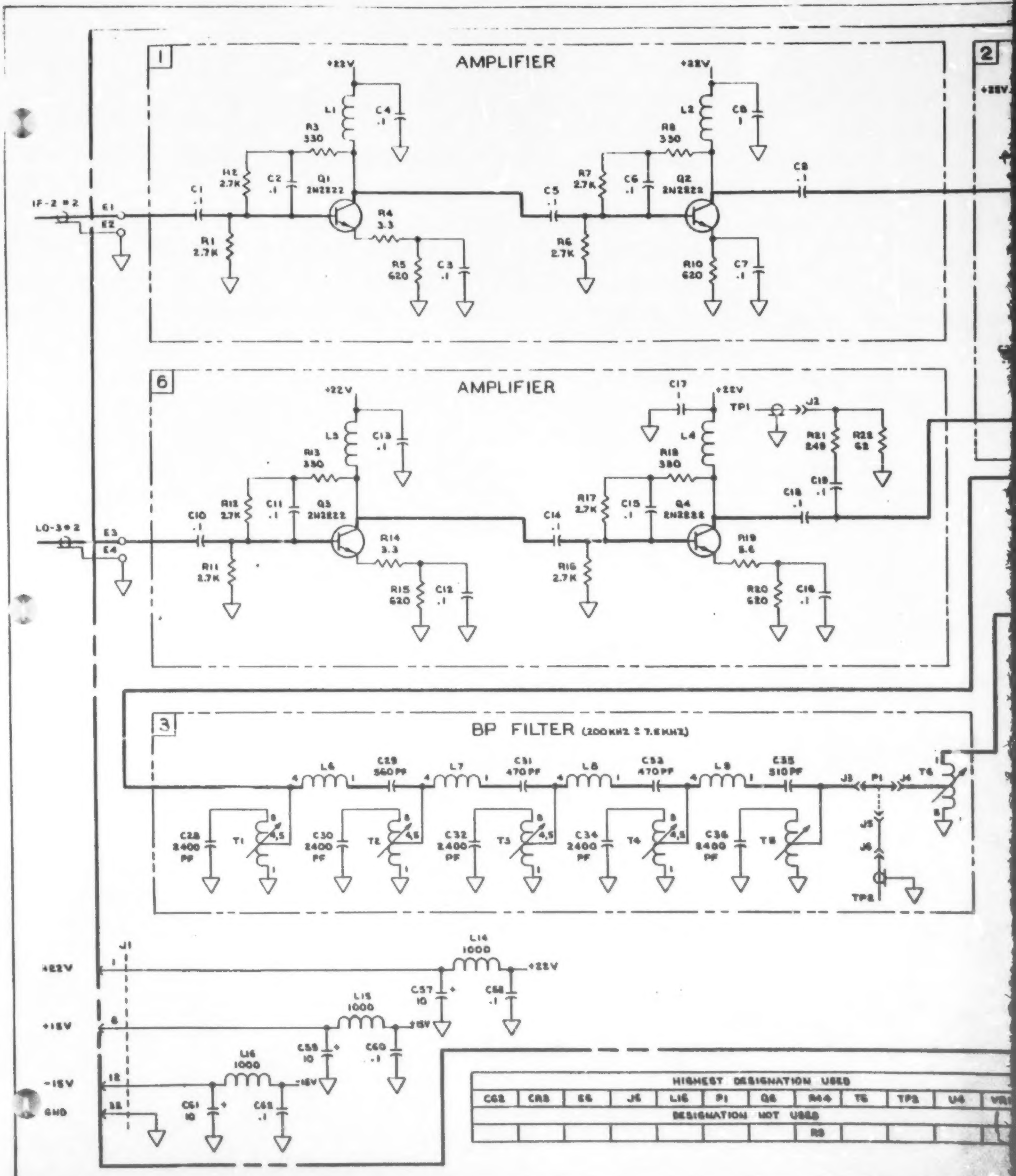
TITLE
BLOCK DIAGRAM
FINAL IF CH.2

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

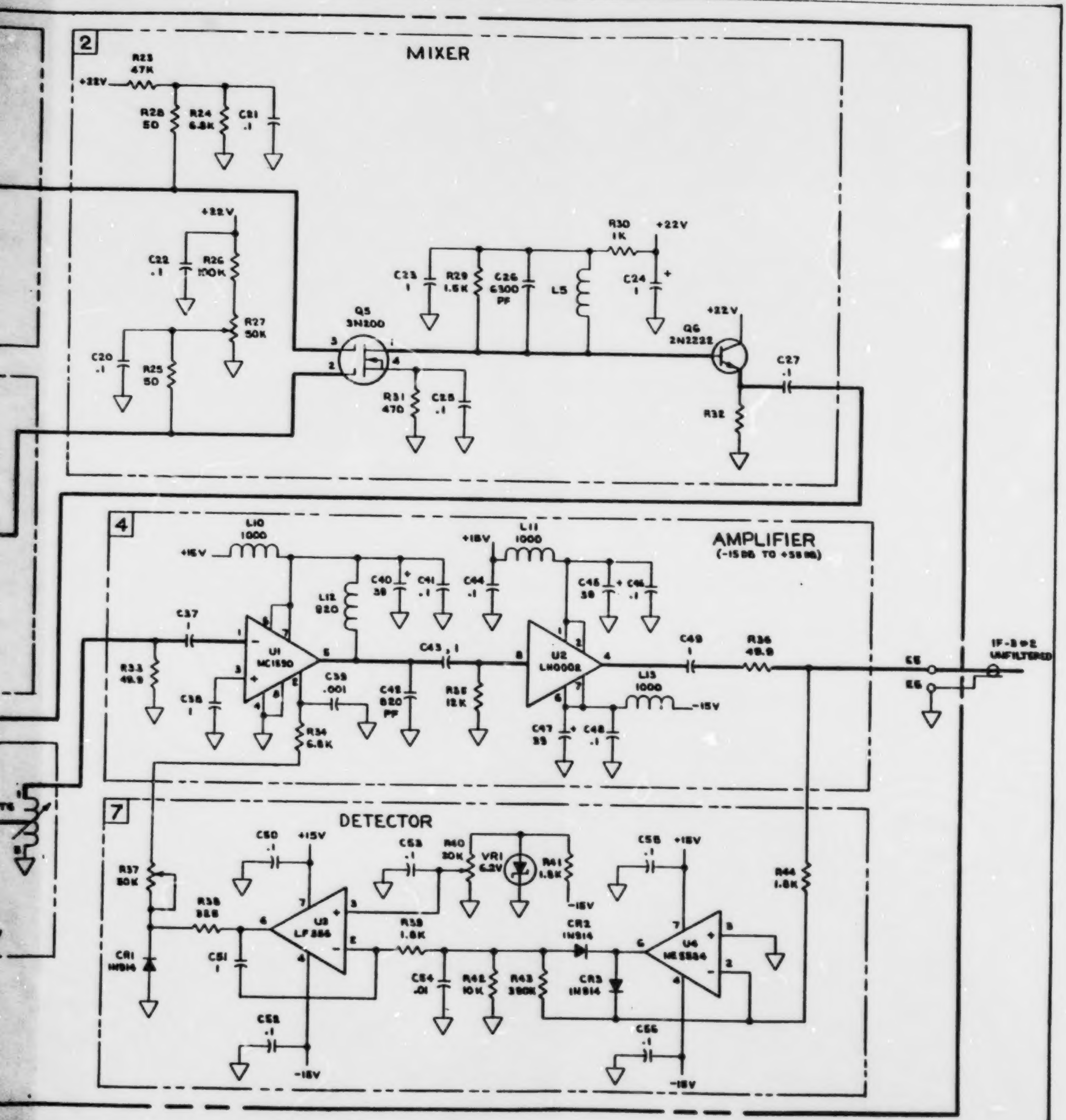
document may be
dealt with.

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ±

DRAWN BY S.B.
DATE 83-1-20
CHECKED BY
APPROVED BY
DRAWING NO. 66-0643.035 326.BD-B


1
AMPLIFIER
+22V
L1
C4 .1
R3 330
R2 2.7K
C2 .1
Q1 2N2222
C1 .1
IF-2 #2
E1
E2
R1 2.7K
R4 3.3
R5 620
C3 .1
+22V
L2
C8 1
R8 330
R7 2.7K
C6 .1
Q2 2N2222
C5 .1
R6 2.7K
R10 620
C7 .1
C9 .1
2
+22V
6
AMPLIFIER
+22V
L3
C13 .1
R13 330
R12 2.7K
C11 .1
Q3 2N2222
C10 .1
LO-3 #2
E3
E4
R11 2.7K
R14 3.3
R15 620
C12 .1
C17
+22V
TP1
J2
L4
R18 330
R17 2.7K
C15 .1
Q4 2N2222
C14 .1
R16 2.7K
R19 5.6
R20 620
C16 .1
R21 249
R22 62
C19 .1
C18 .1
3
BP FILTER (200KHZ ± 7.6KHZ)
L6
C29 560PF
L7
C31 470PF
L8
C33 470PF
L9
C35 510PF
J3
P1
J4
T6
C28 2400 PF
T1
C30 2400 PF
T2
C32 2400 PF
T3
C34 2400 PF
T4
C36 2400 PF
T5
J5
J6
TP2
J1
+22V
L14 1000
+22V
C57 10
C58 .1
+15V
L15 1000
15V
C59 10
C60 .1
-15V
L16 1000
-15V
C61 10
C62 .1
GND
1
6
12
32

| HIGHEST DESIGNATION USED | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C62 | CR3 | E6 | J6 | L16 | P1 | Q6 | R44 | T6 | TP2 | U4 | VR |
| DESIGNATION NOT USED | | | | | | | | | | | |
| | | | | | | | R9 | | | | |


2
MIXER
+22V
R23 47K
R28 50
R24 6.8K
C21 .1
+22V
C22 .1
R26 100K
R27 50K
C20 .1
R25 50
Q5 3N200
3
2
1
4
R31 470
C25 .1
C23 1
R29 1.5K
C26 6300 PF
L5
R30 1K
+22V
C24 1
+
+22V
Q6 2N2222
C27 .1
R32
4
L10 1000
+15V
+15V
L11 1000
AMPLIFIER
(-15DB TO +58DB)
L12 820
C40 39
C41 .1
C44 .1
C45 39
C46 .1
C37 1
R33 49.9
U1 MC1590
C38 1
R34 6.8K
C39 .001
C43 .1
C42 820 PF
R35 12K
U2 LH0002
C47 39
C48 .1
L13 1000
-15V
C49 1
R36 49.9
E5
E6
IF-3 #2 UNFILTERED
7
DETECTOR
C50 .1
+15V
R37 50K
R38 388
CR1 1N914
U3 LF356
C51 1
C52 .1
-15V
C53 .1
R40 20K
VR1 6.2V
R41 1.5K
-15V
R39 1.5K
C54 .01
R42 10K
R43 390K
CR2 1N914
CR3 1N914
C55 .1
+15V
U4 NE5534
C56 .1
-15V
R44 1.8K

| | |
|---|---|
| U4 | VR1 |
| | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

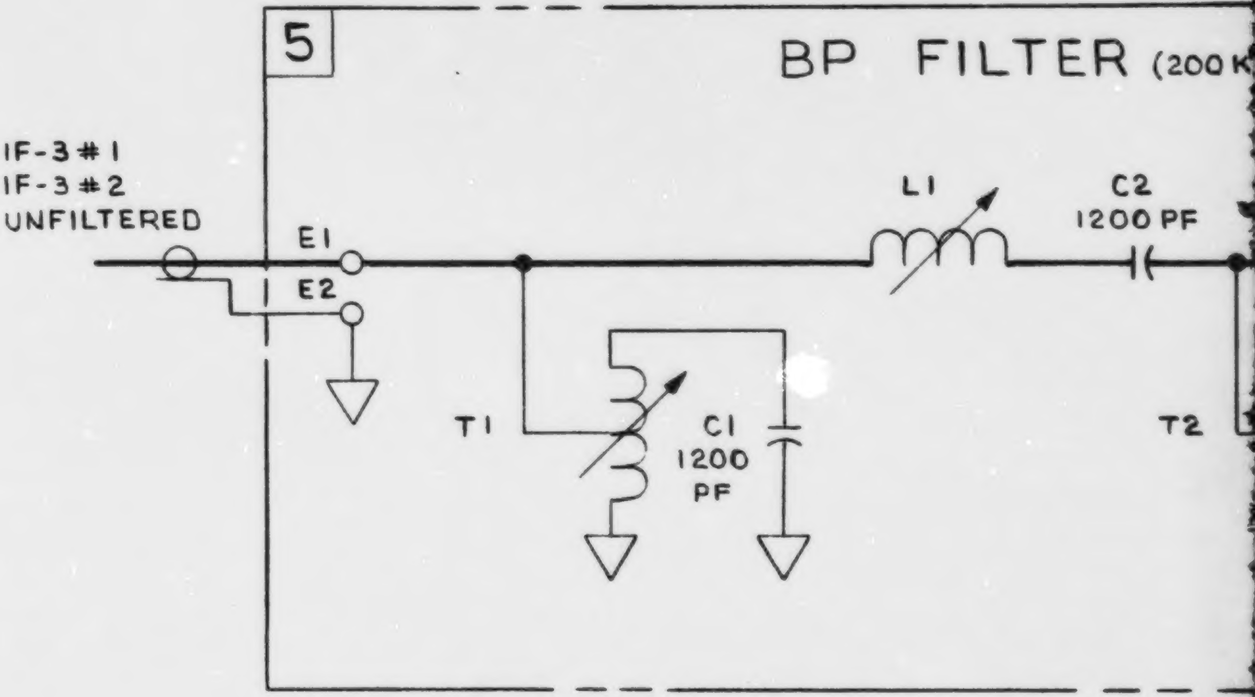
2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES. UNLESS OTHERWISE SPECIFIED.

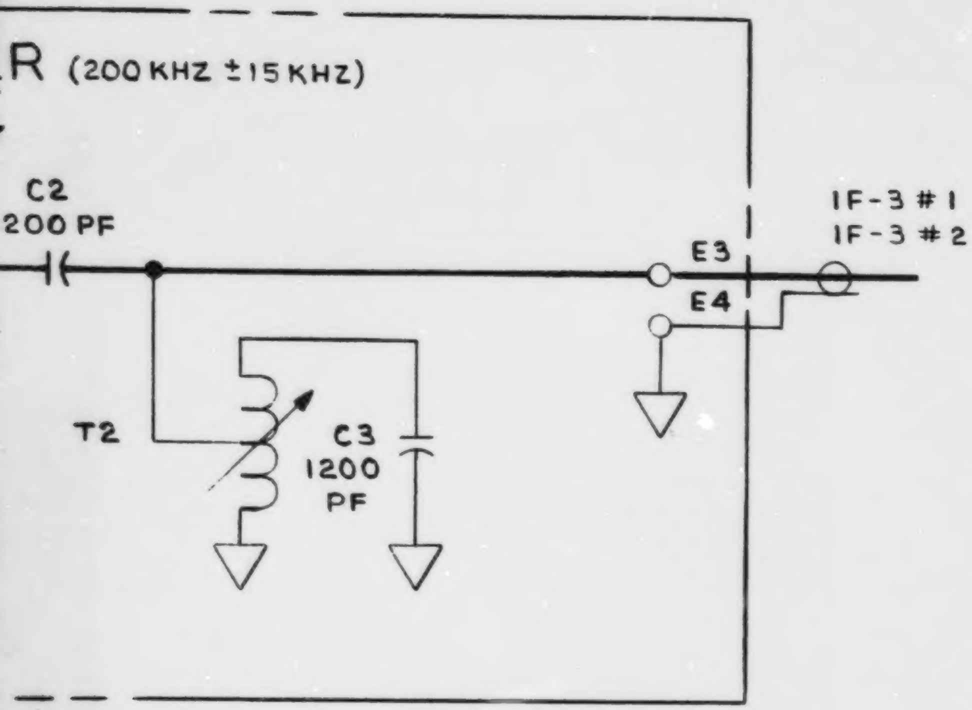
RAVLY

SCHEMATIC DIAGRAM
FINAL IF CHAN 2 MODULE

DWG NO. 66-0843-836 [illegible]


5
BP FILTER (200K
IF-3 #1
IF-3 #2
UNFILTERED
E1
E2
L1
C2
1200 PF
T1
C1
1200
PF
T2

Without prior written consent of
BAYLY ENGINEERING LIMITED, this docum
neither used, copied, reproduced or otherwise
nor its contents communicated to others.


R (200 KHZ ±15 KHZ)
C2
200 PF
E3
E4
IF-3 # 1
IF-3 # 2
T2
C3
1200
PF

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

**BAYLY** ENGINEERING LTD
a member of

TITLE
SCHEMATIC DIAGRAM
FINAL IF CHAN 1+2 (RCVR FRONT OUTSIDE)

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

DRAWN BY
DATE 83-01-02
CHECKED BY
APPROVED BY
DRAWING NO.
66-0643.035 327. CD
-B

of
document may be
dealt with,

### 2.3.7.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 5 | 7 | | | | |
| Adjusters | R27 | T1<br>T2<br>T3<br>T4<br>T5<br>T6 | T1<br>T2<br>L1 | R40<br>R37 | | | | |

a The alignment of block # 3 and # 5 (filters) is done according to specifications written in 2.3.7.4.

b Block 2

Adjust the Gain "R27" for the optimum insertion loss in that conversion.

c Block 7

1) Adjust the output level (output of block 4) at -20 dBm with R40.

2) Adjust the dynamic range of the AGC with R37.

## 2.3.7.4 SPECIFICATIONS

| | BLOCK # | | | | |
|---|---|---|---|---|---|
| | 3 | 5 | | | |
| Impedance INPUT (ohms) | 50 | 50 | | | |
| OUTPUT (ohms) | 50 | 50 | | | |
| Band-Pass (1 dB) (KHz) | | ± 11 | | | |
| (3 dB) (KHz) | ± 7.5 | ± 15 | | | |
| (50 dB) (KHz) | | 114 @ 328 | | | |
| (80 dB) (KHz) | ±18 | | | | |
| Insertion Loss (Center Bandwidth) (dB) | 4 | 1 | | | |
| Center Frequency (KHz) | 200 | 200 | | | |
| | | | | | |

## 2.3.8 PHASE COMPARATOR

a This module is located in the receiver unit.

b Its main functions are :

1 To limit the signal of the two DF channels.

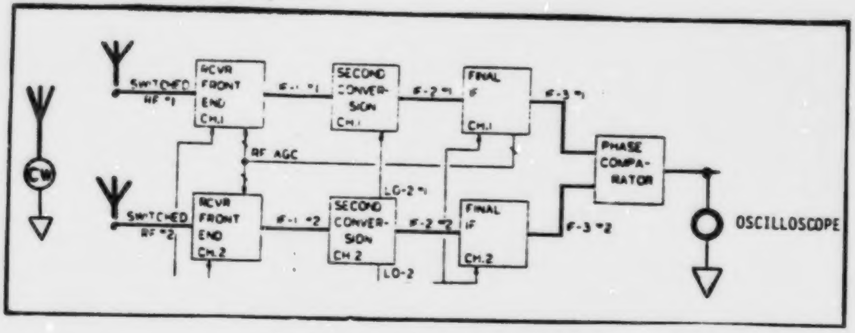
2 To compare the phase difference between the two DF channels.

c On the block diagram, we illustrate the form of the signal at the module output as seen on an oscilloscope.

1 Initial conditions :

Tuning : 118.250 MHz
Field strength (received) : 1 mV/m
Azimuth : 225°

2 Set-up :


SWITCHED RF #1
RCVR FRONT END CH.1
IF-1 #1
SECOND CONVER-SION CH.1
IF-2 #1
FINAL IF CH.1
IF-3 #1
RF AGC
CW
PHASE COMPA-RATOR
LO-2 #1
SWITCHED RF #2
RCVR FRONT END CH.2
IF-1 #2
SECOND CONVER-SION CH 2
IF-2 #2
FINAL IF CH.2
IF-3 #2
LO-2
OSCILLOSCOPE

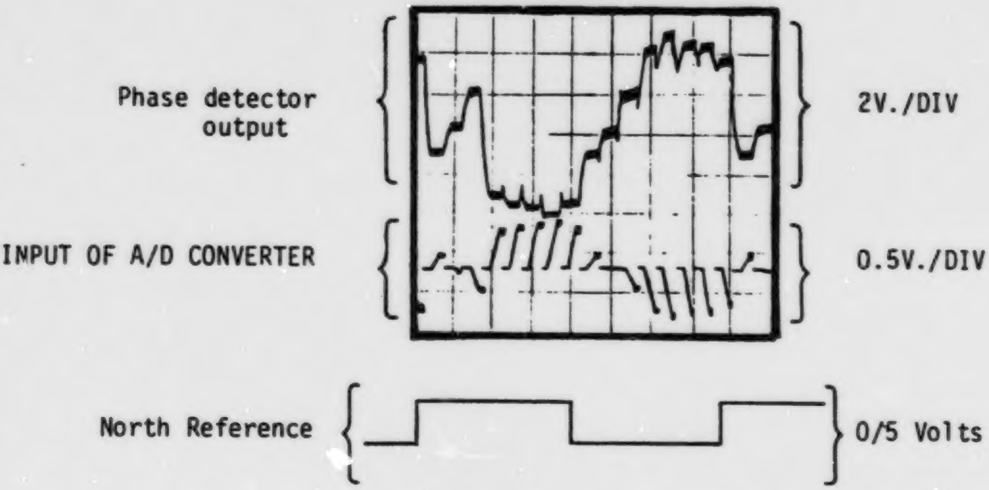
Setting of oscilloscope

External trigger : North Reference
Horizontal : 1.5 ms/DIV
Vertical : 2 V./DIV
Signal strength : 9 volts peak to peak

**OPERATION**

**After limiting the two input signals to a constant amplitude, the phase comparator generates a series of pulses at the incoming signal frequency (200 kHz) which are modulated in width by the phase difference between the two inputs. The pulses are then integrated and filtered to produce a stepped waveform where the height of the steps corresponds to the phase differences between the successive dipole pairs of the antenna array.**

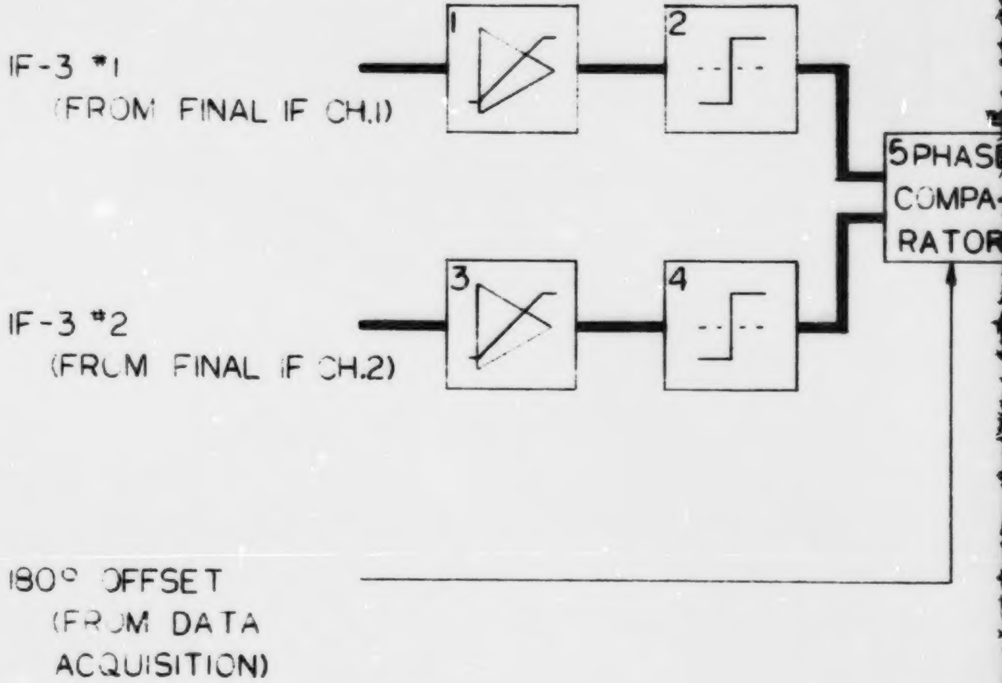
d  Timing between "Phase detector output", North Reference and INPUT OF A/D CONVERTER.



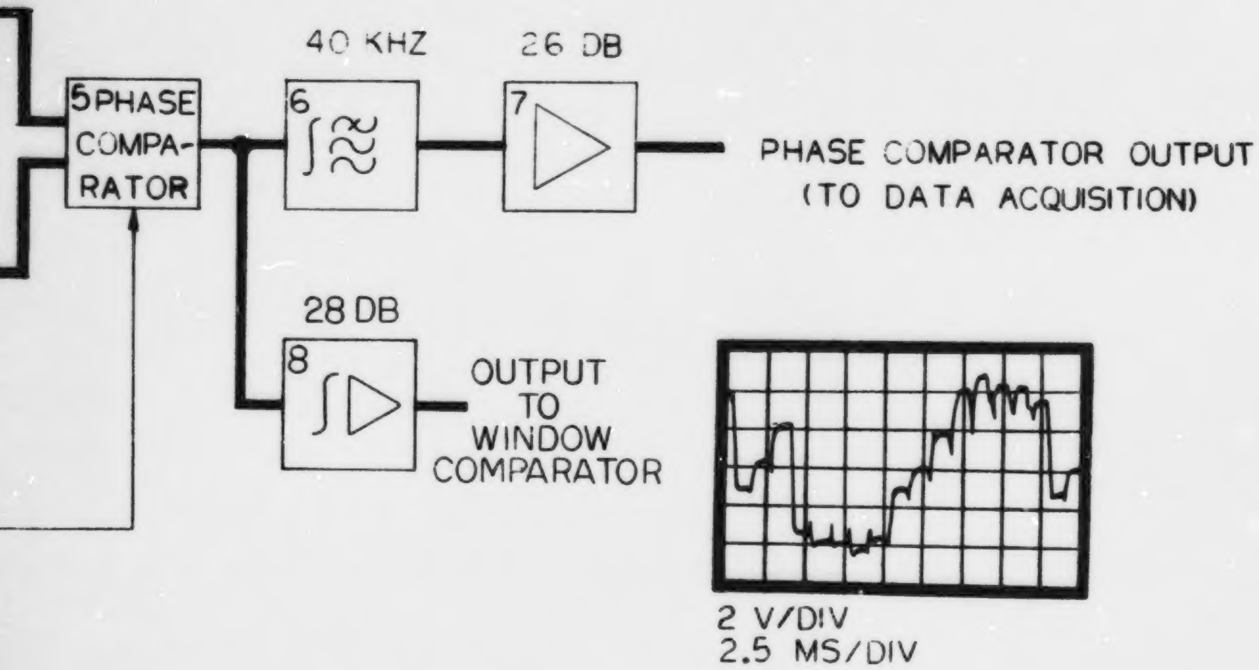
| Identification | Location |
|---|---|
| Phase detector output | At the output of the phase detector |
| INPUT OF A/D CONVERTER | On DATA ACQUISITION BOARD at the input of A/D CONVERTER PIN 14 |
| North Reference | On FRONT PANEL of timing board "North Reference" or TP14 on the PCB. |

## EXTENSION OF THE LINEAR RANGE

**The phase comparator (5) displays a linear voltage/phase characteristic over a range of ±180°. Measurements beyond that range can be made by inverting one of the input channels by 180° and correcting for the inversion in the digital readout. This inversion is routinely performed when the phase reading is above +130° or below -130°, thus extending the total range of the phase detector to ±230°. However, the phase detector is prone to give a high level of noise output when detecting phase differences close to the +180° or -180° limits since the output will fluctuate between the positive and negative values. This unstable condition is detected by tapping the phase comparator output of block (5) and integrating it with a sufficiently small time constant to retain the ±180° noise at its full amplitude. This noise is then amplified by the IC in block 8 and applied to the window comparator in the Data Acquisition Module to cause inversion of the phase detector input and thus cut out the noise.**


IF-3 #1
(FROM FINAL IF CH.1)
1
2
5 PHASE
COMPA-
RATOR
IF-3 #2
(FROM FINAL IF CH.2)
3
4
180° OFFSET
(FROM DATA
ACQUISITION)

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document
neither used, copied, reproduced or otherwise
nor its contents communicated to others.


40 KHZ
26 DB
5 PHASE COMPARATOR
6
7
PHASE COMPARATOR OUTPUT (TO DATA ACQUISITION)
28 DB
8
OUTPUT TO WINDOW COMPARATOR
2 V/DIV
2.5 MS/DIV

| | | | |
|---|---|---|---|
| B | REVISED | 83.5.12 | |
| REV. NO. | REVISION | DATE | APPR. BY |

SCALE
REMOVE BURR MAX 010R
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMALS ± ANGLES ± °
DRAWN BY S.B.
DATE 83-1-20

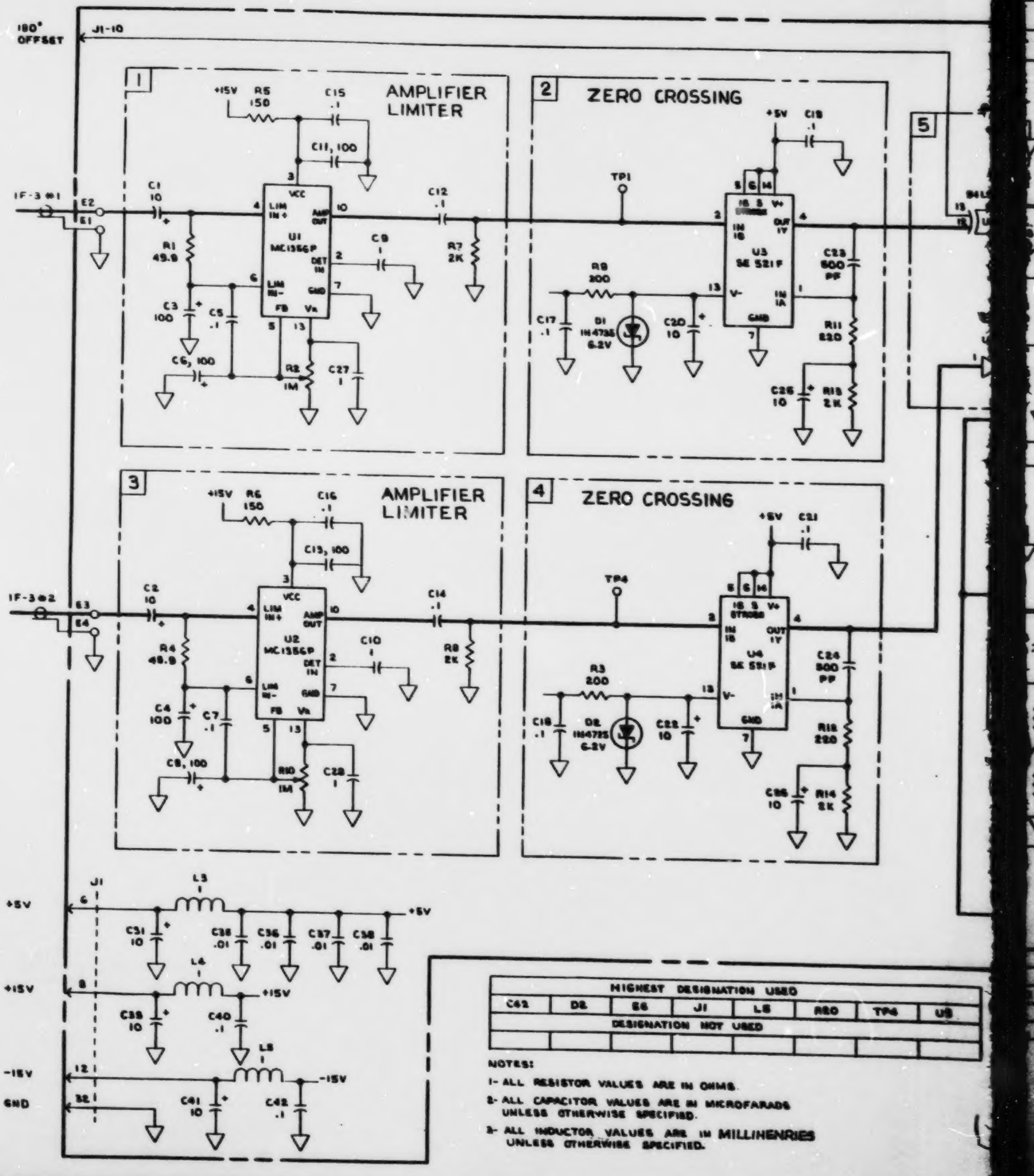
BAYLY ENGINEERING LTD a member of

TITLE
BLOCK DIAGRAM
PHASE COMPARATOR

CHECKED BY
APPROVED BY
DRAWING NO. 66-0643.030 678.BD-B
B

ment of
this document may be
otherwise dealt with,

Without prior written consent of
·V ENGINEERING LIMITED, this document may not be
[illegible]
[illegible]


180° OFFSET
J1-10
1
AMPLIFIER LIMITER
+15V
R5 150
C15 .1
C11, 100
3
VCC
LIM IN+
AMP OUT
U1 MC1356P
DET IN
LIM IN-
GND
FB
Vx
4
10
2
6
7
5
13
IF-3 #1
E2
E1
C1 10
R1 49.9
C3 100
C5 .1
C6, 100
R2 1M
C27 1
C9 1
C12 .1
R7 2K
2
ZERO CROSSING
TP1
+5V
C19 .1
5 6 14
IS S V+
STROBE
IN IB
OUT 1Y
IN IA
V-
GND
U3 SE 521F
R9 200
C17 .1
D1 1N4735 6.2V
C20 10
C23 500 PF
R11 220
C25 10
R13 2K
3
AMPLIFIER LIMITER
+15V
R6 150
C16 .1
C13, 100
U2 MC1356P
IF-3 #2
E3
E4
C2 10
R4 49.9
C4 100
C7 .1
C8, 100
R10 1M
C28 1
C10 1
C14 .1
R8 2K
4
ZERO CROSSING
TP4
+5V
C21 .1
U4 SE 521F
R3 200
C18 .1
D2 1N4735 6.2V
C22 10
C24 500 PF
R12 220
C26 10
R14 2K
5
J1
+5V
6
L3 1
C31 10
C35 .01
C36 .01
C37 .01
C38 .01
+5V
+15V
8
L4 1
C39 10
C40 .1
+15V
-15V
12
L5 1
C41 10
C42 .1
-15V
GND
32

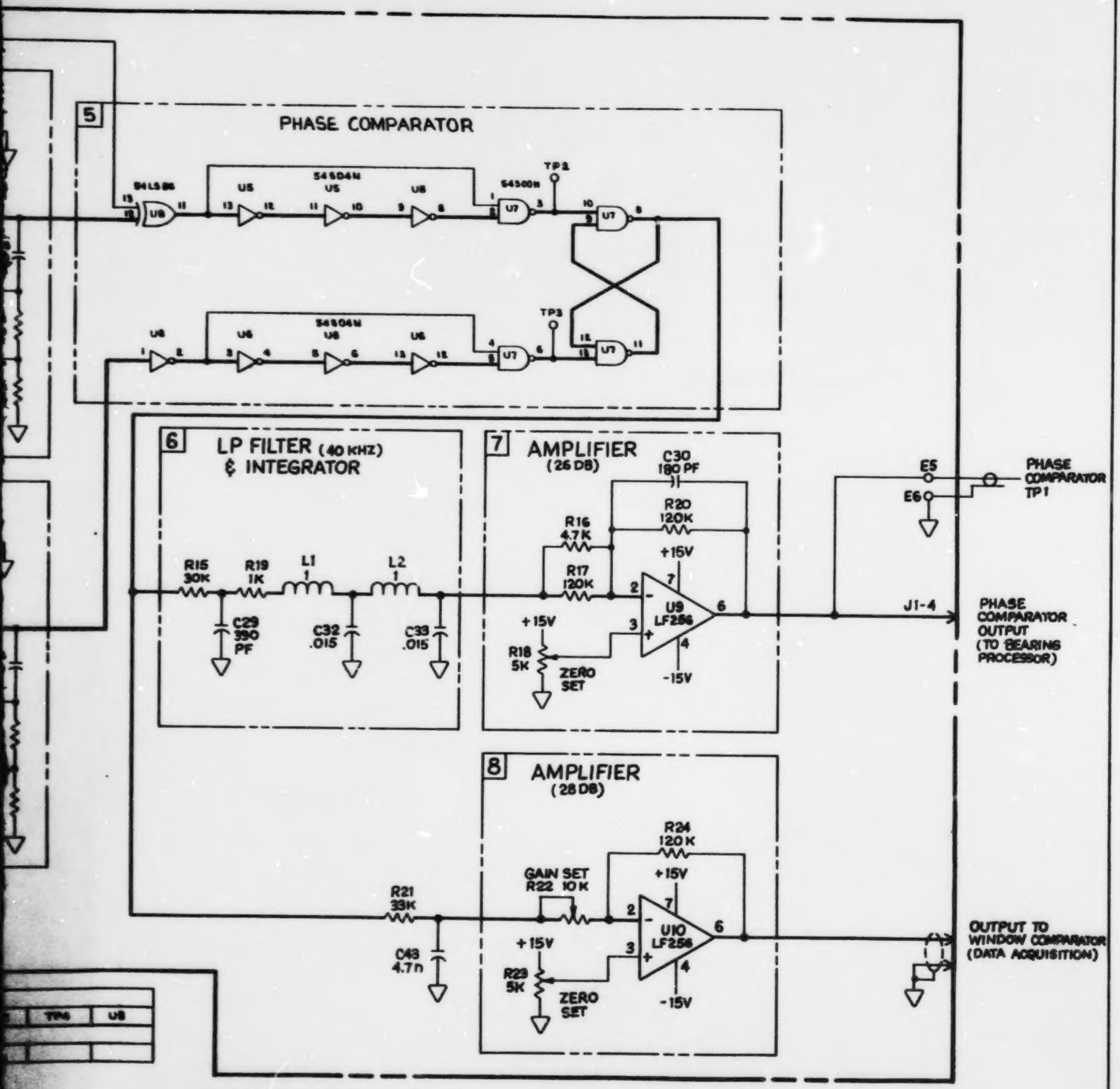
| HIGHEST DESIGNATION USED | | | | | | | |
|---|---|---|---|---|---|---|---|
| C42 | D2 | E6 | J1 | L5 | R20 | TP4 | U5 |
| DESIGNATION NOT USED | | | | | | | |
| | | | | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MILLIHENRIES UNLESS OTHERWISE SPECIFIED.


5
PHASE COMPARATOR
54LS86
U8
U5
54S04N
U5
U8
54S00N
U7
TP2
TP3
U8
U6
54S04N
U6
U6
U7
6
LP FILTER (40 KHZ)
& INTEGRATOR
R15
30K
R19
1K
L1
1
L2
1
C29
390
PF
C32
.015
C33
.015
7
AMPLIFIER
(26 DB)
C30
180 PF
R20
120K
R16
4.7K
R17
120K
+15V
U9
LF256
+15V
R18
5K
ZERO
SET
-15V
E5
E6
PHASE
COMPARATOR
TP1
J1-4
PHASE
COMPARATOR
OUTPUT
(TO BEARING
PROCESSOR)
8
AMPLIFIER
(28 DB)
R24
120 K
GAIN SET
R22 10 K
+15V
R21
33K
C43
4.7n
+15V
R23
5K
ZERO
SET
U10
LF256
-15V
OUTPUT TO
WINDOW COMPARATOR
(DATA ACQUISITION)
TP6
U8

| IC'S SUPPLY DISTRIBUTION | | |
|---|---|---|
| DESIGNATION | GND | +5V |
| U5 TO U8 | PIN 7 | PIN 14 |

BAYLY

SCHEMATIC DIAGRAM
PHASE COMPARATOR

D

### 2.3.8.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 3 | | | | | | |
| Adjusters | R2 | R10 | | | | | | |

Inject an "AM" signal at the input of the Phase Comparator.

IF-3 # 1
IF-3 # 2

Level : - 20 dBm
Tone : 1 KHz
% Modulation : 100 %

Adjust R2 (R10) for a minimum phase jitter at the output of block 2 (4).

Adjust R18 and R23 to give zero DC output for zero input phase

Adjust R22 for the gain of block 8 to be 1-2 dB higher than that of block 7

### 2.3.8.4 SPECIFICATIONS

The linear transfer function for that module is 33 mV for 1 degree difference between IF-3 # 1 and IF-3 # 2. (Signal strength must be between - 40 dBm and + 10 dBm).

## 2.3.9 FREQUENCY SYNTHESIZER

a This module is located in the receiver unit.

b Its main functions are :

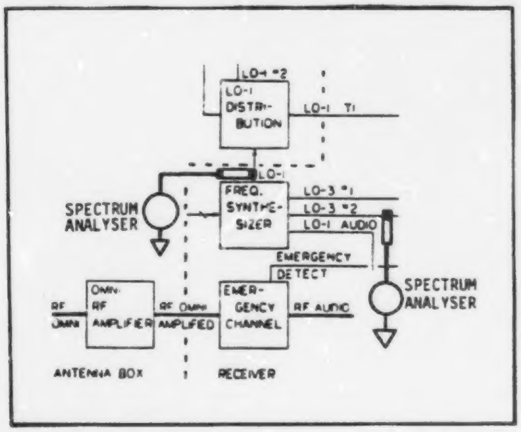
1 Generation of LO-3 for DF channels 1 and 2.
2 Generation of LO-1 for Audio and DF channels.

c On the block diagram, we illustrate the form of two signals on a spectrum analyser.

1 Initial conditions :

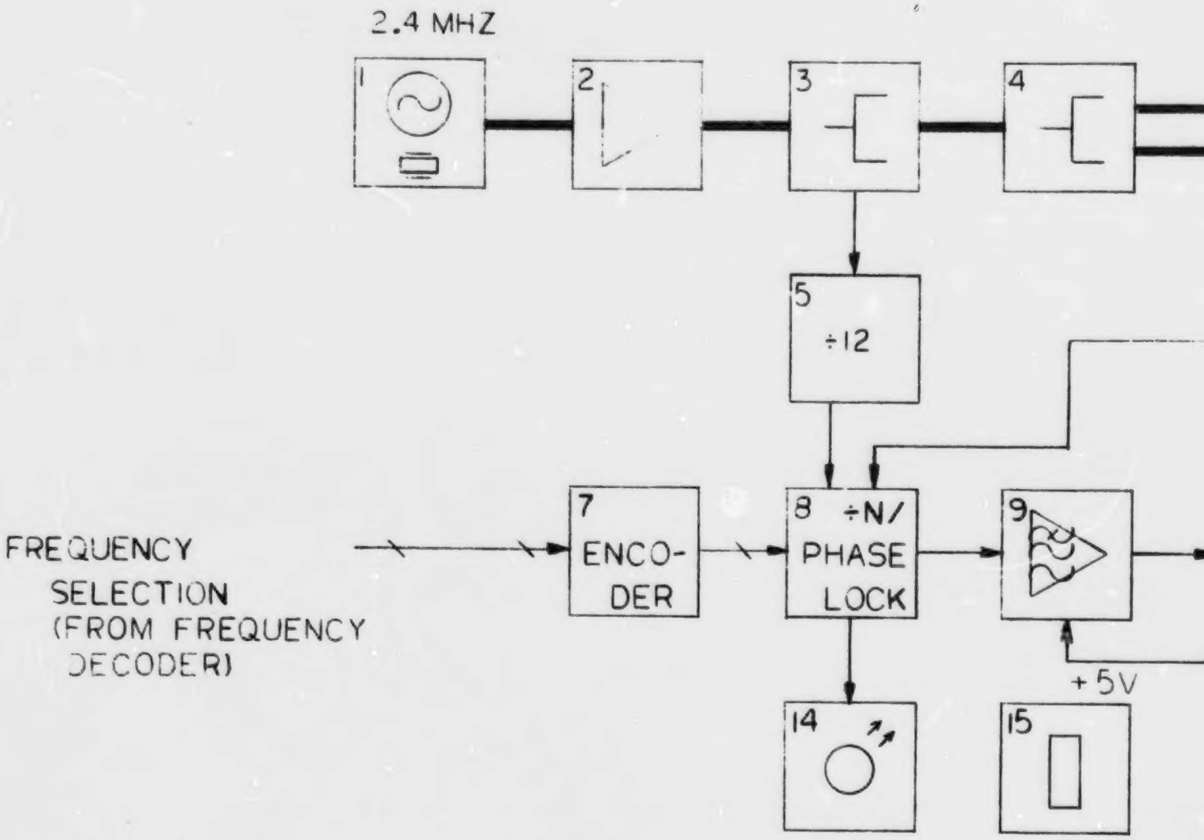
Tuning : 118.250 MHz

2 Set-up :

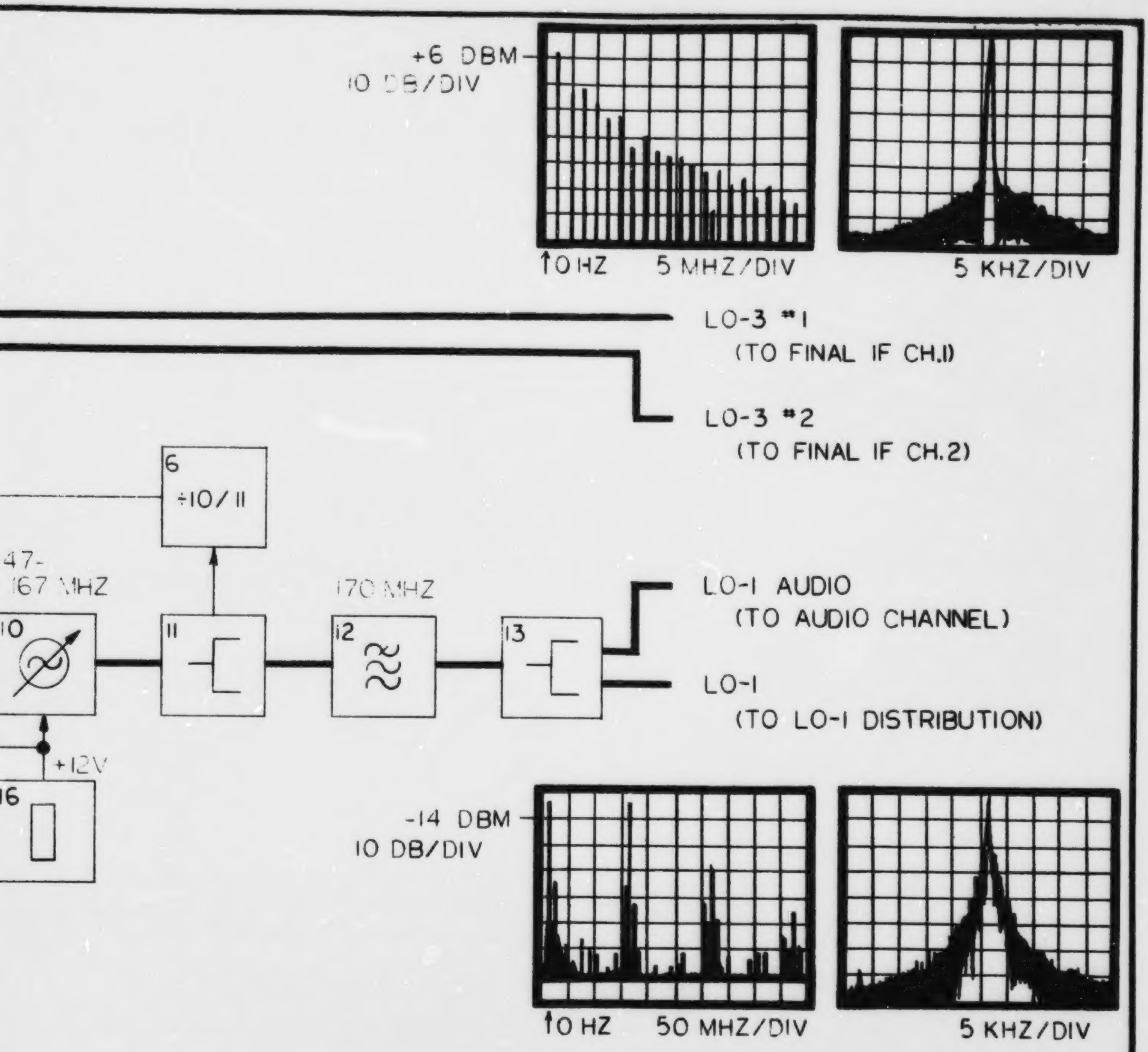

LO-1 #2
LO-1 DISTRI-BUTION
LO-1 T1
LO-1
FREQ. SYNTHE-SIZER
LO-3 #1
LO-3 #2
LO-1 AUDIO
SPECTRUM ANALYSER
EMERGENCY DETECT
SPECTRUM ANALYSER
RF OMNI
OMNI RF AMPLIFIER
RF OMNI AMPLIFIED
EMER-GENCY CHANNEL
RF AUDIO
ANTENNA BOX
RECEIVER

Setting of spectrum analyser

| | LO-1 | | LO-3 | |
|---|---|---|---|---|
| Bandwidth : | 300 Hz | 300KHz | 300 Hz | 10 KHz |
| Scan width : | 5 KHz/DIV | 50 MHz/DIV | 5 KHz/DIV | 5 MHz/DIV |
| Attenuation : | 0 dB | 0 dB | 0 dB | 0 dB |
| Scan Time : | 0.2 SEC/DIV | 50 ms | 0.2 SEC/DIV | 0.2 SEC/DIV |
| Video filter : | 10 KHz | 10 KHz | 10 KHz | 10 KHz |
| Signal strength : | - 4 dBm | - 4 dBm | + 6 dBm | + 6 dBm |


2.4 MHZ
1
2
3
4
5
÷12
7
ENCO-
DER
8 ÷N/
PHASE
LOCK
9
+5V
14
15
FREQUENCY
SELECTION
(FROM FREQUENCY
DECODER)

Without prior written consen
BAYLY ENGINEERING LIMITED, this
neither used, copied, reproduced or oth
nor its contents communicated to others.


+6 DBM
10 DB/DIV
0 HZ
5 MHZ/DIV
5 KHZ/DIV
LO-3 #1
(TO FINAL IF CH.1)
LO-3 #2
(TO FINAL IF CH.2)
6
÷10/11
47-
167 MHZ
170 MHZ
10
11
12
13
LO-1 AUDIO
(TO AUDIO CHANNEL)
LO-1
(TO LO-1 DISTRIBUTION)
+12V
16
-14 DBM
10 DB/DIV
0 HZ
50 MHZ/DIV
5 KHZ/DIV

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE

REMOVE BURR MAX .010R

MATERIAL

FINISH

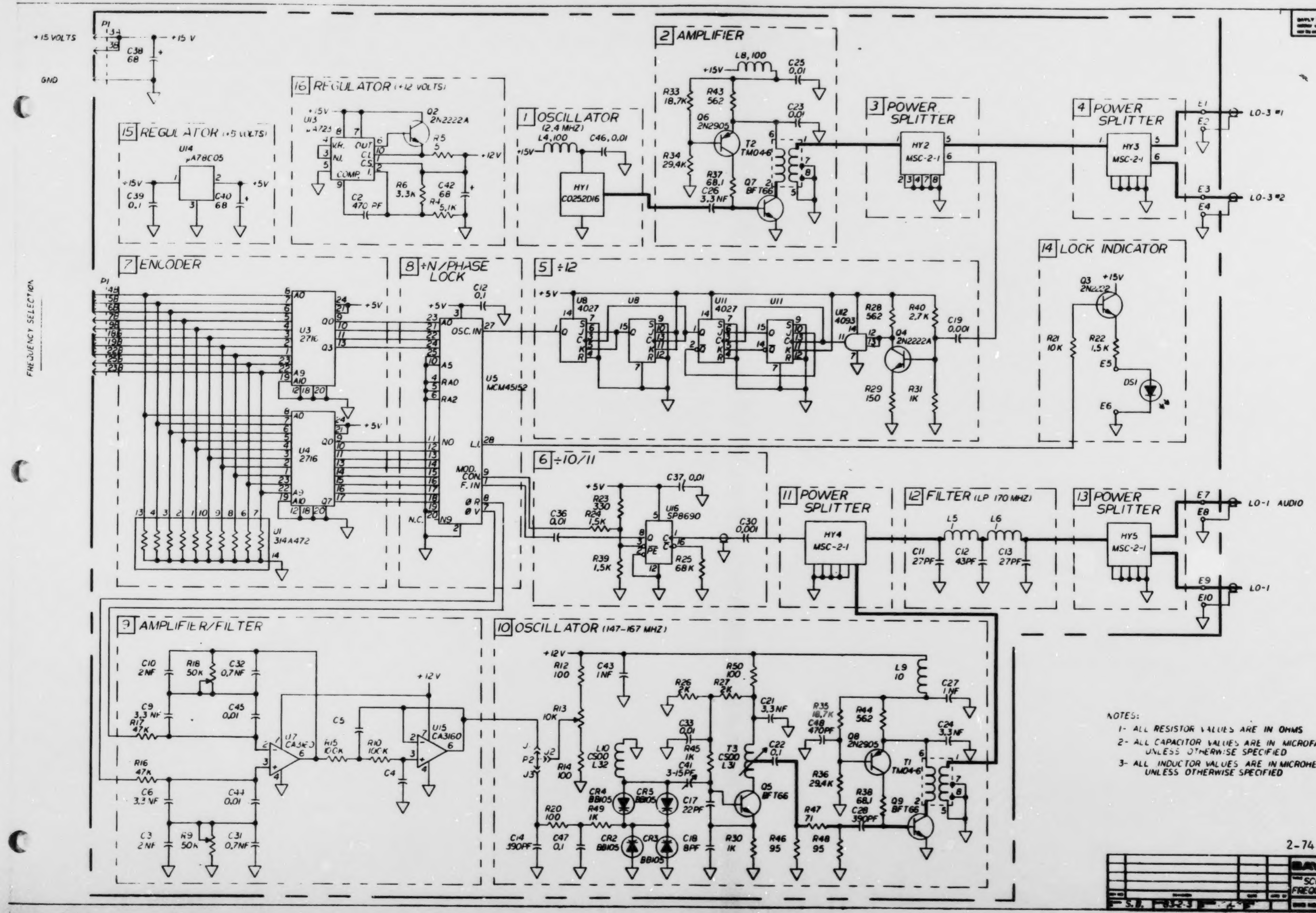
of
cument may be
ise dealt with,

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ±

**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
FREQUENCY SYNTHESIZER

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| S. B. | 83-1-20 | | | 66-0643.035 334.BD-B |


+15 VOLTS
GND
P1
+15 V
C38 68
FREQUENCY SELECTION
15 REGULATOR (+5 VOLTS)
U14 μA78C05
+15V
+5V
C39 0.1
C40 68
16 REGULATOR (+12 VOLTS)
U13 μA723
Q2 2N2222A
R5 5
+12V
C2 470 PF
R6 3.3K
C42 68
R4 5.1K
1 OSCILLATOR (2.4 MHZ)
L4, 100
C46, 0.01
HY1 CO252D16
2 AMPLIFIER
L8, 100
C25 0.01
C23 0.01
R33 18.7K
R43 562
Q6 2N2905
T2 TM04-6
R34 29.4K
R37 68.1
C26 3.3 NF
Q7 BFT66
3 POWER SPLITTER
HY2 MSC-2-1
4 POWER SPLITTER
HY3 MSC-2-1
E1
E2
LO-3 #1
E3
E4
LO-3 #2
7 ENCODER
U3 2716
U4 2716
U1 314A472
8 ÷N/PHASE LOCK
C12 0.1
U5 MCM45152
OSC. IN
MOD. CON.
F. IN
ØR
ØV
N.C.
5 ÷12
U8 4027
U11 4027
U12 4093
R28 562
R40 2.7K
C19 0.001
Q4 2N2222A
R29 150
R31 1K
14 LOCK INDICATOR
Q3 2N2222
+15V
R21 10K
R22 1.5K
E5
DS1
E6
6 ÷10/11
C37, 0.01
R23 330
C36 0.01
R24 1.5K
U16 SP8690
C30 0.001
R39 1.5K
R25 68K
11 POWER SPLITTER
HY4 MSC-2-1
12 FILTER (LP 170 MHZ)
L5
L6
C11 27PF
C12 43PF
C13 27PF
13 POWER SPLITTER
HY5 MSC-2-1
E7
E8
LO-1 AUDIO
E9
E10
LO-1
9 AMPLIFIER/FILTER
C10 2NF
R18 50K
C32 0.7NF
C9 3.3 NF
C45 0.01
R17 47K
U17 CA3160
C5
R15 100K
R10 100K
U15 CA3160
C4
R16 47K
C6 3.3 NF
C44 0.01
C3 2NF
R9 50K
C31 0.7NF
+12V
10 OSCILLATOR (147-167 MHZ)
R12 100
C43 1NF
R13 10K
R14 100
L10 CS00 L32
R26 2K
R27 2K
C33 0.01
R45 1K
C41 3-15PF
T3 CS00 L31
R50 100
C21 3.3 NF
C22 0.1
Q5 BFT66
CR4 BB105
CR5 BB105
C17 22PF
R49 1K
R20 100
C14 390PF
C47 0.1
CR2 BB105
CR3 BB105
C18 8PF
R30 1K
R46 95
R35 18.7K
C48 470PF
R44 562
Q8 2N2905
T1 TM04-6
R36 29.4K
R38 68.1
C28 390PF
Q9 BFT66
R47 71
R48 95
L9 10
C27 1NF
C24 3.3NF
P2
J2
J3

NOTES:
1- ALL RESISTOR VALUES ARE IN OHMS
2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED
3- ALL INDUCTOR VALUES ARE IN MICROHENRES UNLESS OTHERWISE SPECIFIED

| HIGHEST DESIGNATION USED | DESIGNATION NOT USED |
|---|---|
| C48 | C1,7,8,15,16,20,29,34,35 |
| CR5 | CR1 |
| DS1 | |
| E10 | |
| HY5 | |
| J3 | |
| L10 | L1,2,3,7 |
| P2 | |
| Q9 | Q1 |
| R50 | R1,2,3,7,8,11,15,30,32,41,42 |
| T3 | |
| U16 | U2,6,9,10 |

2-74

BAYLY

SCHEMATIC DIAGRAM
FREQUENCY SYNTHESIZER

S.B.
83-2-3
66-0643,035 334,CO-D

### 2.3.9.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 9 | 10 | | | | | | |
| Adjusters | R9<br>R18 | C41<br>T3<br>R13 | | | | | | |

a Adjust R9 and R18 for minimum phase noise and maximum rejection of the reference (25 KHz away).

b With the LOOP OPEN (disconnect DC control for PLL and connect R13), adjust "C31" and "L11" to get the proper frequency range (147 MHz @ 167 MHz).

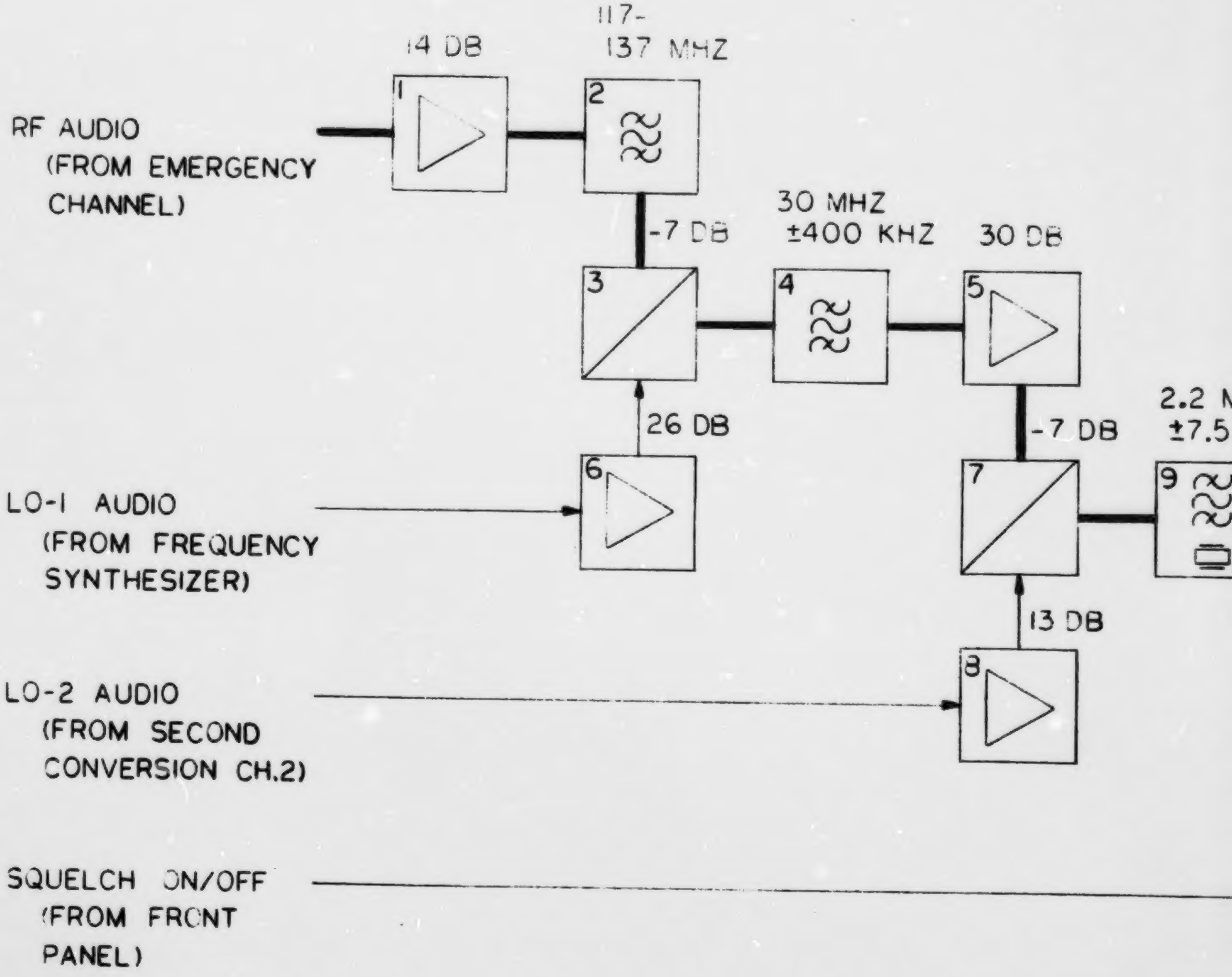
## 2.3.9.4 SPECIFICATIONS

| | Frequency | Level at the output |
|---|---|---|
| LO-3 | 2.400 MHz | + 6 dBm |
| LO-1 | 147.5 to 166.5 MHz | - 4 dBm |

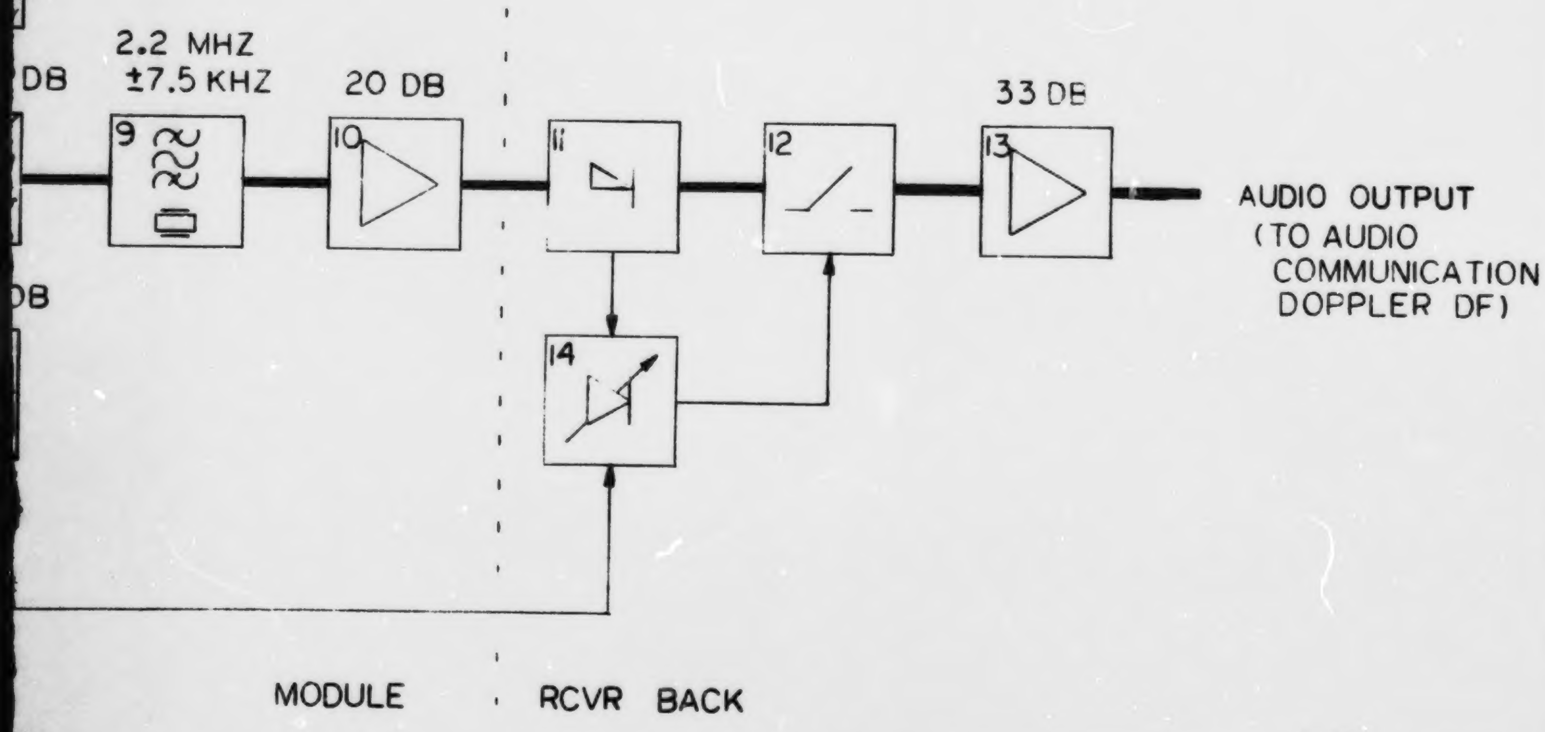
## 2.3.10 AUDIO CHANNEL

a This module is located in the receiver unit and is partially contained in the receiver back.

b Its main function is to demodulate the AM signal.


RF AUDIO (FROM EMERGENCY CHANNEL)
LO-1 AUDIO (FROM FREQUENCY SYNTHESIZER)
LO-2 AUDIO (FROM SECOND CONVERSION CH.2)
SQUELCH ON/OFF (FROM FRONT PANEL)
14 DB
117-137 MHZ
1
2
3
4
5
6
7
8
9
-7 DB
30 MHZ ±400 KHZ
30 DB
26 DB
-7 DB
2.2
±7.5
13 DB

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document
neither used, copied, reproduced or otherwise dealt
nor its contents communicated to others.



DB
DB
2.2 MHZ
±7.5 KHZ
9
20 DB
10
11
12
33 DB
13
14
AUDIO OUTPUT
(TO AUDIO
COMMUNICATION
DOPPLER DF)
MODULE
RCVR BACK

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE

REMOVE BURR MAX .010R

MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED
TOLERANCES DECIMALS ± ANGLES ± °

DRAWN BY S.B.

DATE 83-1-21

CHECKED BY

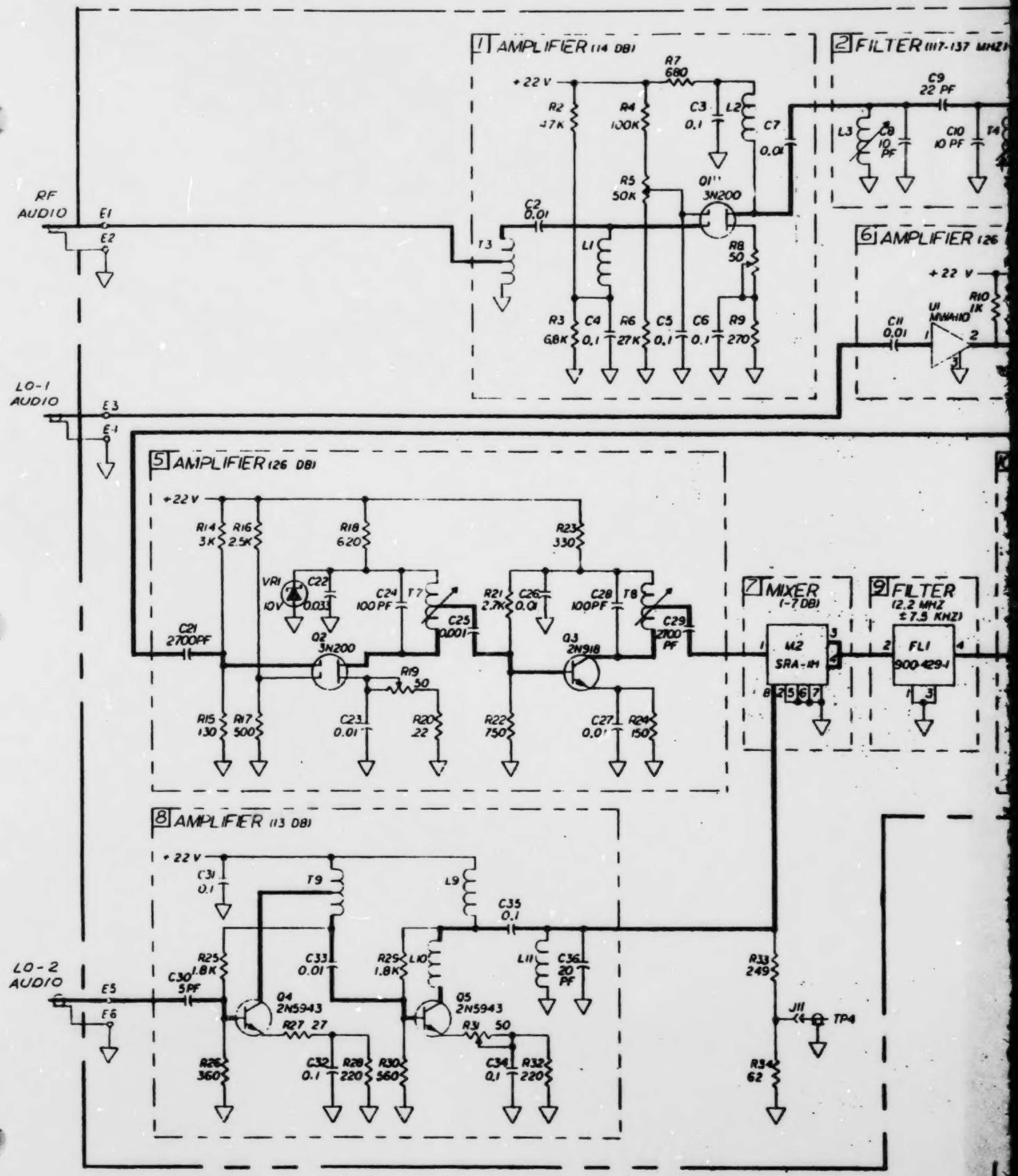
APPROVED BY

**BAYLY** ENGINEERING LTD
a member of

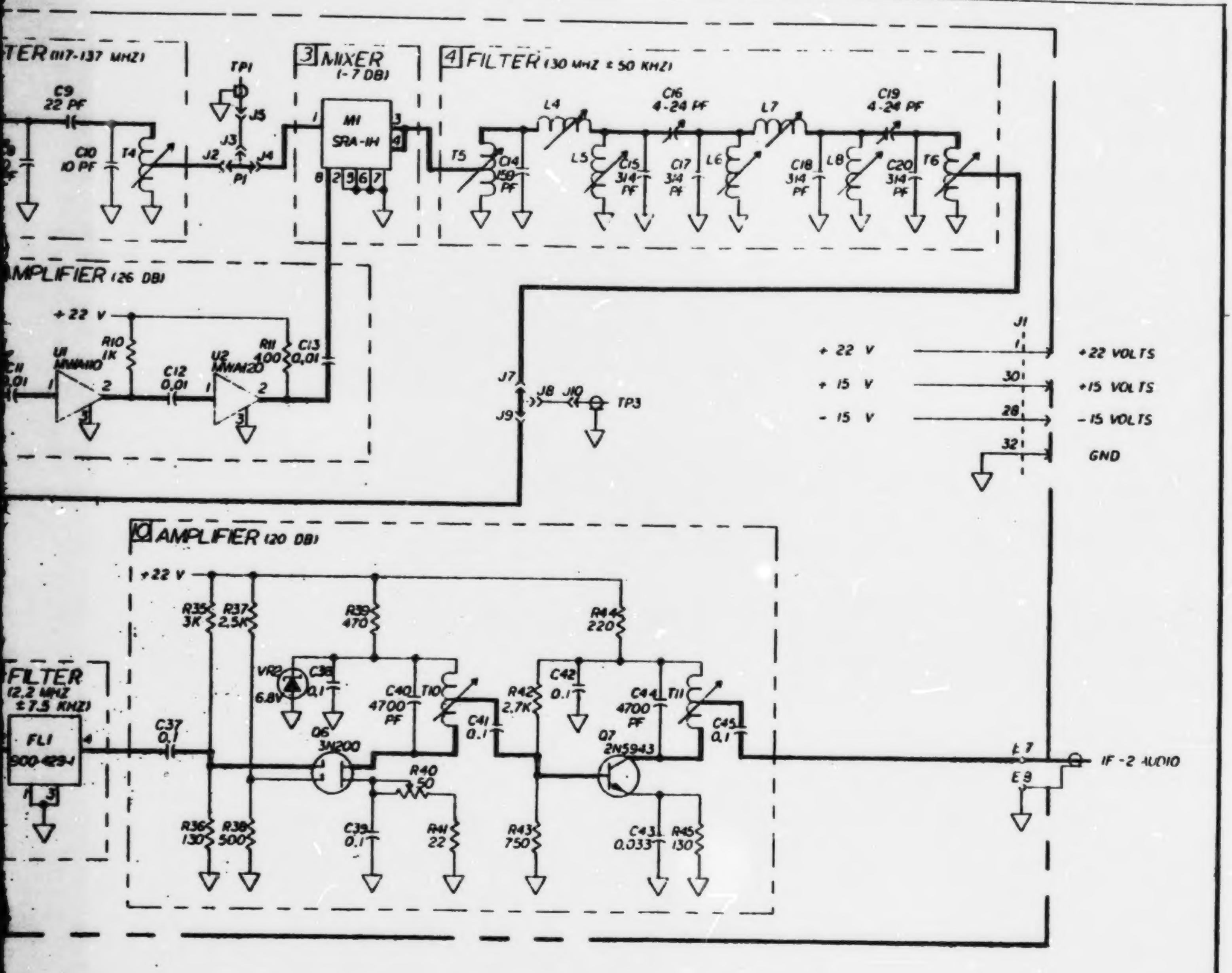
TITLE BLOCK DIAGRAM
AUDIO CHANNEL

DRAWING NO. 714-0643.030 522.BD-B

of
document may be
dealt with,


RF AUDIO
E1
E2
LO-1 AUDIO
E3
E-1
LO-2 AUDIO
E5
E6
1 AMPLIFIER (14 DB)
+22 V
R7 680
R2 47K
R4 100K
C3 0.1
L2
C7 0.01
R5 50K
Q1 3N200
C2 0.01
T3
L1
R8 50
R3 6.8K
C4 0.1
R6 27K
C5 0.1
C6 0.1
R9 270
2 FILTER (117-137 MHZ)
C9 22 PF
L3
C8 10 PF
C10 10 PF
T4
6 AMPLIFIER (26
+22 V
R10 1K
C11 0.01
U1 MWA110
1
2
3
5 AMPLIFIER (26 DB)
+22 V
R14 3K
R16 2.5K
R18 620
R23 330
VR1 10V
C22 0.033
C24 100 PF
T7
C25 0.001
R21 2.7K
C26 0.01
C28 100 PF
T8
C29 2700 PF
C21 2700PF
Q2 3N200
R19 50
Q3 2N918
R15 130
R17 500
C23 0.01
R20 22
R22 750
C27 0.01
R24 150
7 MIXER (-7 DB)
M2 SRA-1H
1
3
4
8
2
5
6
7
9 FILTER 12.2 MHZ ±7.5 KHZ
FL1 9004291
2
4
1
3
8 AMPLIFIER (13 DB)
+22 V
C31 0.1
T9
L9
C35 0.1
R25 1.8K
C33 0.01
R25 1.8K
L10
L11
C36 20 PF
C30 5PF
Q4 2N5943
Q5 2N5943
R27 27
R31 50
R26 360
C32 0.1
R28 220
R30 560
C34 0.1
R32 220
R33 249
J11
TP4
R34 62

4E

 
TER (117-137 MHZ)
C9
22 PF
C10
10 PF
T4
TP1
J5
J3
J2
P1
J4
3 MIXER
(1-7 DB)
M1
SRA-1H
4 FILTER (30 MHZ ± 50 KHZ)
L4
C16
4-24 PF
L7
C19
4-24 PF
T5
C14
150 PF
L5
C15
314 PF
C17
314 PF
L6
C18
314 PF
L8
C20
314 PF
T6
AMPLIFIER (26 DB)
+22 V
R10
1K
U1
MWA110
C11
0.01
C12
0.01
U2
MWA120
R11
400
C13
0.01
J7
J8
J10
TP3
J9
J1
+ 22 V
+ 15 V
- 15 V
+22 VOLTS
+15 VOLTS
-15 VOLTS
GND
10 AMPLIFIER (20 DB)
+22 V
R35
3K
R37
2.5K
R39
470
R44
220
VR2
6.8V
C38
0.1
C40
4700 PF
T10
R42
2.7K
C42
0.1
C44
4700 PF
T11
C41
0.1
C45
0.1
Q6
3N200
Q7
2N5943
R40
50
FILTER
(2.2 MHZ
±7.5 KHZ)
FL1
900-429-1
C37
0.1
R36
130
R38
500
C39
0.1
R41
22
R43
750
C43
0.033
R45
130
E7
E8
IF-2 AUDIO

| HIGHEST DESIGNATION USED | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C45 | | E6 | FL1 | J11 | L11 | M2 | P1 | | Q7 | R45 | T11 | TP4 | U2 | VR2 |
| DESIGNATION NOT USED | | | | | | | | | | | | | | |
| C1 | | | | J6 | | | | | | R1, R12,<br>R13 | T1, T2 | TP2 | | |

NOTES

1- ALL RESISTOR VALUES ARE IN OHMS.

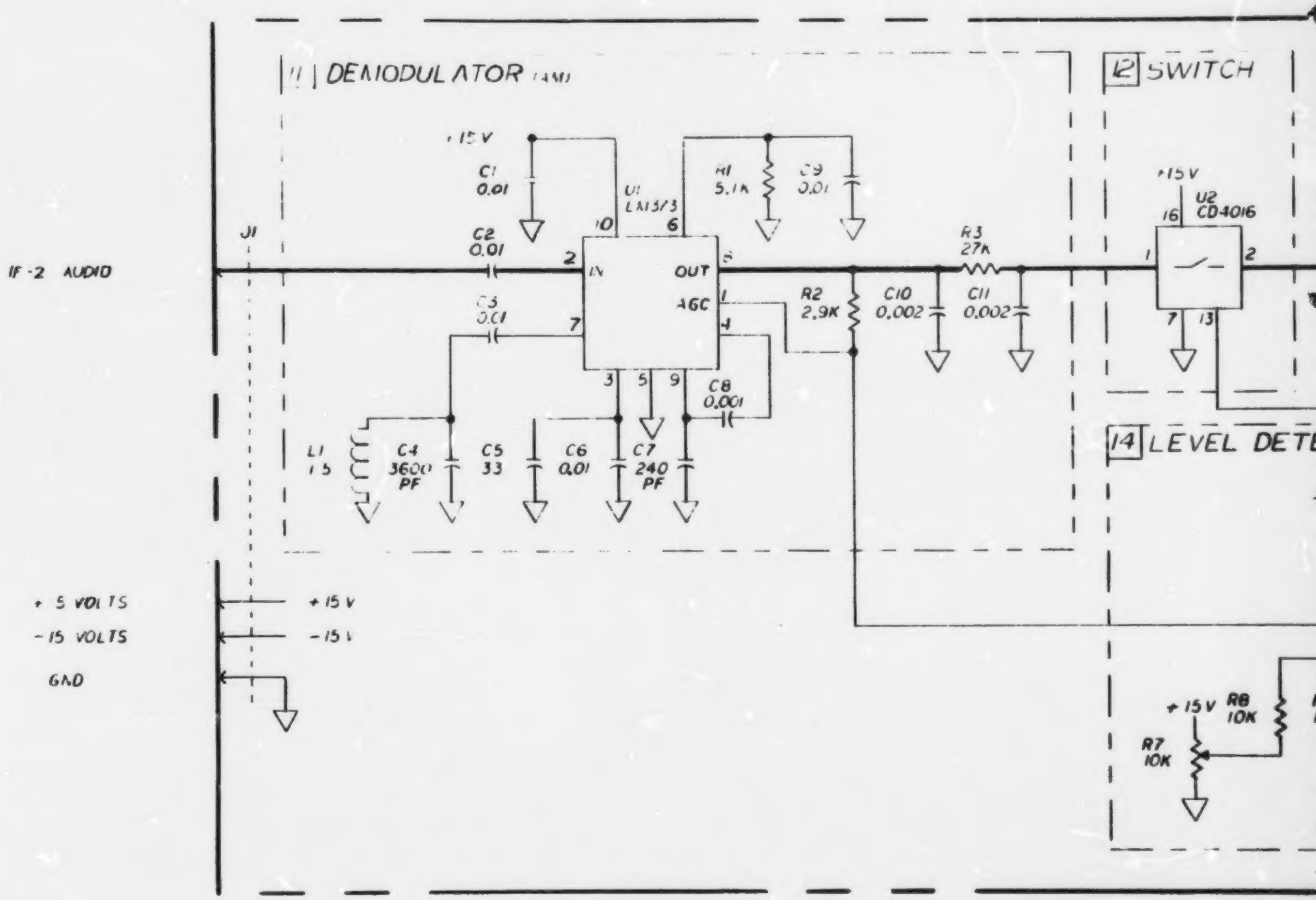
2- ALL CAPACITOR VALUES ARE IN MICROFARADS
UNLESS OTHERWISE SPECIFIED.

BAYLY

SCHEMATIC DIAGRAM
AUDIO CHANNEL MODULE

S.B. 82-1-87

714-643030 522.CD-0


11 DEMODULATOR (AM)
12 SWITCH
14 LEVEL DETE
IF-2 AUDIO
J1
+15 V
C1 0.01
U1 LM1373
C2 0.01
C3 0.01
IN
OUT
AGC
R1 5.1K
C9 0.01
R2 2.9K
C10 0.002
R3 27K
C11 0.002
C8 0.001
L1 1.5
C4 3600 PF
C5 33
C6 0.01
C7 240 PF
+15V
U2 CD4016
+5 VOLTS
-15 VOLTS
GND
+15 V
-15 V
+15 V
R8 10K
R7 10K

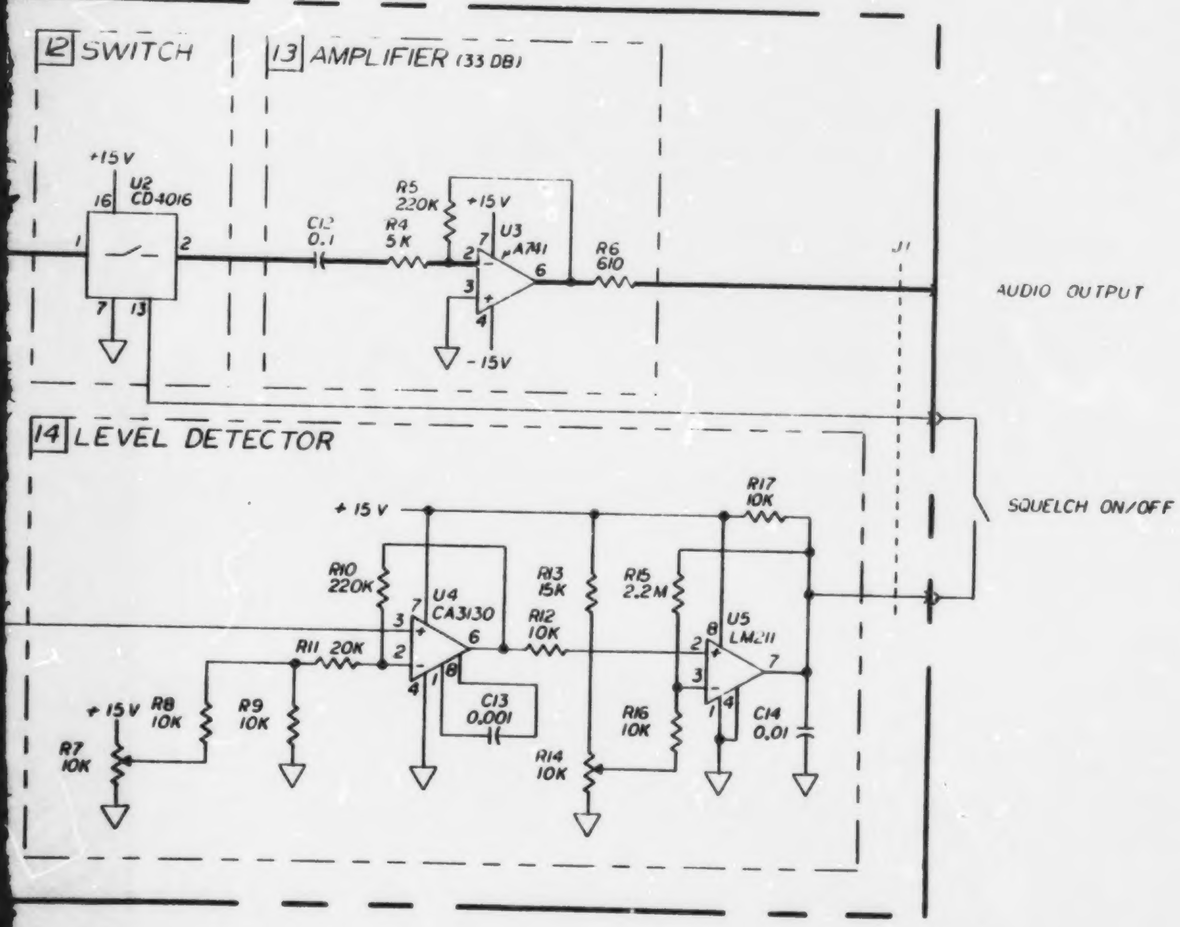
| HIGHEST DESIGNATION USED | | | | |
|---|---|---|---|---|
| C11 | J1 | L1 | R17 | U5 |
| DESIGNATION NOT USED | | | | |
| | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES.


12 SWITCH
13 AMPLIFIER (33 DB)
14 LEVEL DETECTOR
+15 V
U2
CD4016
16
1
2
7
13
C12
0.1
R4
5K
R5
220K
+15 V
U3
μA741
7
2
3
4
6
-15 V
R6
610
J1
AUDIO OUTPUT
SQUELCH ON/OFF
+15 V
R10
220K
U4
CA3130
3
2
7
6
4
1
8
C13
0.001
R11 20K
R8
10K
R9
10K
+15 V
R7
10K
R13
15K
R12
10K
R14
10K
R15
2.2 M
R16
10K
R17
10K
U5
LM211
8
2
3
7
1
4
C14
0.01

2-80

BAYLY

SCHEMATIC DIAGRAM
AUDIO CHANNEL RCVR BACK

S.B.
83-1-20
714-0643.035 324.CD-D

## 2.3.10.3 ALIGNMENT

| | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 5 | 8 | 10 | 14 | |
| Adjusters | R5<br>R8 | L3<br>L4 | T5<br>T6<br>L4<br>L5<br>L6<br>L7<br>L8<br>C16<br>C19 | T7<br>T8<br>R19 | R31 | R40<br>T10<br>T11 | R7 | |

a The alignment of block # 2 and # 4 (filters) is done according to specifications written in 2.3.10.4.

b The alignment of block # 1, # 5, # 8 and # 10 is done by tuning the 'LC Tank' and by adjusting it to a specified amplitude response at the center frequency (see 2.3.10.4).

c Block # 14

With "NO" signal at the input of "OMNI RF AMPLIFIER" adjust R55 for 0 Vdc at the output of the operational amplifier.

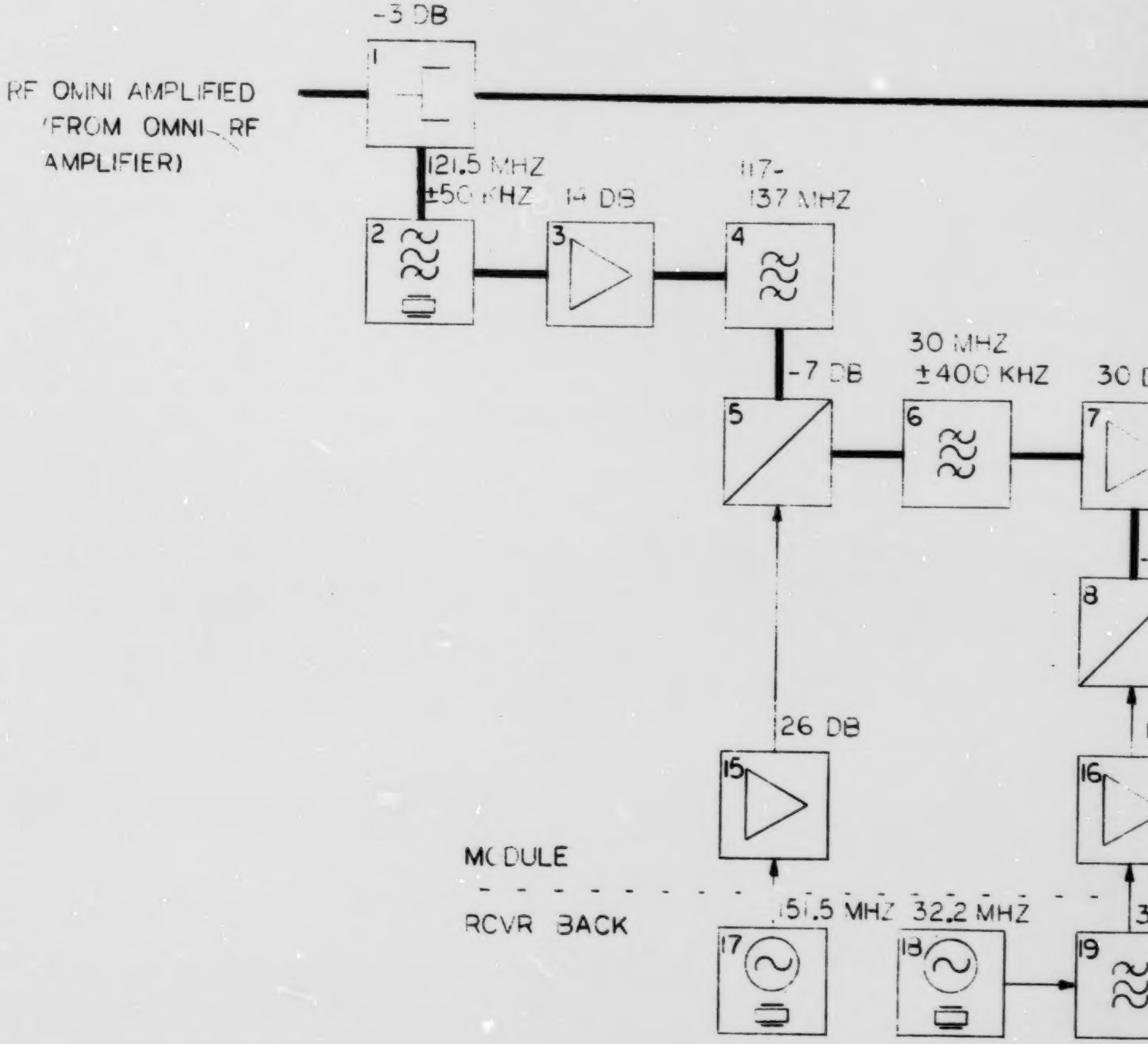
## 2.3.10.4 SPECIFICATIONS

| | BLOCK # | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 5 | 8 | 10 |
| Impedance INPUT (ohms) | 50 | | 50 | 50 | 50 | 50 |
| OUTPUT (ohms) | | 50 | 50 | 50 | 50 | 50 |
| Gain - Loss (dB) | 14 | | | 30 | 13 | 20 |
| Band-Pass (1 dB) (MHz) | | 117 @ 137 | | | | |
| (3 dB) (KHz) | | | ± 50 | | | |
| Center Frequency (MHz) | | | 30 | | | |
| | | | | | | |

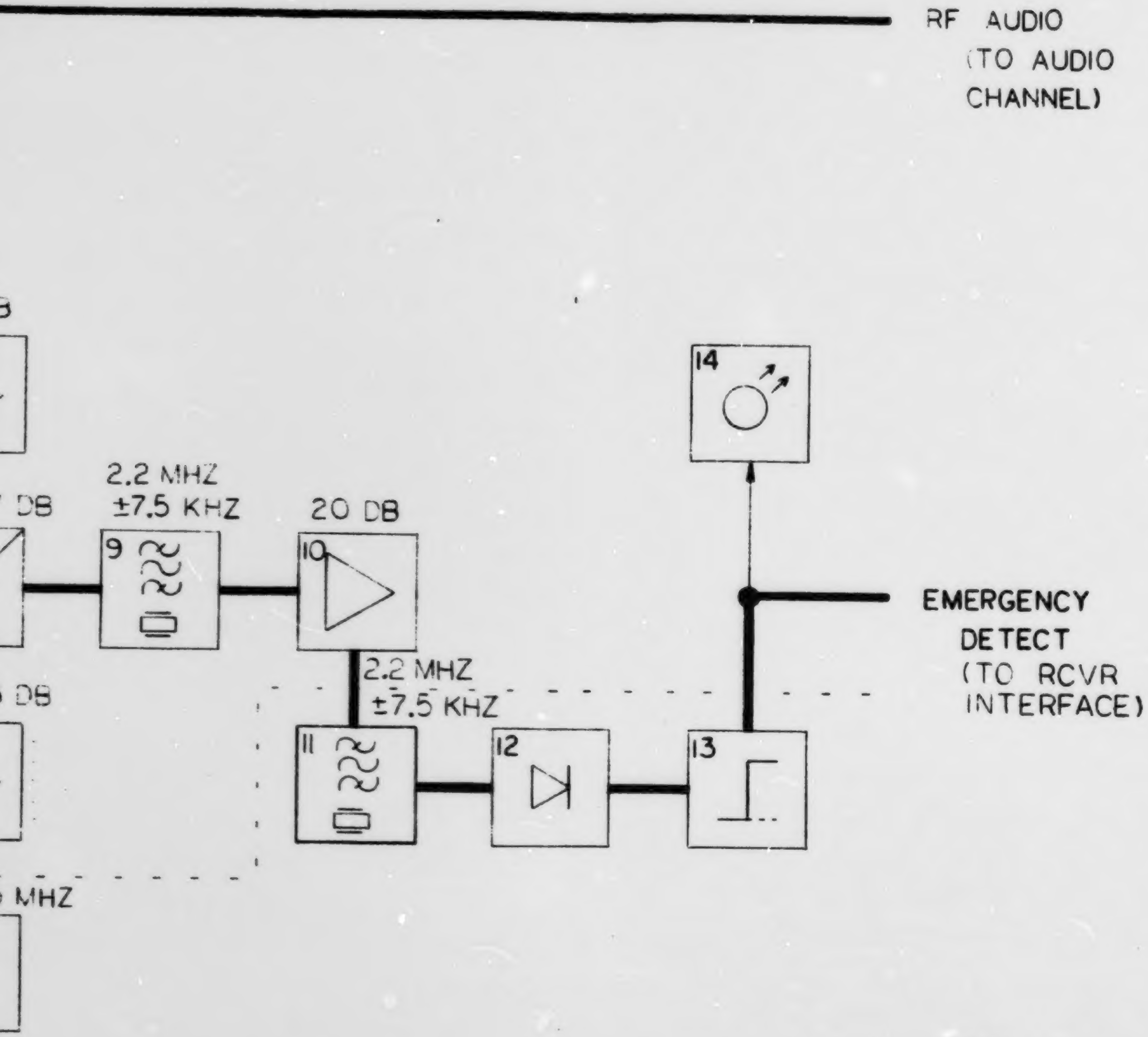
## 2.3.11 EMERGENCY CHANNEL

a This module is located in the receiver unit and is partially contained in the receiver back.

b Its main function is to detect the presence of a signal transmitted at 121.5 MHz.


-3 DB
1
RF OMNI AMPLIFIED
(FROM OMNI RF
AMPLIFIER)
121.5 MHZ
±50 KHZ
14 DB
117-
137 MHZ
2
3
4
-7 DB
30 MHZ
±400 KHZ
30 D
5
6
7
8
26 DB
15
16
MODULE
RCVR BACK
151.5 MHZ
32.2 MHZ
3
17
18
19

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document m
neither used, copied, reproduced or otherwise dealt
nor its contents communicated to others.


RF AUDIO
(TO AUDIO CHANNEL)
B
DB
2.2 MHZ
±7.5 KHZ
9
20 DB
10
DB
2.2 MHZ
±7.5 KHZ
11
12
13
14
EMERGENCY DETECT
(TO RCVR INTERFACE)
MHZ

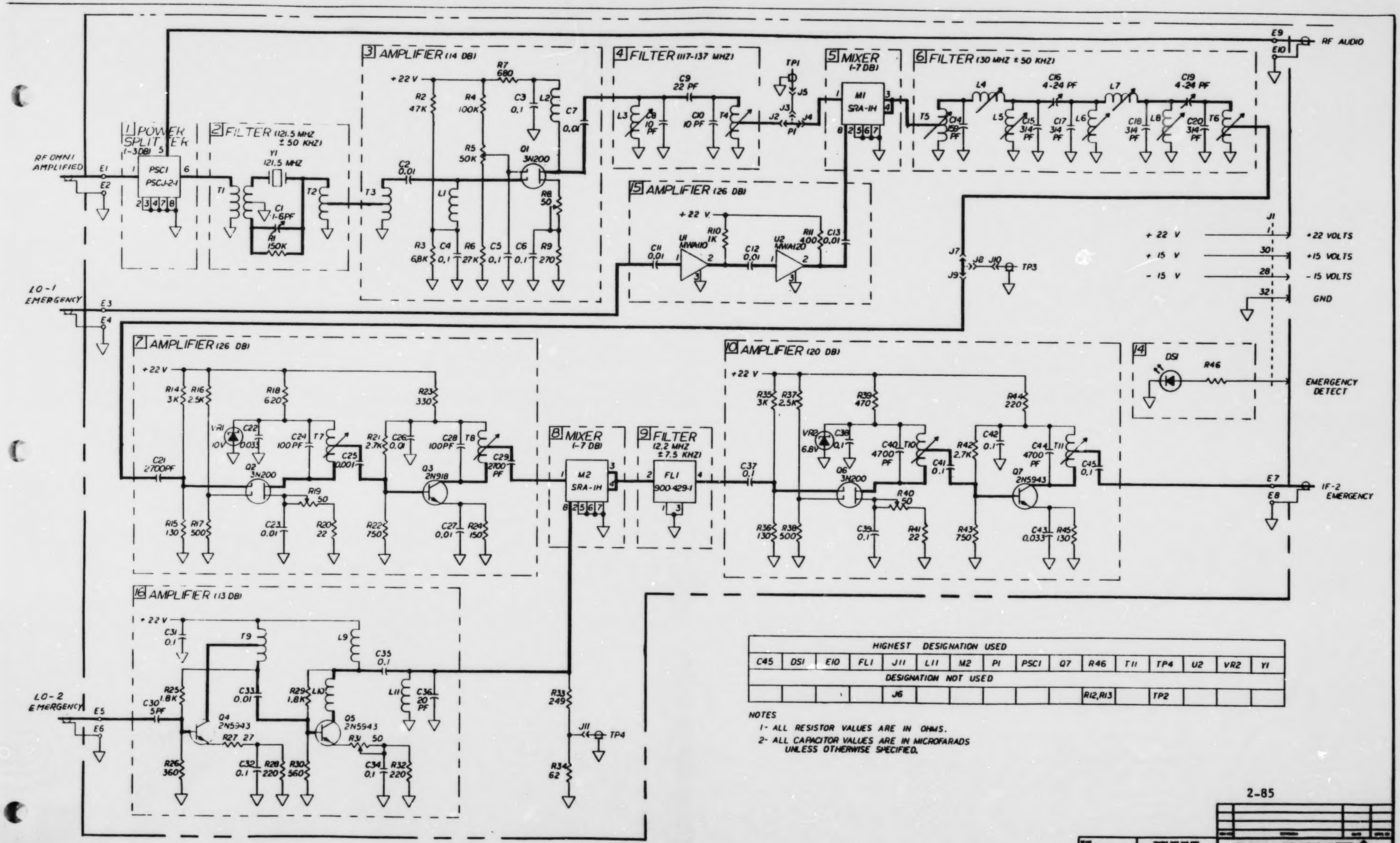
| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|

| | | |
|---|---|---|
| SCALE | REMOVE BURR MAX .010R | |
| MATERIAL | | |
| FINISH | | |
| UNLESS OTHERWISE SPECIFIED<br>TOLERANCES ANGLES<br>DECIMALS ± ± | DRAWN BY<br>S.B. | DATE<br>83-1-21 |

**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
EMERGENCY CHANNEL

| CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|
| | | 714-0643.030 524.BD-B |


RF OMNI AMPLIFIED
E1
E2
1 POWER SPLITTER (-3DB)
PSC1 PSCJ-2-1
2 FILTER (121.5 MHZ ± 50 KHZ)
Y1 121.5 MHZ
C1 1-6PF
R1 150K
T1
T2
3 AMPLIFIER (14 DB)
+22 V
R7 680
R2 47K
R4 100K
C3 0.1
L2
C7 0.01
R5 50K
Q1 3N200
C2 0.01
T3
L1
R8 50
R3 6.8K
C4 0.1
R6 27K
C5 0.1
C6 0.1
R9 270
4 FILTER (117-137 MHZ)
C9 22 PF
L3
C8 10 PF
C10 10 PF
T4
TP1
J5
J3
J2
P1
J4
5 MIXER (-7 DB)
M1 SRA-1H
6 FILTER (30 MHZ ± 50 KHZ)
L4
C16 4-24 PF
L7
C19 4-24 PF
T5
C14 150 PF
L5
C15 314 PF
C17 314 PF
L6
C18 314 PF
L8
C20 314 PF
T6
E9
E10
RF AUDIO
15 AMPLIFIER (26 DB)
+22 V
R10 1K
R11 400
C13 0.01
C11 0.01
U1 MWA110
C12 0.01
U2 MWA120
J7
J8
J10
TP3
J9
J1
+ 22 V
+ 15 V
- 15 V
30
28
32
+22 VOLTS
+15 VOLTS
- 15 VOLTS
GND
LO-1 EMERGENCY
E3
E4
7 AMPLIFIER (26 DB)
+22 V
R14 3K
R16 2.5K
R18 620
R23 330
VR1 10V
C22 0.033
C24 100 PF
T7
C25 0.001
R21 2.7K
C26 0.01
C28 100PF
T8
C29 2700 PF
C21 2700PF
Q2 3N200
R19 50
Q3 2N918
R15 130
R17 500
C23 0.01
R20 22
R22 750
C27 0.01
R24 150
8 MIXER (-7 DB)
M2 SRA-1H
9 FILTER (12.2 MHZ ± 7.5 KHZ)
FL1 900 429-1
10 AMPLIFIER (20 DB)
+22 V
R35 3K
R37 2.5K
R39 470
R44 220
VR2 6.8V
C38 0.1
C40 4700 PF
T10
C41 0.1
R42 2.7K
C42 0.1
C44 4700 PF
T11
C45 0.1
C37 0.1
Q6 3N200
R40 50
Q7 2N5943
R36 130
R38 500
C39 0.1
R41 22
R43 750
C43 0.033
R45 130
14
DS1
R46
EMERGENCY DETECT
E7
E8
IF-2 EMERGENCY
16 AMPLIFIER (13 DB)
+22 V
C31 0.1
T9
L9
C35 0.1
C33 0.01
R25 1.8K
R29 1.8K
L10
L11
C36 20 PF
LO-2 EMERGENCY
E5
E6
C30 5PF
Q4 2N5943
R27 27
Q5 2N5943
R31 50
R26 360
C32 0.1
R28 220
R30 560
C34 0.1
R32 220
R33 249
J11
TP4
R34 62

| HIGHEST DESIGNATION USED | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C45 | DS1 | E10 | FL1 | J11 | L11 | M2 | P1 | PSC1 | Q7 | R46 | T11 | TP4 | U2 | VR2 | Y1 |
| **DESIGNATION NOT USED** | | | | | | | | | | | | | | | |
| | | | | J6 | | | | | | R12,R13 | | TP2 | | | |

NOTES

1- ALL RESISTOR VALUES ARE IN OHMS.

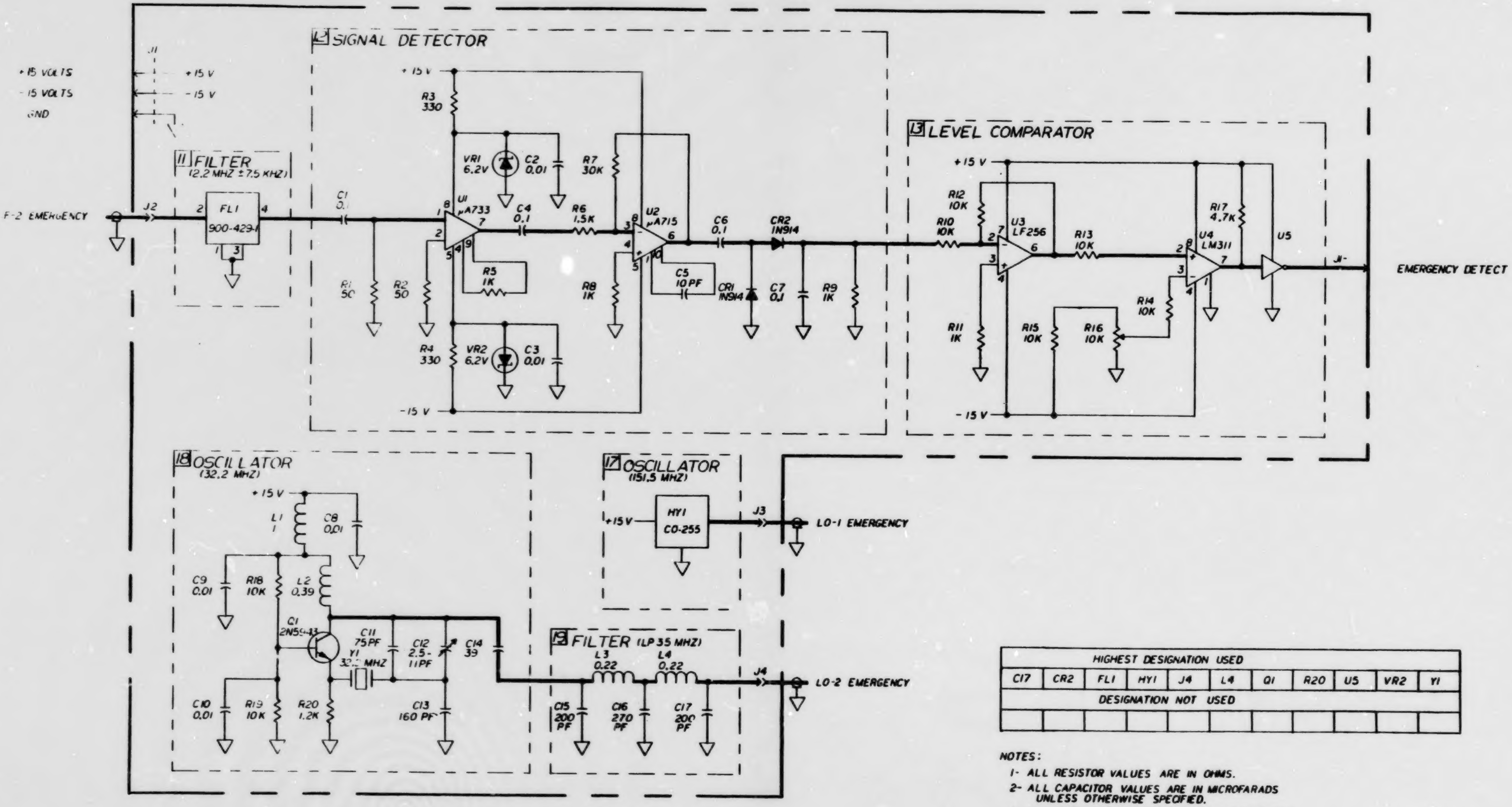
2- ALL CAPACITOR VALUES ARE IN MICROFARADS
UNLESS OTHERWISE SPECIFIED.

BAYLY

SCHEMATIC DIAGRAM
EMERGENCY CHANNEL MODULE

S.B. 12-1-26

714-0643.030 S24.C0-D


+15 VOLTS
-15 VOLTS
GND
J1
+15 V
-15 V
F-2 EMERGENCY
J2
11 FILTER
(12.2 MHZ ±7.5 KHZ)
FL1
900-429-1
2
4
1
3
12 SIGNAL DETECTOR
C1
0.1
R1
50
R2
50
R3
330
R4
330
VR1
6.2V
VR2
6.2V
C2
0.01
C3
0.01
U1
μA733
C4
0.1
R5
1K
R6
1.5K
R7
30K
R8
1K
U2
μA715
C5
10 PF
C6
0.1
CR1
1N914
CR2
1N914
C7
0.1
R9
1K
+15 V
-15 V
13 LEVEL COMPARATOR
R10
10K
R11
1K
R12
10K
U3
LF256
R13
10K
R14
10K
R15
10K
R16
10K
R17
4.7K
U4
LM311
U5
J1-
EMERGENCY DETECT
18 OSCILLATOR
(32.2 MHZ)
+15 V
L1
1
C8
0.01
C9
0.01
R18
10K
L2
0.39
Q1
2N5943
C11
75 PF
Y1
32.2 MHZ
C12
2.5-
11PF
C14
39
C10
0.01
R19
10K
R20
1.2K
C13
160 PF
17 OSCILLATOR
(151.5 MHZ)
+15V
HY1
CO-255
J3
LO-1 EMERGENCY
19 FILTER (LP 35 MHZ)
L3
0.22
L4
0.22
C15
200
PF
C16
270
PF
C17
200
PF
J4
LO-2 EMERGENCY

| HIGHEST DESIGNATION USED | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| C17 | CR2 | FL1 | HY1 | J4 | L4 | Q1 | R20 | U5 | VR2 | Y1 |
| DESIGNATION NOT USED | | | | | | | | | | |
| | | | | | | | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

3- ALL INDUCTOR VALUES ARE IN MICROHENRIES UNLESS OTHERWISE SPECIFIED.

BAYLY

SCHEMATIC DIAGRAM
EMERGENCY CHANNEL RCVR BACK

S.B. 12-1-27

714-0643,036 323,CD-D

## 2.3.11.3 ALIGNMENT

| | BLOCK # | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 2 | 3 | 4 | 6 | 7 | 10 | 13 | 16 | 18 |
| Adjusters | C1 | R5<br>R8 | L3<br>T4 | T5<br>T6<br>L4<br>L5<br>L6<br>L7<br>L8<br>C16<br>C19 | R19<br>T7<br>T8 | R40<br>T10<br>T11 | R16 | R31 | C12 |

a The alignment of block # 2, # 4 and # 6 (filters) is done according to the specifications written in 2.3.10.4.

b The alignment of block # 3, # 7, # 10, # 16 and # 19 is done by tuning the "LC Tank" and by adjusting to a specified amplitude response at the center frequency (see 2.3.11.4).

c Block 13

With a target at 3 μV/m and 121.5 MHz, adjust R16 for an emergency detect ON.

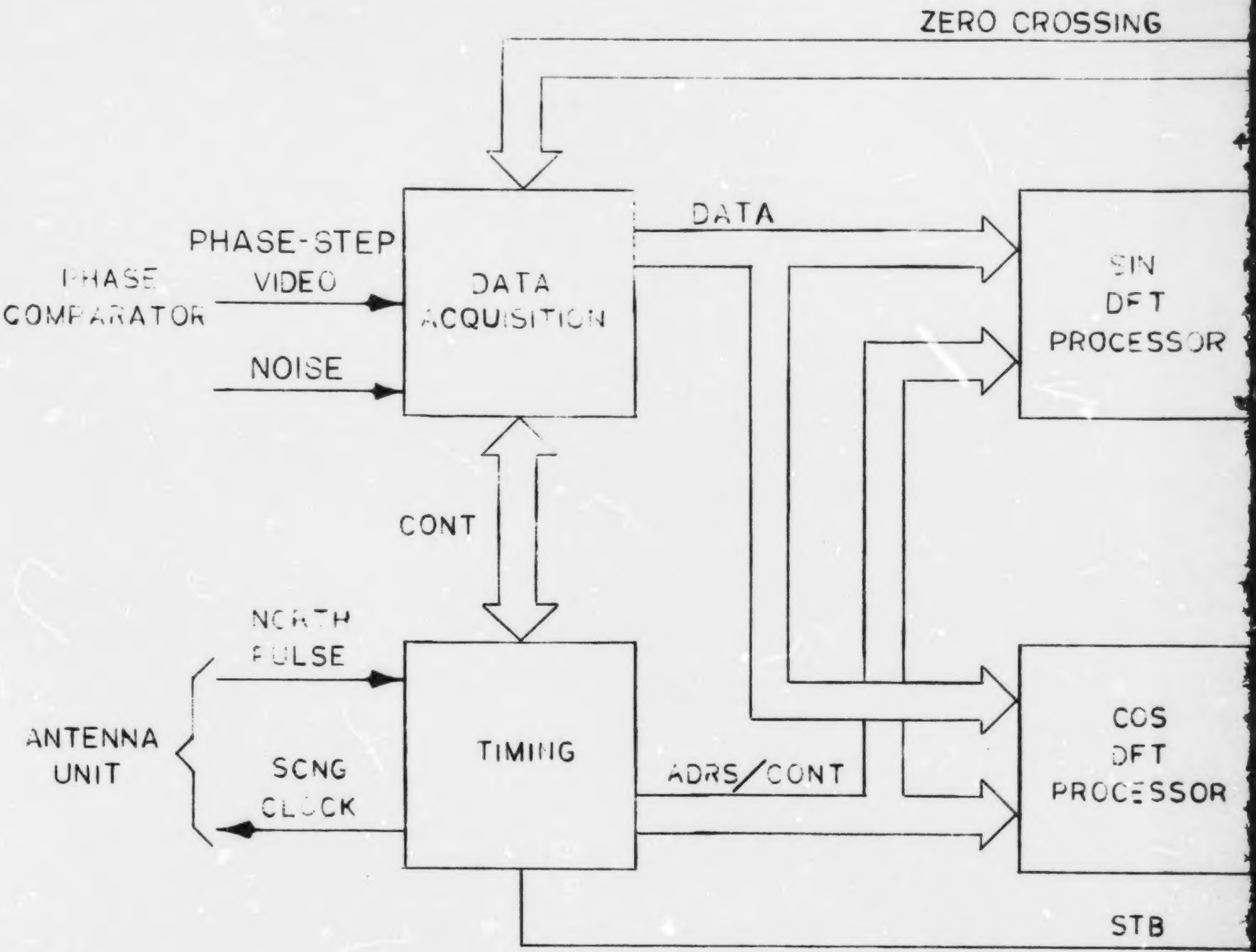
## 2.3.11.4 SPECIFICATIONS

| | | BLOCK # | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 2 | 3 | 4 | 6 | 7 | 10 | 16 | 18 |
| Impedance INPUT | (ohms) | 50 | 50 | 50 | 50 | 50 | 50 | 50 | |
| OUTPUT | (ohms) | 50 | 50 | 50 | 50 | 50 | 50 | 50 | 50 |
| Gain - Loss | (dB) | | 14 | | | 30 | 20 | 13 | |
| Band-Pass (1 dB) | (MHz) | | | 117 @ 137 | | | | | |
| (3 dB) | (KHz) | ± 50 | | | ± 400 | | | | |
| Center Frequency | (MHz) | 121.5 | | | | | | | 32.2 |

## 2.4 BEARING PROCESSOR MODULES

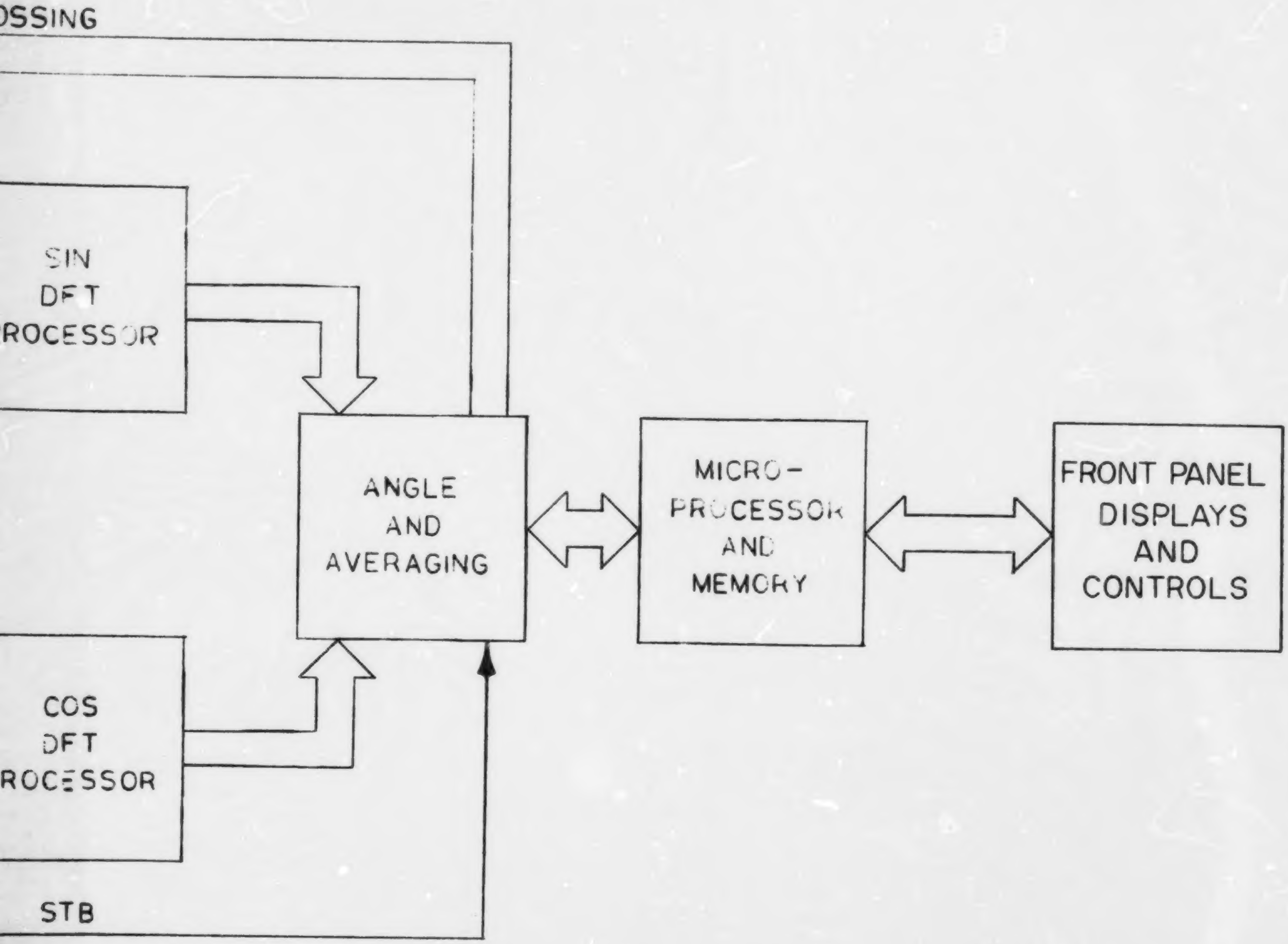
**Index**

2.4.1 Data Acquisition
2.4.2 DFT Processor
2.4.3 Angle and Average
2.4.4 Microprocessor and Memory
2.4.5 Timing and Control


ZERO CROSSING
DATA
PHASE-STEP
VIDEO
PHASE
COMPARATOR
DATA
ACQUISITION
NOISE
SIN
DFT
PROCESSOR
CONT
NORTH
PULSE
ANTENNA
UNIT
SCNG
CLOCK
TIMING
ADRS/CONT
COS
DFT
PROCESSOR
STB

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document
neither used, copied, reproduced or otherwise
nor its contents communicated to others.

66-0643.035 330.BD-B


OSSING
SIN
DFT
ROCESSOR
ANGLE
AND
AVERAGING
MICRO-
PROCESSOR
AND
MEMORY
FRONT PANEL
DISPLAYS
AND
CONTROLS
COS
DFT
ROCESSOR
STB

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| B | REVISED | [illegible] | |

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

ne of
document may be
erwise dealt with,

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
BEARING PROCESSOR

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. | |
|---|---|---|---|---|---|
| L.T. | 83-01-26 | LA | | 66-0643.035 330.BD-B | B |

## 2.4.1 DATA ACQUISITION

The main purpose of the Data Acquisition Card is to sample and convert the phase detector output to a 12 bit number.

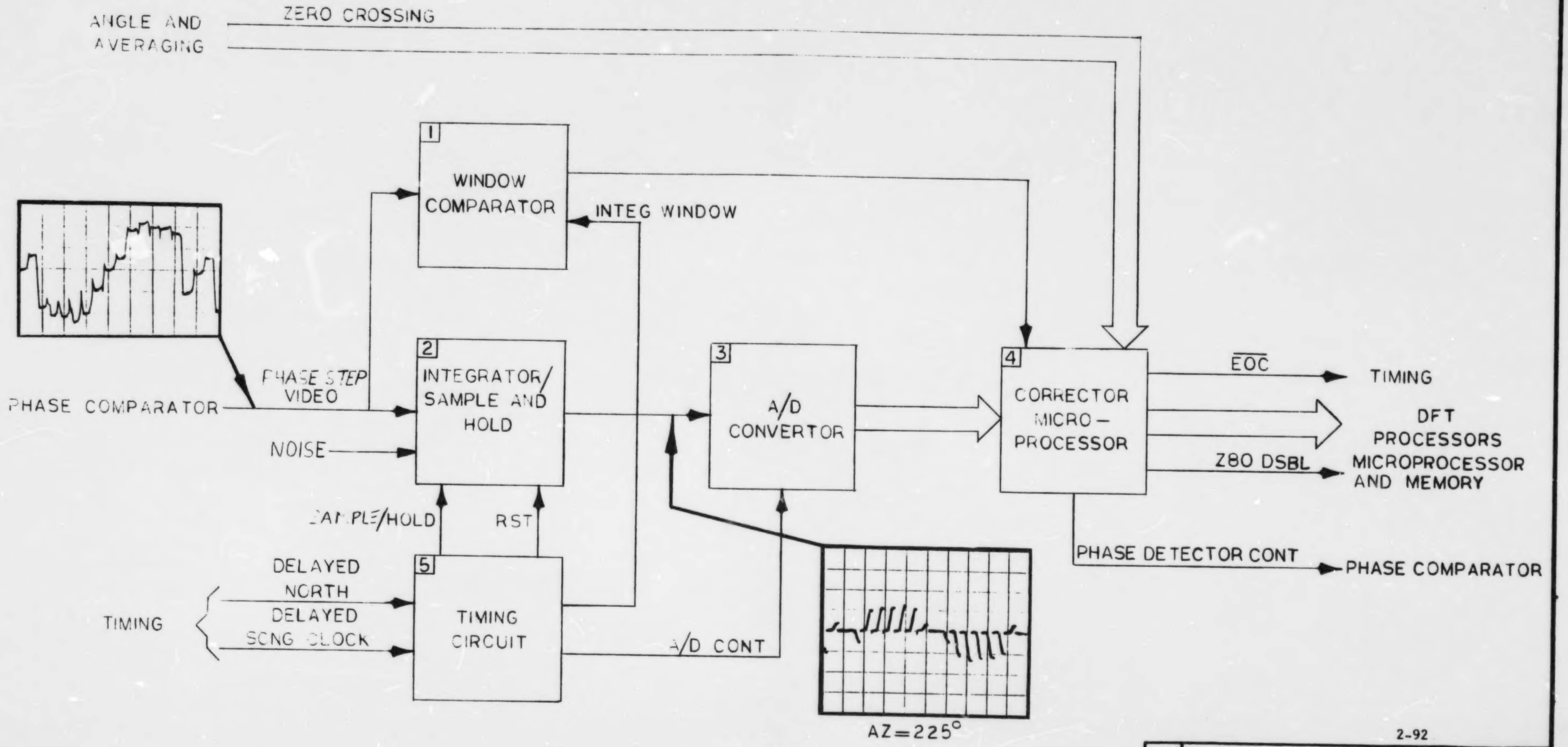
To reduce the effect of noise, the phase is integrated for a time window which covers the flat and transient free part at the time a particular dipole pair is selected. The result of this integration, which is proportional to the phase difference for the selected pair, is sampled and digitized (by a 12 bit A to D converter) and is brought out to a correction processor (corrector).

This correction is necessary because of the phase detector sensing angles outside its -180° to + 180° range.

Such large phase angles may occur because of the large antenna dipole spacing designed for higher sensitivity, further augmented by noise and harmonic distortions of the antenna pattern.

The corrector microprocessor observes the phase signal for one scan (reference scan) and identifies the samples to be corrected. These samples are then corrected and brought out to the angle calculator in the course of the following "n" scans (measurement scans) where "n" is the averaging constant over which the finding of the measurement scans are averaged.

The correction is done by shifting the phase detector range from ±180° to 0° to 360° (or -360° to 0°) for the range where the phase was more than 180° (or -180°). The value of the shifted samples is then added to 180° (or -180° whichever is the case) before feeding them to the angle calculation.


ANGLE AND AVERAGING
ZERO CROSSING
1
WINDOW COMPARATOR
INTEG WINDOW
PHASE STEP VIDEO
PHASE COMPARATOR
NOISE
2
INTEGRATOR/ SAMPLE AND HOLD
3
A/D CONVERTOR
4
CORRECTOR MICRO-PROCESSOR
EOC
TIMING
DFT PROCESSORS MICROPROCESSOR AND MEMORY
Z80 DSBL
PHASE DETECTOR CONT
PHASE COMPARATOR
SAMPLE/HOLD
RST
DELAYED NORTH
DELAYED SONG CLOCK
TIMING
5
TIMING CIRCUIT
A/D CONT
AZ=225°

| REV NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

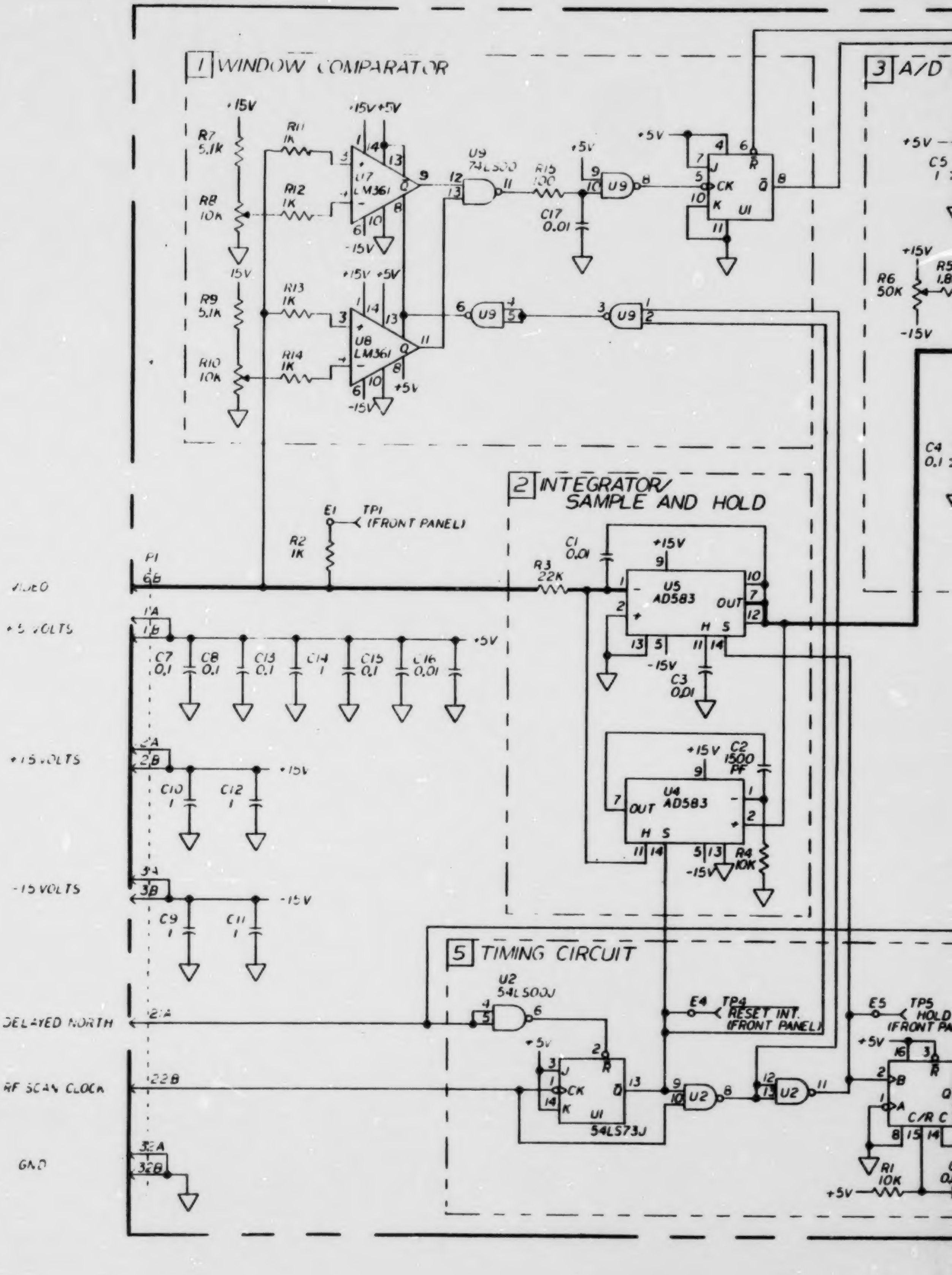
**BAYLY** ENGINEERING LTD a member of

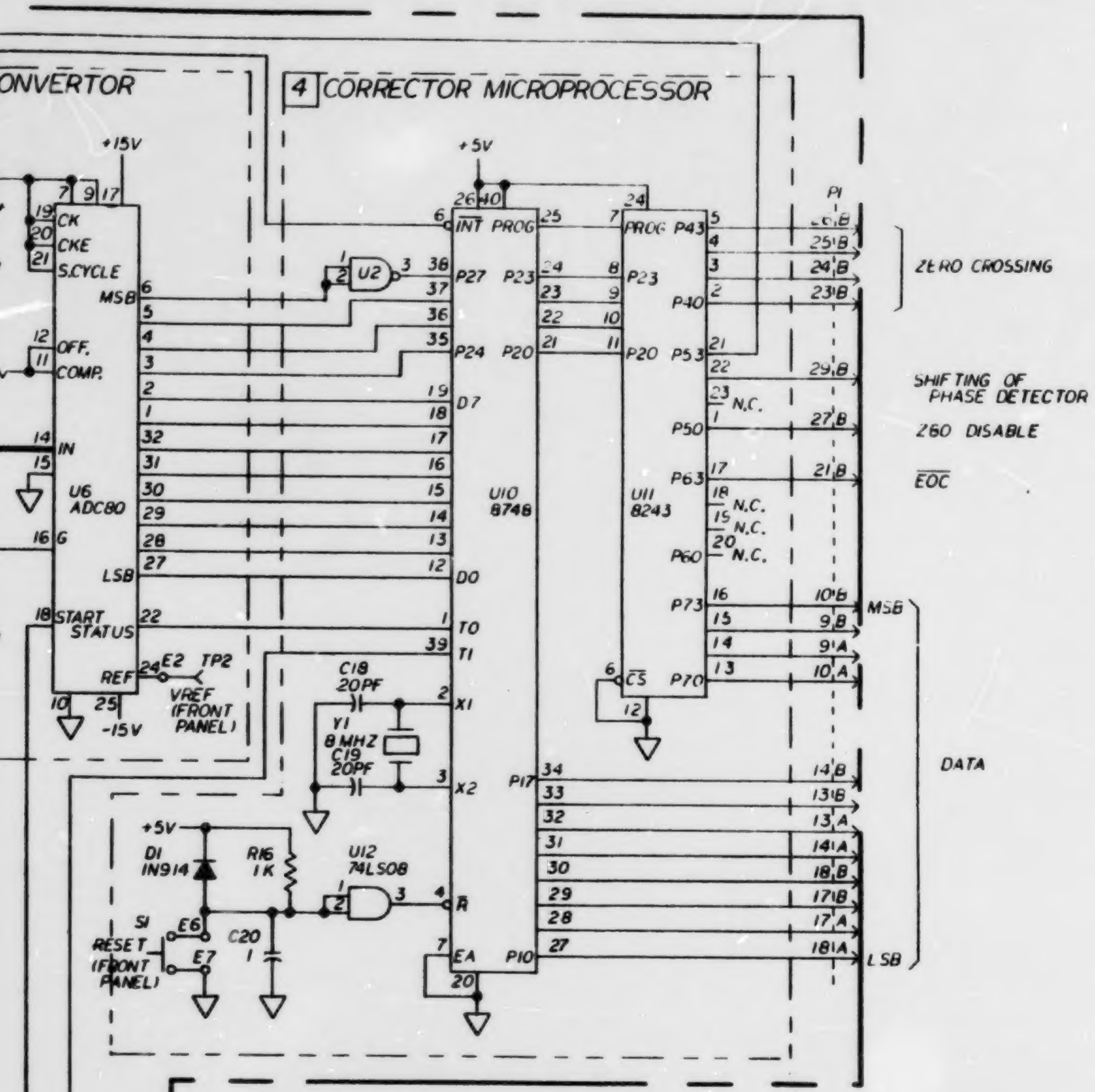
TITLE
BLOCK DIAGRAM
DATA ACQUISITION

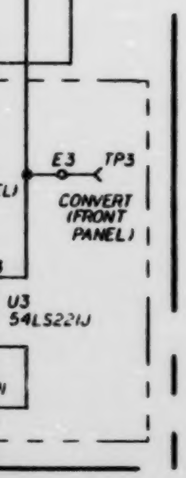
| UNLESS OTHERWISE SPECIFIED TOLERANCES DECIMALS ± ANGLES ± ° | DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|---|
| | X.T. | 83-01-31 | L.A | | 66-0643.027 966.BD-B |

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

K&E CRYSTALLENE


1 WINDOW COMPARATOR
2 INTEGRATOR/ SAMPLE AND HOLD
3 A/D
5 TIMING CIRCUIT
R7 5.1K
R8 10K
R9 5.1K
R10 10K
R11 1K
R12 1K
R13 1K
R14 1K
U7 LM361
U8 LM361
U9 74LS00
R15 100
C17 0.01
U1
R6 50K
R5 1.8
C5
C4 0.1
E1 TP1 (FRONT PANEL)
R2 1K
P1 6B
VIDEO
R3 22K
C1 0.01
U5 AD583
C3 0.01
U4 AD583
C2 1500 PF
R4 10K
+5 VOLTS
+15 VOLTS
-15 VOLTS
C7 0.1
C8 0.1
C13 0.1
C14 1
C15 0.1
C16 0.01
C10 1
C12 1
C9 1
C11 1
DELAYED NORTH
RF SCAN CLOCK
GND
1A
1B
2A
2B
3A
3B
21A
22B
32A
32B
U2 54LS00J
U1 54LS73J
E4 TP4 RESET INT. (FRONT PANEL)
E5 TP5 HOLD (FRONT PA
R1 10K
+5V
+15V
-15V


ONVERTOR
4 CORRECTOR MICROPROCESSOR
+15V
+5V
CK
CKE
S.CYCLE
MSB
OFF.
COMP.
IN
U6
ADC80
G
LSB
START
STATUS
REF
E2 TP2
VREF
(FRONT
PANEL)
-15V
U2
INT PROG
P27 P23
P24 P20
D7
D0
T0
T1
X1
X2
U10
8748
P17
P10
R
EA
C18
20PF
Y1
8MHZ
C19
20PF
+5V
D1
IN914
R16
1K
U12
74LS08
S1
RESET
(FRONT
PANEL)
E6
E7
C20
1
PROG P43
P23
P40
P20 P53
P50
P63
P60
P73
P70
CS
U11
8243
N.C.
N.C.
N.C.
N.C.
P1
26 B
25 B
24 B
23 B
29 B
27 B
21 B
10 B
9 B
9 A
10 A
14 B
13 B
13 A
14 A
18 B
17 B
17 A
18 A
ZERO CROSSING
SHIFTING OF
PHASE DETECTOR
Z60 DISABLE
EOC
MSB
DATA
LSB


E3 TP3
CONVERT
(FRONT
PANEL)
U3
54LS221J

| HIGHEST DESIGNATION USED | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| C20 | D1 | E7 | F1 | R16 | S1 | TP5 | U12 | Y1 |
| DESIGNATION NOT USED | | | | | | | | |
| | | | | | | | | |

NOTES:

1 - ALL RESISTOR VALUES ARE IN OHMS
2 - ALL CAPACITOR VALUES ARE IN MICROFARADS

| IC'S SUPPLY DISTRIBUTION | | |
|---|---|---|
| DESIGNATION | GND | +5V |
| U2, U9, U12 | PIN 7 | PIN 14 |

BAYLY

SCHEMATIC DIAGRAM
DATA ACQUISITION

SB 83-2-4 L.A

66-0543.027 986.CD-0

### 2.4.1.3 TEST

a. Check that timing between signals correspond to the diagram of figure 1.

b. Integrator/Sample and Hold check.

   1. Initial conditions :

      Tuning : 118.250 MHz
      Field strength : 1 mV/m
      (received)
      Azimuth : 225°

   2. Set-up : See figure 2.

   3. Connect oscilloscope's channel 1 to point Ⓐ and channel 2 to point Ⓑ .

      Point Ⓐ is the output of the PHASE DETECTOR.
      Point Ⓑ is U6-14 on DATA ACQUISITION.

      Also connect oscilloscope's external trigger input to NORTH REFERENCE on front panel of timing.

   4. Setting of oscilloscope :

      Trigger : external (+)
      Horizontal : 1.5 ms/DIV
      Vert. CH.1 : 2V/DIV
      Vert. CH.2 : 0.5V/DIV

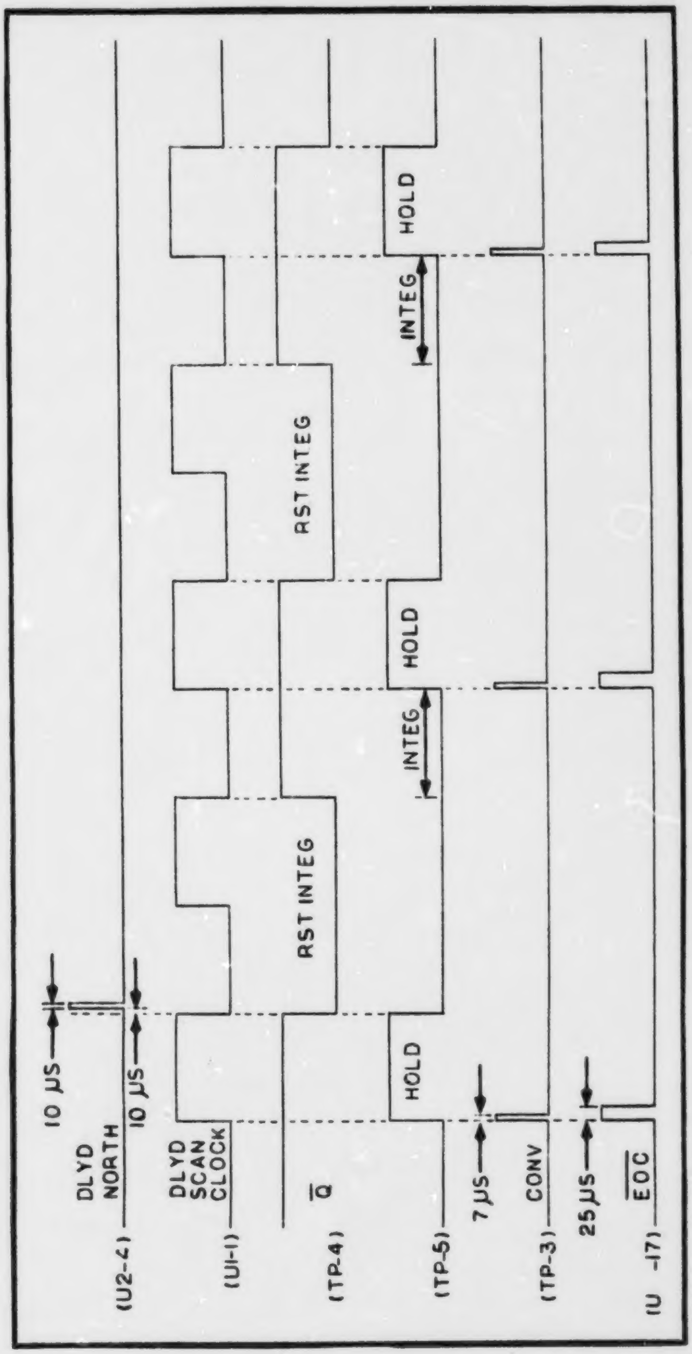
      Signal strength : 9V P.-P.

   5. Check that waveforms are similar to figure 3.

c. Window comparator adjustment :

   1. Connect a DMM on cursor of R   and adjust this latter to read +3.8V.

   2. Connect a DMM on cursor of R   and ajust this latter to read -3.8V.



DLYD NORTH
(U2-4)
10 µS
10 µS
DLYD SCAN CLOCK
(U1-1)
$\overline{Q}$
(TP-4)
HOLD
RST INTEG
INTEG
RST INTEG
INTEG
HOLD
HOLD
(TP-5)
7 µS
CONV
(TP-3)
25 µS
$\overline{EOC}$
(U -17)

Figure 1

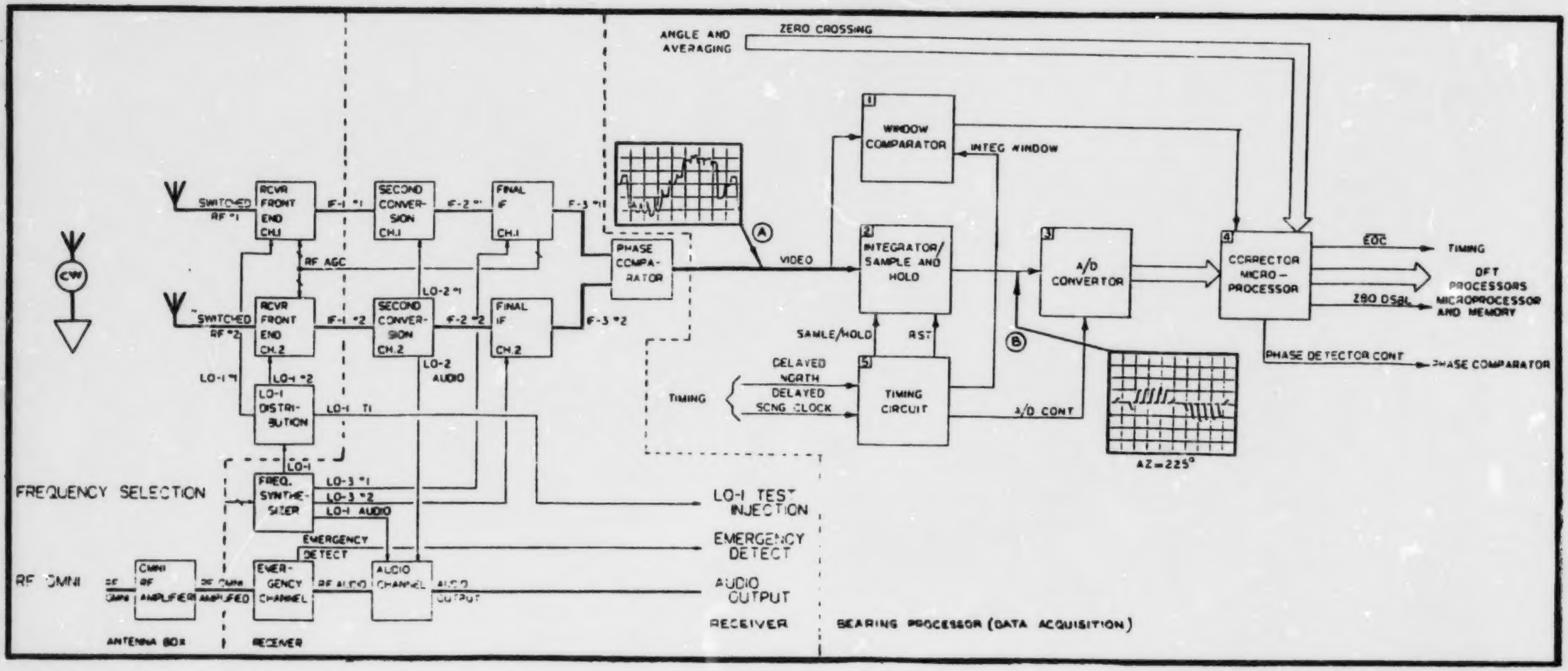

ANGLE AND AVERAGING
ZERO CROSSING
SWITCHED RF #1
SWITCHED RF #2
RCVR FRONT END CH.1
RCVR FRONT END CH.2
IF-1 #1
IF-1 #2
RF AGC
SECOND CONVERSION CH.1
SECOND CONVERSION CH.2
IF-2 #1
IF-2 #2
LO-2 #1
LO-2 AUDIO
FINAL IF CH.1
FINAL IF CH.2
IF-3 #1
IF-3 #2
PHASE COMPARATOR
CW
LO-1 #1
LO-1 #2
LO-1 DISTRIBUTION
LO-1 T1
LO-1
FREQUENCY SELECTION
FREQ. SYNTHESIZER
LO-3 #1
LO-3 #2
LO-1 AUDIO
EMERGENCY DETECT
RF OMNI
RF OMNI
OMNI RF AMPLIFIER
RF OMNI AMPLIFIED
EMERGENCY CHANNEL
RF AUDIO
AUDIO CHANNEL
AUDIO OUTPUT
ANTENNA BOX
RECEIVER
LO-1 TEST INJECTION
EMERGENCY DETECT
AUDIO OUTPUT
RECEIVER
A
VIDEO
1
WINDOW COMPARATOR
INTEG WINDOW
2
INTEGRATOR/ SAMPLE AND HOLD
SAMLE/HOLD
RST
5
TIMING CIRCUIT
TIMING
DELAYED NORTH
DELAYED SCNG CLOCK
B
A/D CONT
3
A/D CONVERTOR
AZ=225°
4
CORRECTOR MICRO-PROCESSOR
EOC
TIMING
DFT PROCESSORS MICROPROCESSOR AND MEMORY
Z80 DSBL
PHASE DETECTOR CONT
PHASE COMPARATOR
BEARING PROCESSOR (DATA ACQUISITION)

Figure 2

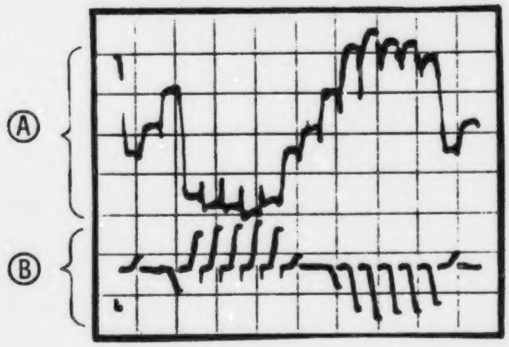


Figure 3

## 2.4.1.4 SOFTWARE

### Corrector Processor : program description

The corrector processor is part of the Data Acquisition board. This corrector is necessary because of the ambiguity due to the phase detector sensing angles outside the ± 180° range.

The output of the phase detector is a linear ramp going from approximately -6 volts for - 180°, to + 6 volts for + 180°. So if an angle goes from 180° to a value greater than 180°, then the output of the phase detector will drop from an output voltage of 6 volts to -6 volts. This is due to the fact that, for the phase detector, an angle greater than 180° is seen as an angle greater than - 180° (this is 360° shift : 190° - 360° =-170°).

A correction on the phase detector output must, therefore, be done to improve the accuracy. This is done by shifting the phase detector range from ± 180° to 0° to 360° (or - 360° to 0°).

As a result of the range shifting, the portion of the signal prone to foldback will be detected as shifted by 180° but, as a whole, with no swap and foldback.

As the scheme involves controlling the phase detector, than the sample to be corrected must be known before it is actually present at the phase detector input. This seems ambiguous as the sample must be read to know if correction is needed, and on the other hand, shifting of the phase detector must be accomplished before reading the sample. The following paragraph explains the correction algorithm.

The identification of the samples to be corrected is based on the assumption that the original phase signal never exceeds 240°.

Under such assumption, the folded back phase of the phase detector output falls in the 130° to 180° (or -130° to -180°) region. Therefore comparing the incoming sample levels to ± 120° identifies the samples to be corrected.

There is another anomaly observed for the portions of the phase signal in the vicinity of ± 180°. It can have noise spikes which may, or may not, fold back at the output of the phase detector. The phenomenon after integration produces average readouts in the good sample region (±130°) and no attempt will be made to correct them according to the first criterion.

To avoid the problem, a window comparator is used to sense the output of the phase detector (so, before the integrator). Upon sensing a readout close to 180° (or -180°) during the integration region, this circuit produces an interrupt to the corrector microprocessor. This interrupt identifies the sample as a bad sample to be corrected even if the microprocessor senses it as a good sample (in the ± 130° zone).

The observation to identify the good and bad sample is done during one scan, called the reference scan. One scan is defined as one complete antenna rotation, starting with the "north" dipole. The antenna is made of 16 different dipoles, so one scan produces 16 samples.

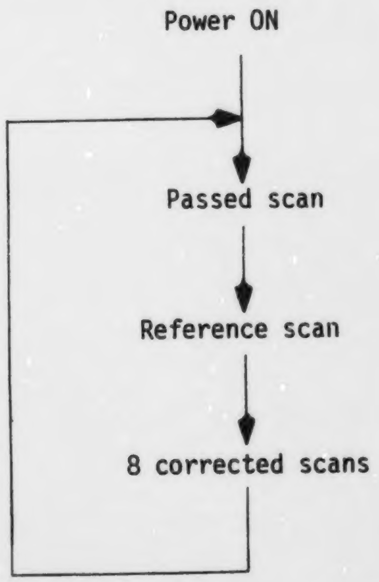
During the reference scan all 16 samples are read and compared to the limit of $130^0$ (or - $130^0$). If it is found outside the valid region of ± $130^0$, or identified by the window comparator as bad, then this samples is flagged as one to be corrected.

The following 8 scans use this information to decide if the phase detector needs to be shifted or not before the presence of the corresponding sample. When shifted, the corrected sample is read and the value of $180^0$ (or - $180^0$) is added to it before it is sent to the DFT card.

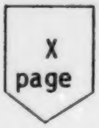
To decide if $180^0$ or - $180^0$ is to be added in the above correction, the relative position of the sample is required with respect to the main positive zero crossing of the signal. This zero crossing is, in fact, roughly equal to the target angle (bearing angle) and is calculated by the bearing processor in the previous measurement scan. It is reported as feedback to the corrector processor in the reference scan.

The above procedure, however, suffers from the lack of zero crossing report in the very first reference scan at the power up. Therefore, an initialization scan is required. During this scan, the corrector processor does nothing on the incoming samples but just passes them to the angle calculator. This non correcting scan will be repeated also after each 8 corrected scans (so before each reference scan).

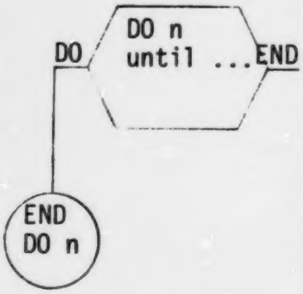
The main flow of the corrector program then looks like this :



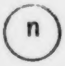
## FLOWCHART SYMBOLS



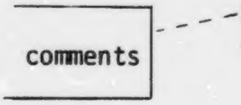
Off-page connector. The letter inside the symbol is used to differentiate between different connection. A letter is related to one specific input point. Page number is also included to ease the search.



Loop This symbol represents a loop, which is identified by number "n". The sequence of instruction which is done repetitevely in the loop is described starting on the side of the symbol marked "DO". The end of the sequence is identified by the termination circle. The number "n" inside the circle relates to the corresponding loop number. This sequence will be repeated as long as the condition specified after the word "until" is not met. When the condition is fulfilled, then the symbol output marked "END" is used.

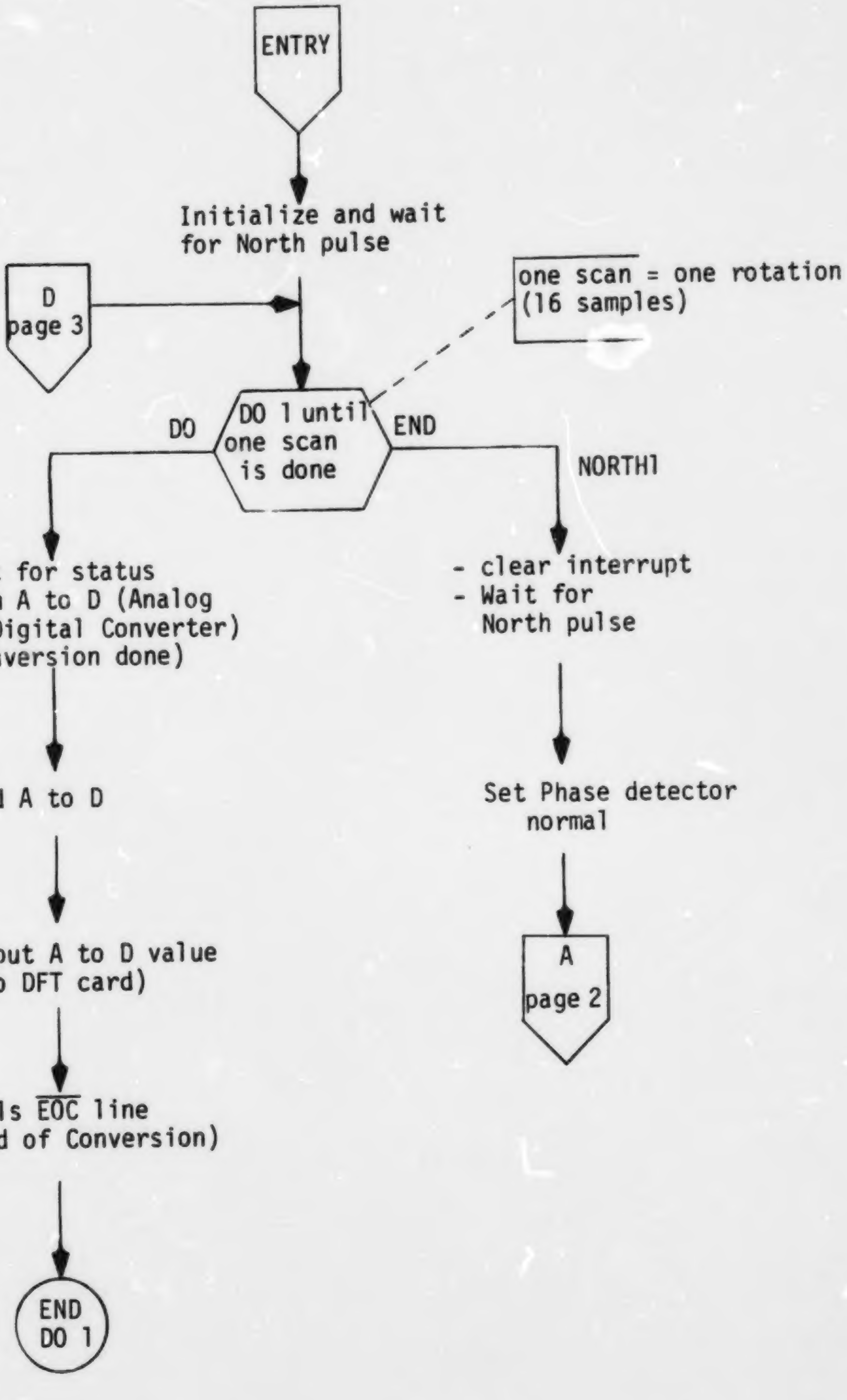


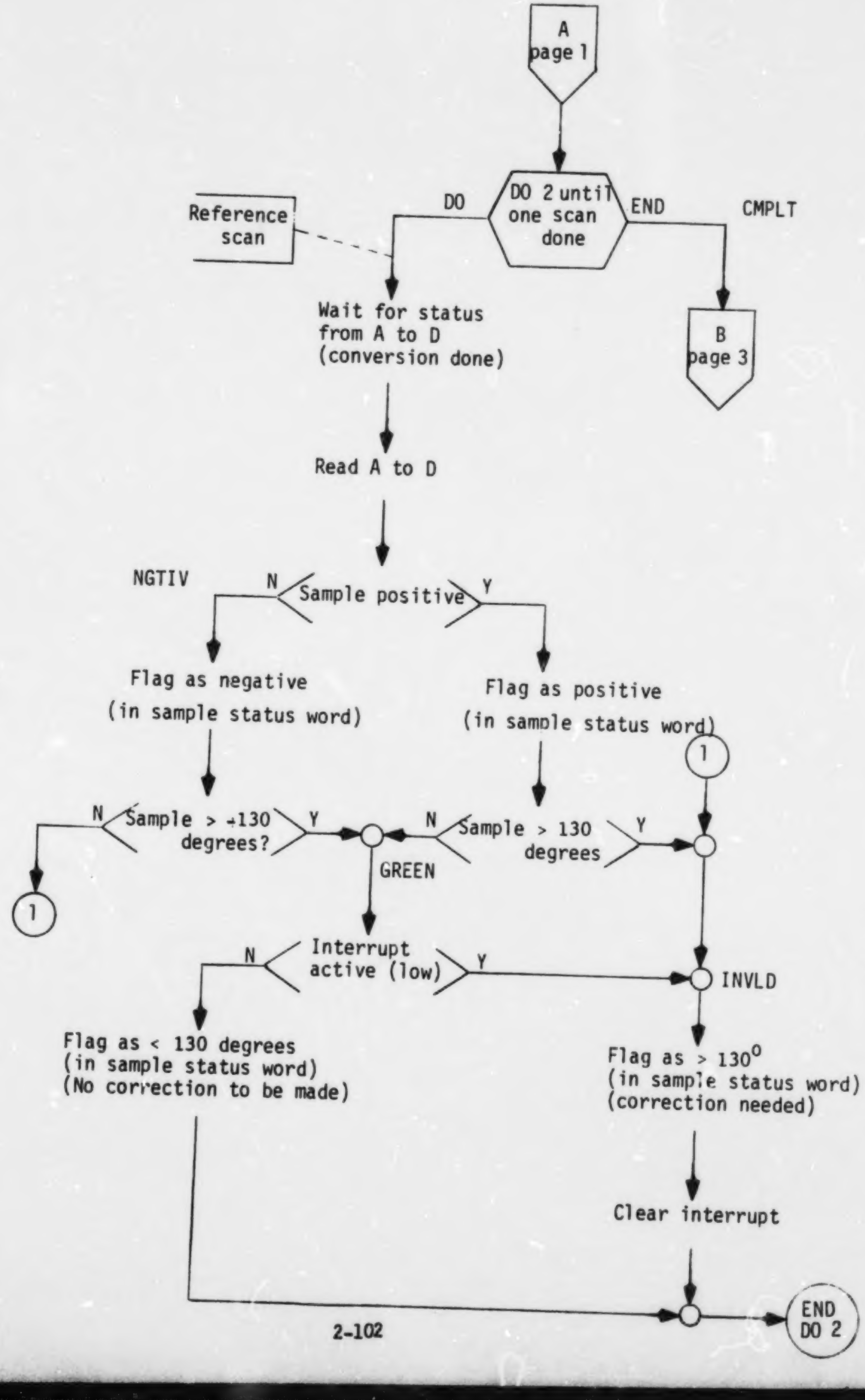
On-page connector. An arrow pointing to or from the bubble identifies the flow path. Connection is always done on the same page.

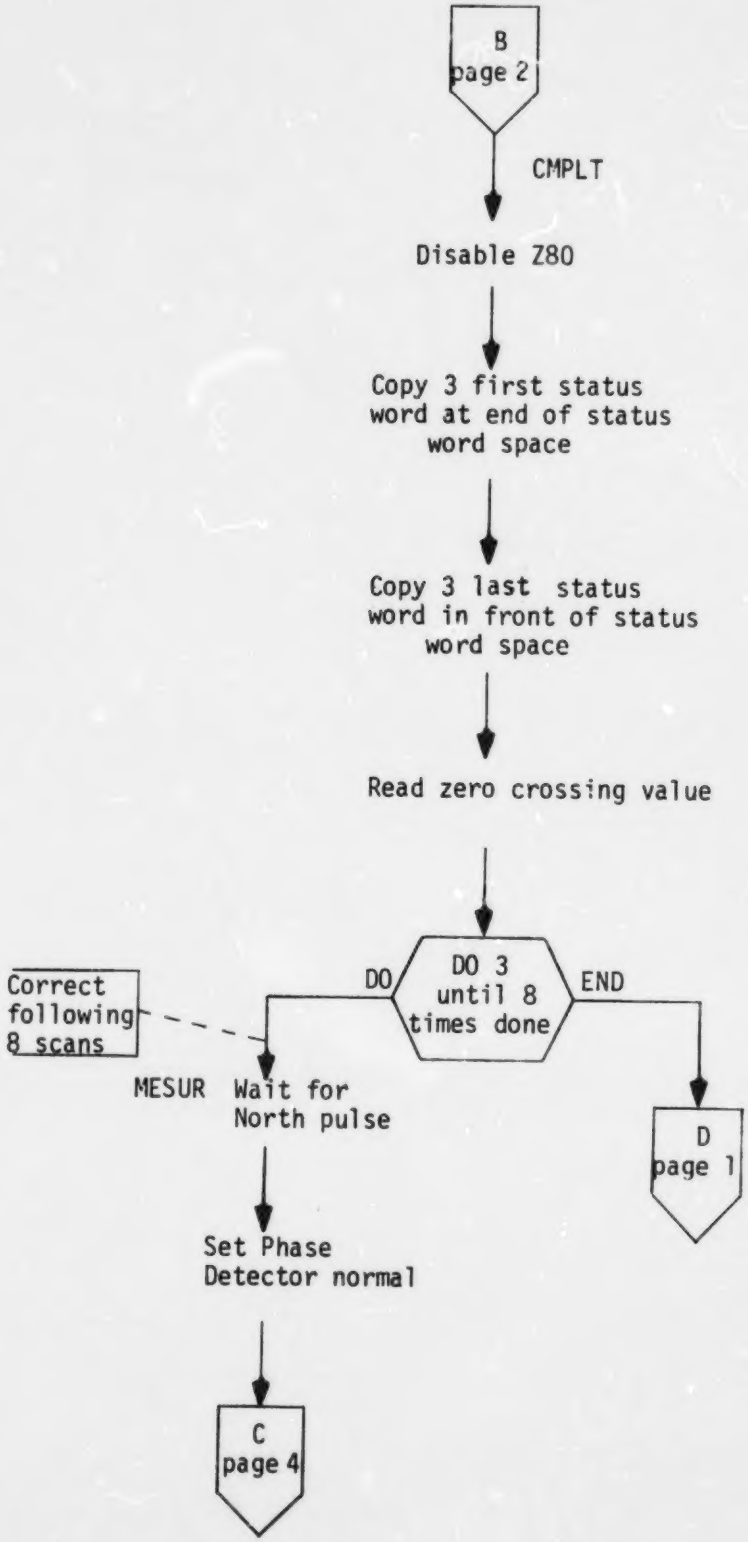


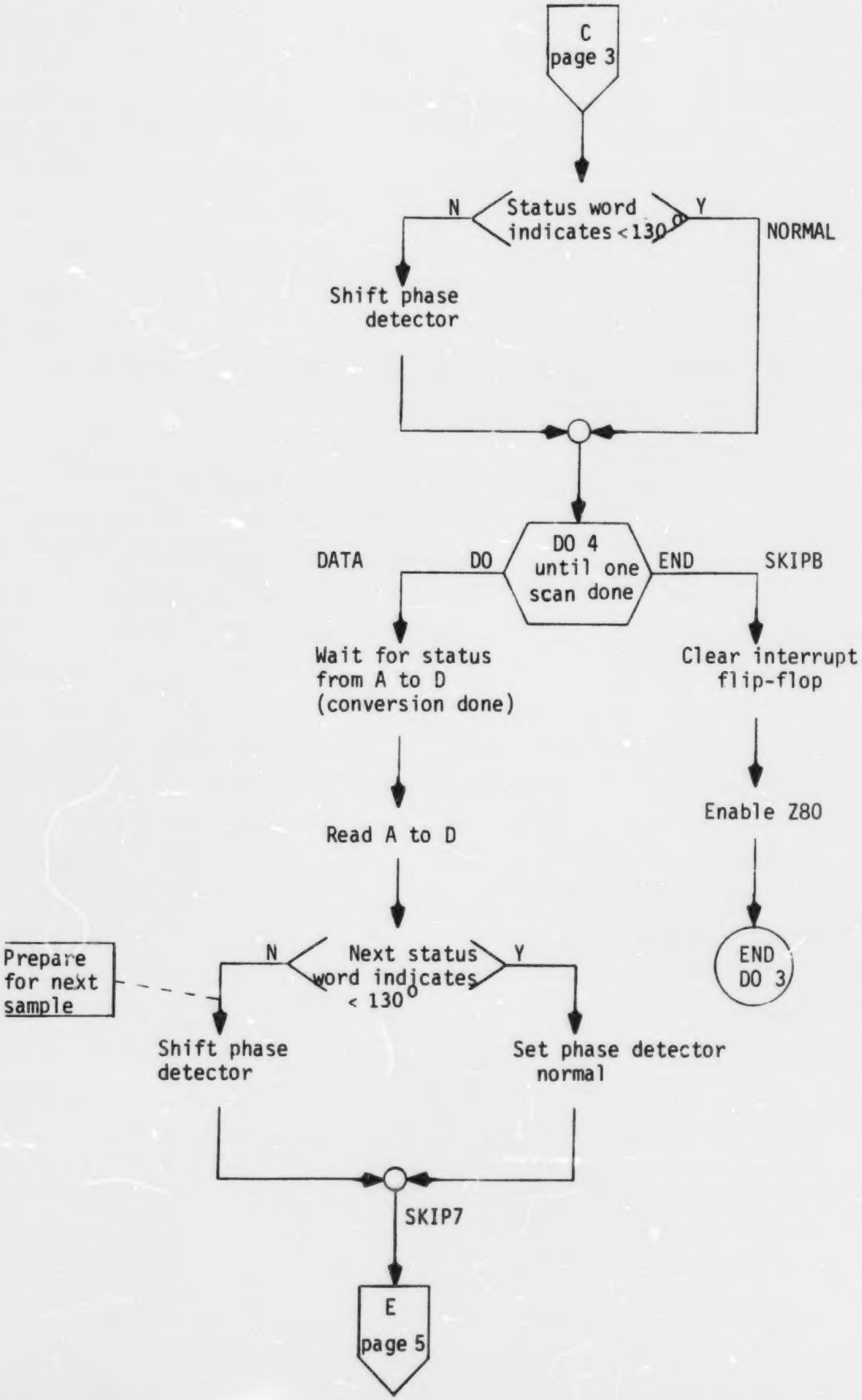
Dashed line without an arrowhead is used to provide comments.

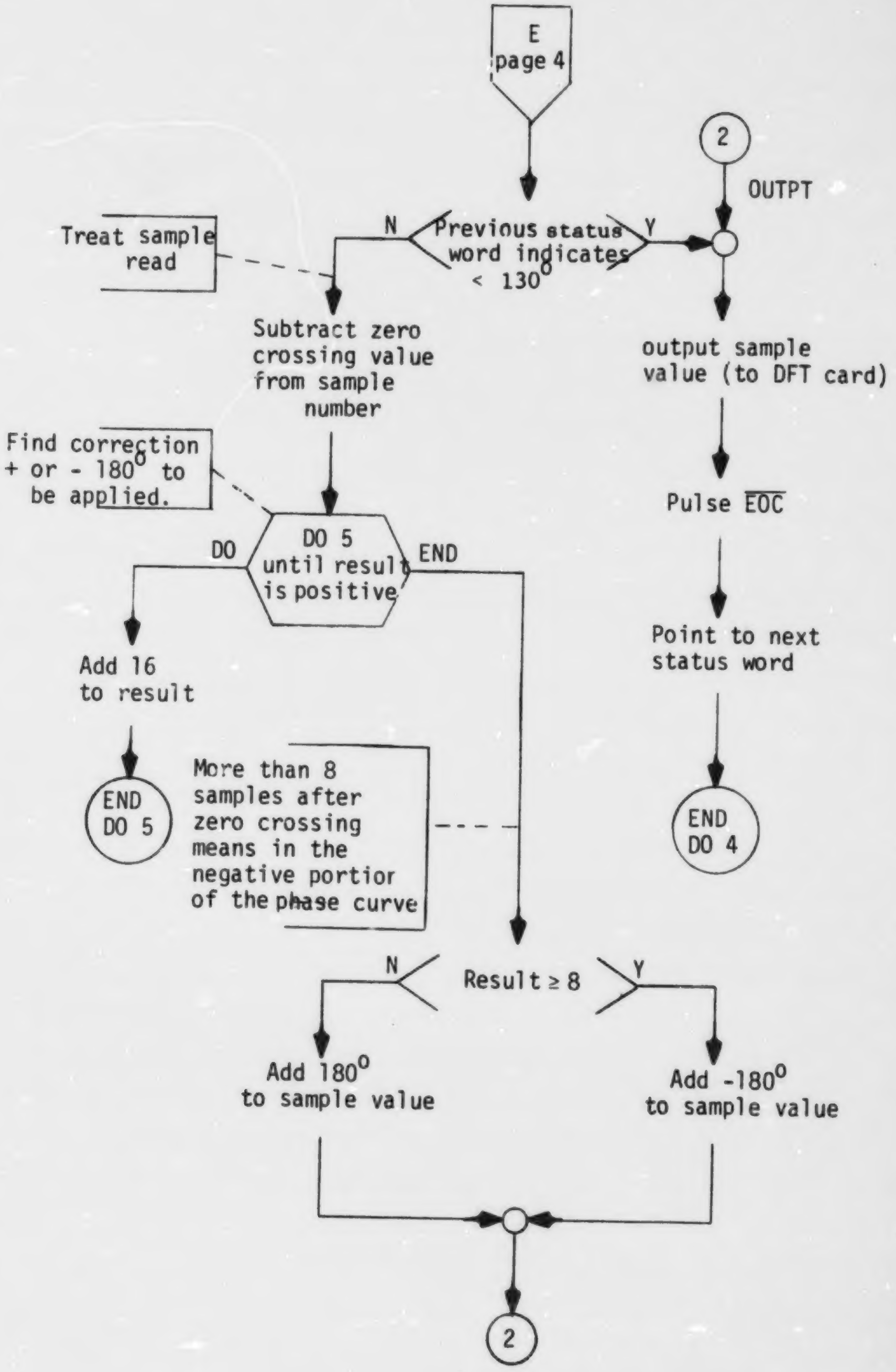
# DATA ACQUISITION FLOW CHART


ENTRY
Initialize and wait for North pulse
D page 3
one scan = one rotation (16 samples)
DO 1 until one scan is done
DO
END
NORTH1
Wait for status from A to D (Analog to Digital Converter) (conversion done)
Read A to D
output A to D value (to DFT card)
Pulls $\overline{EOC}$ line (End of Conversion)
END DO 1
- clear interrupt
- Wait for North pulse
Set Phase detector normal
A page 2


A
page 1
DO 2 until
one scan
done
DO
END
CMPLT
Reference
scan
B
page 3
Wait for status
from A to D
(conversion done)
Read A to D
NGTIV
N
Sample positive
Y
Flag as negative
(in sample status word)
Flag as positive
(in sample status word)
1
N
Sample > -130
degrees?
Y
N
Sample > 130
degrees
Y
1
GREEN
N
Interrupt
active (low)
Y
INVLD
Flag as < 130 degrees
(in sample status word)
(No correction to be made)
Flag as > 130°
(in sample status word)
(correction needed)
Clear interrupt
END
DO 2


B
page 2
CMPLT
Disable Z80
Copy 3 first status word at end of status word space
Copy 3 last status word in front of status word space
Read zero crossing value
DO
DO 3 until 8 times done
END
Correct following 8 scans
MESUR
Wait for North pulse
D
page 1
Set Phase Detector normal
C
page 4


C
page 3
Status word indicates < 130°
N
Y
NORMAL
Shift phase detector
DATA
DO
DO 4 until one scan done
END
SKIPB
Wait for status from A to D (conversion done)
Clear interrupt flip-flop
Enable Z80
Read A to D
END DO 3
Prepare for next sample
N
Next status word indicates < 130°
Y
Shift phase detector
Set phase detector normal
SKIP7
E
page 5


E
page 4
2
OUTPT
N
Previous status word indicates < 130°
Y
Treat sample read
Subtract zero crossing value from sample number
output sample value (to DFT card)
Find correction + or - 180° to be applied.
DO
DO 5 until result is positive
END
Pulse $\overline{EOC}$
Point to next status word
Add 16 to result
More than 8 samples after zero crossing means in the negative portion of the phase curve
END DO 5
END DO 4
N
Result ≥ 8
Y
Add 180° to sample value
Add -180° to sample value
2

Corrector microprocessor

input TO : status coming from the Analog to Digital converter (A to D)
- 0 : conversion done
- 1 : busy

input TI : North pulse
- 0 : not at north position
- 1 : North indication

input INT : Window comparator
- 0 : sample is to be corrected
- 1 : no correction (good sample)

Status word : used to memorize if a sample needs to be corrected or not.

bit 0 : 0 if sample < $130^0$ (or > $-130^0$) (no correction)
1 if sample > $130^0$ (or < $-130^0$) (correction needed)

bit 1 : 0 if sample positive (+)
1 if sample negative (-)

bit 2 to 7 : not used.

status word for sample 1 located at RAM address 40 ($28_{16}$)
status word for sample 2 located at RAM address 41 ($29_{16}$)
: : :
status word for sample 16 located at RAM address 55 ($37_{16}$)

```
                  ;      ***********************************************
                  ;      *                                             *
                  ;      *  D. F. CORRECTION PROGRAM                   *
                  ;      *                                             *
                  ;      ***********************************************


                         ;
                         ; Initialization
                         ;
      0000    >          ORG 0
0000 15           RSTRT  DIS I                 ;DISABLE INTERRUPTS
0001 35                  DIS TCNTI
0002 C5                  SEL RB0
0003 27                  CLR A
0004 AD                  MOV R5,A
0005 00                  NOP
0006 00                  NOP
0007 2308                MOV A,#08H
0009 3E                  MOVD P6,A
000A 00                  NOP
000B 00                  NOP
000C 00                  NOP
000D 00                  NOP
000E 2304                MOV A,#00000100B      ;GO TO INITIALIZATION SCAN
0010 3D                  MOVD P5,A             ;PHASE DETECTOR NORMAL
0011 00                  NOP
0012 00                  NOP
0013 00           INISC  NOP
0014 4613     >          JNT1 INISC            ;WAIT FOR NORTH PULSE

                         ;
                         ; Passed Scan
                         ;

0016 BA00         PASS   MOV R2,#00
0018 00                  NOP
0019 00                  NOP
001A 361E     >   INPUT  JT0 NEWIN
001C 041A     >          JMP INPUT             ;WAIT FOR STATUS FROM A TO D
001E 00           NEWIN  NOP                   ;GET NXT SAMPLE
001F 361E     >          JT0 NEWIN
0021 97                  CLR C
0022 08                  INS A,BUS
0023 0301                ADD A,#01
0025 39                  OUTL P1,A             ;AND OUTPUT IT TO DFT CARD
0026 00                  NOP
0027 0A                  IN A,P2
0028 47                  SWAP A
0029 1300                ADDC A,#0
002B 530F                ANL A,#0FH
002D 3F                  MOVD P7,A
002E 00                  NOP
```

```
00054 002F 00                  NOP
00055 0030 27                  CLR A
00056 0031 3E                  MOVD P6,A            ;ACTIVATE EOC (=0)
00057 0032 00                  NOP
00058 0033 00                  NOP
00059 0034 00                  NOP
00060 0035 00                  NOP
00061 0036 00                  NOP
00062 0037 00                  NOP
00063 0038 2308                MOV A,#08H
00064 003A 3E                  MOVD P6,A            ;EOC=1
00065 003B FA                  MOV A,R2             ;CHECK IF CMPLETE
00066 003C 17                  INC A
00067 003D 9242    >           JB4 NORTH1
00068 003F AA                  MOV R2,A
00069 0040 041A    >           JMP INPUT
00070                          ;
00071                          ;Clear interrupt
00072                          ;
00073 0042 2307         NORTH1 MOV A,#7
00074 0044 9D                  ANLD P5,A
00075 0045 00                  NOP
00076 0046 00                  NOP
00077 0047 2308                MOV A,#8
00078 0049 8D                  ORLD P5,A
00079 004A 00                  NOP
00080 004B 00                  NOP
00081 004C 00                  NOP
00082
00083
00084                          ;
00085                          ; Wait for north pulse
00086                          ;
00087 004D 00           NORTH  NOP                  ;WAIT FOR NORTH PULSE
00088 004E 464D    >           JNT1 NORTH
00089 0050 FD                  MOV A,R5             ;8 CORRECTED SCAN DONE ?
00090 0051 9655    >           JNZ MESUR1           ;IF NOT ZERO MEASUREMENT
00091 0053 0459    >           JMP RFSCN
00092 0055 04F3    >    MESUR1 JMP MESUR
00093 0057 00                  NOP
00094 0058 00                  NOP
00095
00096
00097                          ;
00098                          ; Reference Scan
00099                          ;
00100 0059 230C         RFSCN  MOV A,#0CH           ;MAKE PD NORMAL
00101 005B 8D                  ORLD P5,A
00102 005C B928                MOV R1,#40
00103 005E BA00                MOV R2,#0
00104 0060 00                  NOP
00105 0061 00                  NOP
00106 0062 00                  NOP
```

```
00107 0063 00                 NOP
00108 0064 00                 NOP
00109
00110 0065 3669   >  MAIN     JT0 NEWDT               ;WAIT FOR STATUS FROM A TO D
00111 0067 0465   >           JMP MAIN
00112 0069 00        NEWDT    NOP
00113 006A 3669   >           JT0 NEWDT
00114
00115 006C 00                 NOP
00116 006D 00                 NOP
00117 006E 97                 CLR C
00118 006F 08                 INS A,BUS               ;READ AND STORE
00119 0070 0301                ADD A,#01H
00120 0072 AE                 MOV R6,A
00121 0073 0A                 IN A,P2
00122 0074 00                 NOP
00123 0075 00                 NOP
00124 0076 47                 SWAP A
00125 0077 1300               ADDC A,#00H
00126 0079 530F               ANL A,#00001111B
00127 007B 00                 NOP
00128 007C 00                 NOP
00129 007D 00                 NOP
00130 007E 00                 NOP
00131
00132 007F AF                 MOV R7,A
00133 0080 72B7   >           JB3 NGTIV               ;SEE IF POSITIVE
00134 0082 F1                 MOV A,@R1               ;IF POSITIVE MARK +
00135 0083 53FD               ANL A,#11111101B
00136 0085 A1                 MOV @R1,A
00137 0086 FE                 MOV A,R6                ;COMPARE TO 130
00138 0087 97                 CLR C
00139 0088 0360               ADD A,#LSM13
00140 008A FF                 MOV A,R7
00141 008B 130B               ADDC A,#MSM13
00142 008D 729F   >           JB3 GREEN               ;IF SMALLER MARK G
00143 008F 2307      INVLD    MOV A,#00000111B        ;CLEAR THE I LATCH
00144 0091 9D                 ANLD P5,A
00145 0092 F1                 MOV A,@R1
00146 0093 4301               ORL A,#01H
00147 0095 A1                 MOV @R1,A
00148 0096 2308               MOV A,#00001000B
00149 0098 8D                 ORLD P5,A
00150 0099 04A9   >           JMP CHECK
00151 009B 00                 NOP
00152 009C 00                 NOP
00153 009D 00                 NOP
00154 009E 00                 NOP
00155
00156 009F 868F   >  GREEN    JNI INVLD               ;CHECK INTERRUPT
00157 00A1 F1                 MOV A,@R1
00158 00A2 53FE               ANL A,#11111110B
00159 00A4 A1                 MOV @R1,A
```

```
00160 00A5 00                 NOP
00161 00A6 00                 NOP
00162 00A7 00                 NOP
00163 00A8 00                 NOP
00164
00165 00A9 FA         CHECK   MOV A,R2
00166 00AA 17                 INC A
00167 00AB 92C6    >          JB4 CMPLT
00168 00AD AA                 MOV R2,A
00169 00AE 0328               ADD A,#40
00170 00B0 A9                 MOV R1,A
00171 00B1 0465    >          JMP MAIN
00172 00B3 00                 NOP
00173 00B4 00                 NOP
00174 00B5 00                 NOP
00175 00B6 00                 NOP
00176
00177 00B7 F1         NGTIV   MOV A,@R1               ;MARK NEG
00178 00B8 4302               ORL A,#00000010B
00179 00BA A1                 MOV @R1,A               ;SEE IF < -130
00180 00BB 97                 CLR C
00181 00BC FE                 MOV A,R6
00182 00BD 03A0               ADD A,#LSP13
00183 00BF FF                 MOV A,R7
00184 00C0 1304               ADDC A,#MSP13
00185 00C2 728F    >          JB3 INVLD
00186 00C4 049F    >          JMP GREEN
00187
00188
00189
00190 00C6 2301       CMPLT   MOV A,#01               ;DISABLE Z80
00191 00C8 8D                 ORLD P5,A
00192 00C9 B828               MOV R0,#40
00193 00CB B938               MOV R1,#56              ;EXTEND REGIS 3 UP
00194
00195 00CD F0                 MOV A,@R0               ;READ FIRST STATUS WORD AND
00196                                                 ;SAVE(AT END OF STATUS ZONE)
00197 00CE A1                 MOV @R1,A
00198 00CF 18                 INC R0
00199 00D0 19                 INC R1
00200
00201 00D1 F0                 MOV A,@R0
00202 00D2 A1                 MOV @R1,A
00203 00D3 18                 INC R0
00204 00D4 19                 INC R1
00205
00206 00D5 F0                 MOV A,@R0
00207 00D6 A1                 MOV @R1,A
00208
00209 00D7 B937               MOV R1,#55              ; AND 3 DOWN, READ LAST STATUS WORD
00210                                                 ; AND SAVE(BEFORE STATUS ZONE)
00211 00D9 B827               MOV R0,#39
00212
```

```
00213 00DB F1                MOV A,@R1
00214 00DC A0                MOV @R0,A
00215 00DD C9                DEC R1
00216 00DE C8                DEC R0
00217
00218 00DF F1                MOV A,@R1
00219 00E0 A0                MOV @R0,A
00220 00E1 C9                DEC R1
00221 00E2 C8                DEC R0
00222
00223 00E3 F1                MOV A,@R1
00224 00E4 A0                MOV @R0,A
00225
00226 00E5 BD08              MOV R5,#8
00227 00E7 00                NOP
00228 00E8 00                NOP
00229 00E9 0C                MOVD A,P4           ;GET THE ZERO XING
00230 00EA 530F              ANL A,#0FH          ;4 BITS VALUE SPECIFIES ZERO CROSSING
00231                                            ;ZONE (22.5 DEGREE INCREMENT)
00232 00EC AB                MOV R3,A
00233 00ED 00                NOP
00234 00EE 00                NOP
00235 00EF 00                NOP
00236 00F0 00                NOP
00237 00F1 044D     >        JMP NORTH
00238                   ;
00239                   ;    MEASURMENT SCAN
00240                   ;    ****************
00241
00242 00F3 2308         MESUR MOV A,#08H
00243 00F5 3E                MOVD P6,A
00244 00F6 2304              MOV A,#04H
00245 00F8 8D                ORLD P5,A
00246 00F9 BA00              MOV R2,#0
00247 00FB B928              MOV R1,#40          ;CHECK THE TYPE OF S0
00248 00FD F1                MOV A,@R1
00249 00FE 37                CPL A
00250 00FF 1204     >        JB0 NORMAL          ;IF GREEN SKIP
00251 0101 23FB              MOV A,#11111011B
00252 0103 9D                ANLD P5,A           ;OTHERWISE INVERT P.D.
00253 0104 00           NORMAL NOP
00254 0105 00                NOP
00255 0106 00                NOP
00256 0107 00                NOP
00257 0108 00                NOP
00258 0109 00                NOP
00259
00260 010A 00           DATA NOP                 ;WAIT FOR S0 (1 st STATUS)
00261 010B 360A     >        JT0 DATA
00262 010D 97                CLR C
00263 010E 08                INS A,BUS           ;READ IT AND STORE
00264 010F 0301              ADD A,#01H
00265 0111 AE                MOV R6,A
```

```
00266 0112 0A              IN A,P2
00267 0113 47              SWAP A
00268 0114 1300            ADDC A,#00H
00269 0116 AF              MOV R7,A
00270 0117 19              INC R1
00271 0118 F1              MOV A,@R1              ;CHECK THE PREDICATION OF NEXT
00272                                             ;(IN ORDER TO PREPARE THE PHASE
00273                                             ;  DETECTOR FOR THE NEXT SAMPLE)
00274 0119 00              NOP
00275 011A 00              NOP
00276 011B 00              NOP
00277 011C 00              NOP
00278 011D 1224    >       JB0 IIII               ;  SAMPLE FOR TYPE AND CONTROL P.D.ACCORDINGLY
00279 011F 2304            MOV A,#00000100B
00280 0121 8D              ORLD P5,A
00281 0122 2427    >       JMP SKIP7
00282 0124 23FB      IIII  MOV A,#11111011B
00283 0126 9D              ANLD P5,A
00284
00285 0127 00        SKIP7 NOP
00286 0128 00              NOP
00287 0129 00              NOP
00288 012A 00              NOP
00289 012B 00              NOP
00290 012C 00              NOP
00291
00292 012D C9              DEC R1
00293 012E F1              MOV A,@R1              ;NOW CHECK S(n) FOR TYPE
00294                                             ; WAS IT SHIFTED OR NOT
00295 012F 37              CPL A
00296 0130 125E    >       JB0 OUTPT              ;IF GREEN OUTPUT IT
00297 0132 FA              MOV A,R2               ;IF NOT SUBTRACT n FROM A
00298 0133 37              CPL A                  ; (SAMPLE NUMBER - ZERO CROSSING)
00299 0134 6B              ADD A,R3
00300 0135 37              CPL A
00301
00302 0136 F25A    > RIGHT JB7 LEFT
00303 0138 724D    >       JB3 BLUE               ;IF RESULT POSITIVE, WE ARE ON THE RIGHT OF XING
00304 013A 00              NOP                    ; IF SAMPLE NUMBER >8, THEN IN THE NEGATIVE
00305                                             ;  PORTION OF THE PHASE CURVE.
00306 013B 00              NOP
00307 013C 00              NOP
00308 013D 00              NOP
00309                                             ;IF n - A >8 THIS IS BLUE
00310 013E FE        RED   MOV A,R6
00311 013F 97              CLR C
00312 0140 0367            ADD A,#LSP18           ;ADD 180 DEGREES
00313 0142 AE              MOV R6,A
00314 0143 FF              MOV A,R7
00315 0144 1306            ADDC A,#MSP18
00316 0146 AF              MOV R7,A
00317 0147 245E    >       JMP OUTPT
00318
```

```
00319 0149 00                 NOP
00320 014A 00                 NOP
00321 014B 00                 NOP
00322 014C 00                 NOP
00323
00324 014D 97           BLUE  CLR C                ;IF BLUE SUBTRACE 180 DEG
00325 014E FE                 MOV A,R6
00326 014F 0399               ADD A,#LSM18
00327 0151 AE                 MOV R6,A
00328 0152 FF                 MOV A,R7
00329 0153 1309               ADDC A,#MSM18        ; ADD MINUS 180 DEGREES
00330 0155 AF                 MOV R7,A
00331 0156 245E    >          JMP OUTPT
00332
00333 0158 00                 NOP
00334 0159 00                 NOP
00335 015A 0310         LEFT  ADD A,#16
00336 015C 2436    >          JMP RIGHT
00337
00338 015E FE           OUTPT MOV A,R6             ; OUTPUT Sn TO DFT CARD
00339 015F 00                 NOP
00340 0160 39                 OUTL P1,A
00341 0161 FF                 MOV A,R7
00342 0162 00                 NOP
00343 0163 3F                 MOVD P7,A
00344 0164 00                 NOP
00345 0165 00                 NOP
00346 0166 2307               MOV A,#00000111B;    ;OUTPUT EOC(BAR)=0
00347 0168 9E                 ANLD P6,A
00348
00349 0169 FA                 MOV A,R2
00350 016A 17                 INC A
00351 016B 927A    >          JB4 SKIP8            ;16 SAMPLE DONE
00352 016D AA                 MOV R2,A
00353 016E 0328               ADD A,#40
00354 0170 A9                 MOV R1,A
00355 0171 2308               MOV A,#00001000B     ;RASIE EOC(BAR)
00356 0173 8E                 ORLD P6,A            ;EOC=1
00357 0174 3678    >    STAY  JT0 DATAA            ;IF SO GO FOR NEXT SAMPLE
00358 0176 2474    >          JMP STAY
00359 0178 240A    >    DATAA JMP DATA
00360
00361 017A 23F7         SKIP8 MOV A,#0F7H
00362 017C 9D                 ANLD P5,A
00363 017D 00                 NOP                  ;CLEAR INTERRUPT
00364 017E 00                 NOP
00365 017F 2308               MOV A,#8
00366 0181 8D                 ORLD P5,A
00367 0182 00                 NOP
00368 0183 00                 NOP
00369 0184 23FE               MOV A,#0FEH
00370 0186 9D                 ANLD P5 ,A           ;ENABLE Z80
00371 0187 00                 NOP
```

```
00372 0188 00                 NOP
00373 0189 CD                 DEC R5
00374 018A 2308               MOV A,#00001000B
00375 018C 8E                 ORLD P6,A               ;EOC(BAR)=1
00376 018D 044D               JMP NORTH               ;AND WAIT FOR NORTH
00377
00378      0004       MSP13   EQU 04H
00379      00A0       LSP13   EQU 0A0H
00380
00381      0006       MSP18   EQU 006H
00382      0067       LSP18   EQU 067H
00383
00384      000B       MSM13   EQU 00BH
00385      0060       LSM13   EQU 60H
00386
00387      0009       MSM18   EQU 009H
00388      0099       LSM18   EQU 099H
00389
```

```
Scalars

   LSM13 -- 0060        LSM18 -- 0099        LSP13 -- 00A0        LSP18 -- 0067        MSM13 -- 000B
   MSM18 -- 0009        MSP13 -- 0004        MSP18 -- 0006

%FIRSTD (default) Section (018F)

   BLUE --- 014D        CHECK -- 00A9        CMPLT -- 00C6        DATA --- 010A        DATAA -- 0178
   GREEN -- 009F        IIII --- 0124        INISC -- 0013        INPUT -- 001A        INVLD -- 008F
   LEFT --- 015A        MAIN --- 0065        MESUR -- 00F3        MESUR1 - 0055        NEWDT -- 0069
   NEWIN -- 001E        NGTIV -- 00B7        NORMAL - 0104        NORTH -- 004D        NORTH1 - 0042
   OUTPT -- 015E        PASS --- 0016        RED ---- 013E        RFSCN -- 0059        RIGHT -- 0136
   RSTRT -- 0000        SKIP7 -- 0127        SKIP8 -- 017A        STAY --- 0174


    389 Source Lines     389 Assembled Lines   44202 Bytes available

              >>> No assembly errors detected <<<
```

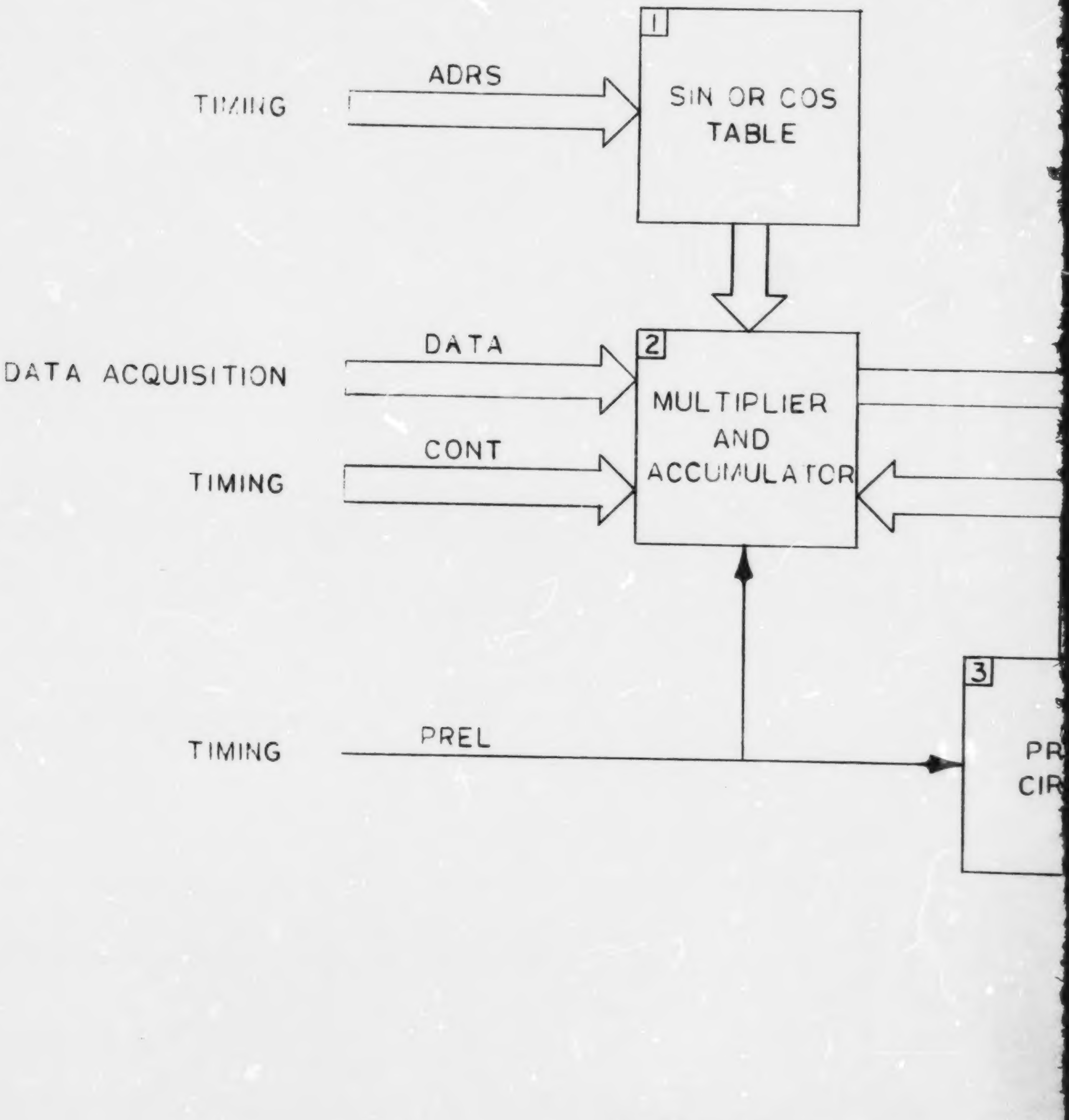
### 2.4.2 DFT PROCESSOR

The DFT processor board is composed of one multiplier/accumulator and two PROMS which contain values for the sin or cosine of angles ranging from 0 to 337.5 degrees in steps of 22.5°.

In the bearing processor, there are two DFT processors, DFT sine and DFT cosine. The electrical operation of the two cards is identical.

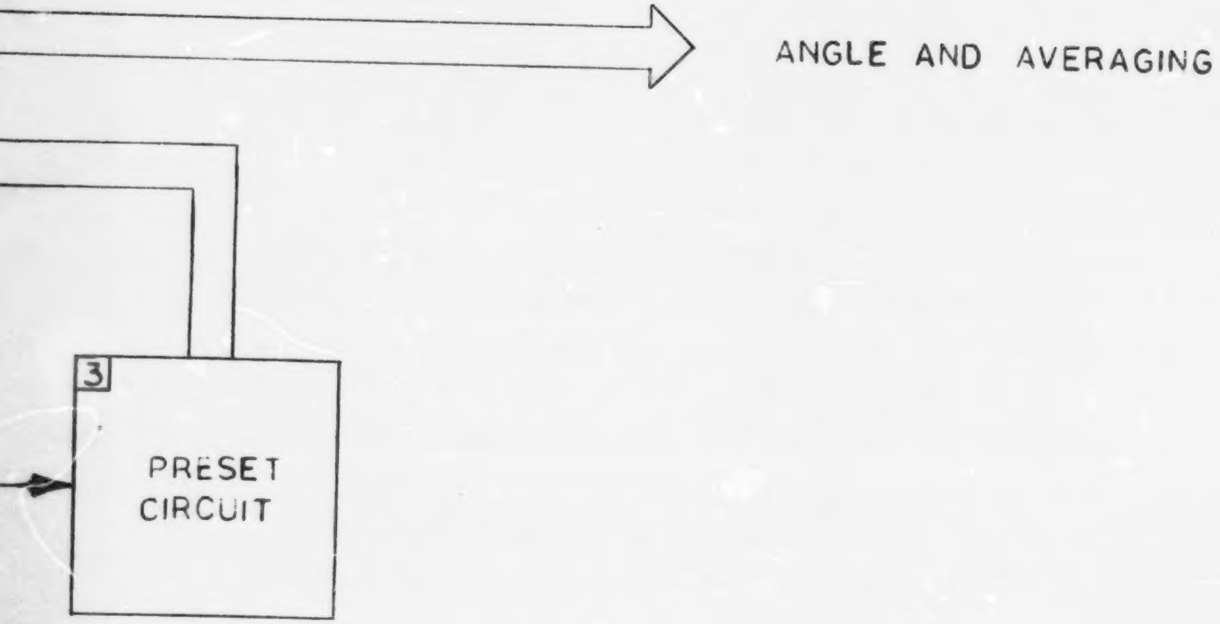
The address lines for the two PROMS originate from the timing board. The multiplier/accumulator is a 12 x 12 bit device. It multiplies the incoming data from the data acquisition board with a sine (or cosine) value from the PROM table. As the sampling continues, each successive digital word from the data acquisition board is multiplied by successive values from the PROMS. The answers are accumulated, and when sixteen samples have been multiplied and accumulated, the final answer is sent to the angle and averaging card.

The timing to the multiplier/accumulator is supplied from the timing board.



1
SIN OR COS TABLE
TIMING
ADRS
2
MULTIPLIER AND ACCUMULATOR
DATA ACQUISITION
DATA
TIMING
CONT
TIMING
PREL
3
PR
CIR

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be
neither used, copied, reproduced or otherwise dealt with
nor its contents communicated to others.


ANGLE AND AVERAGING
3
PRESET CIRCUIT

rent of
is document may be
otherwise dealt with,

| | | | |
|---|---|---|---|
| REV. NO. | REVISION | DATE | APPR. BY |

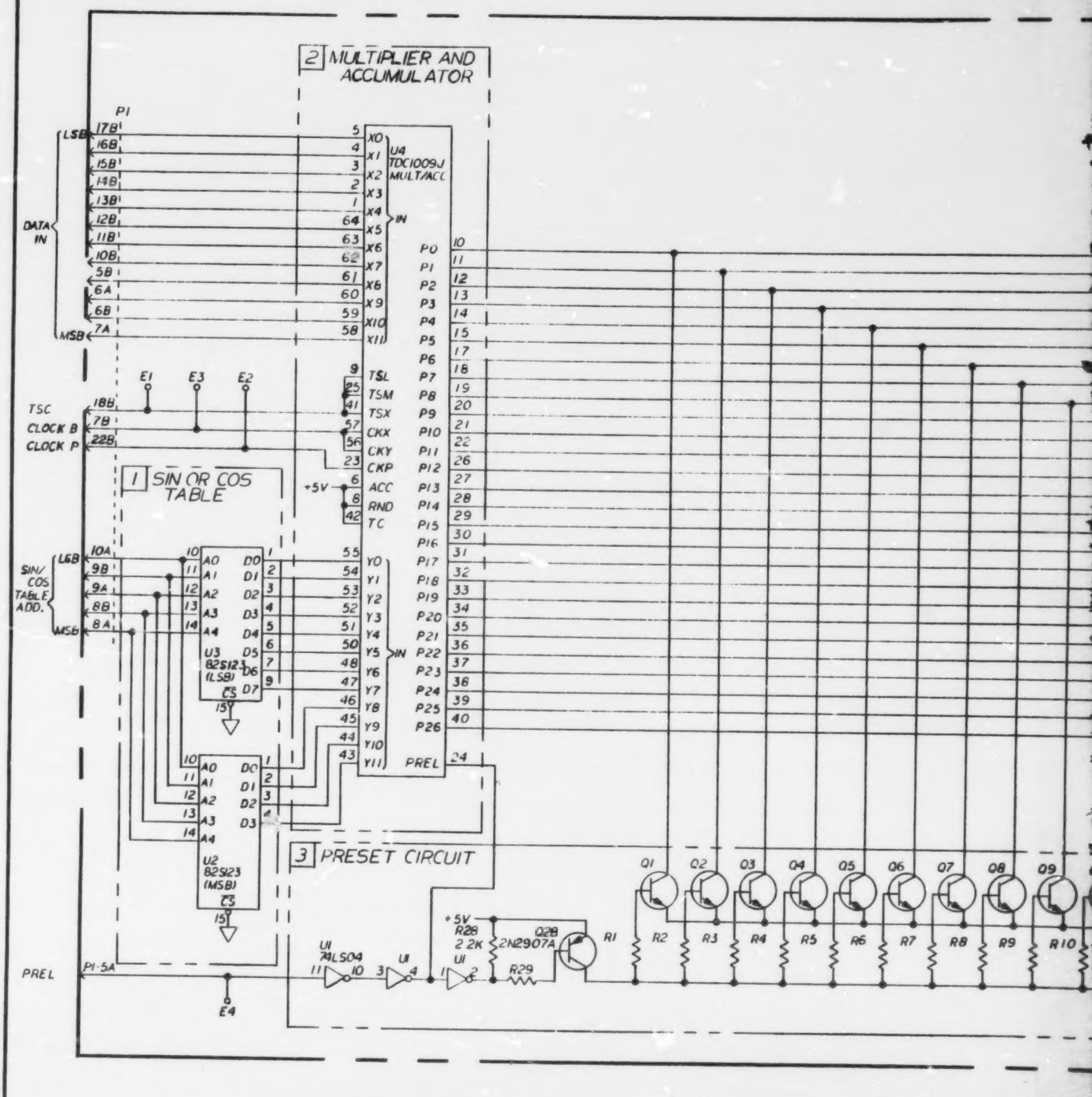
SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

**BAYLY** ENGINEERING LTD a member of AEG

TITLE
BLOCK DIAGRAM
DFT PROCESSOR (SIN OR COS)

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

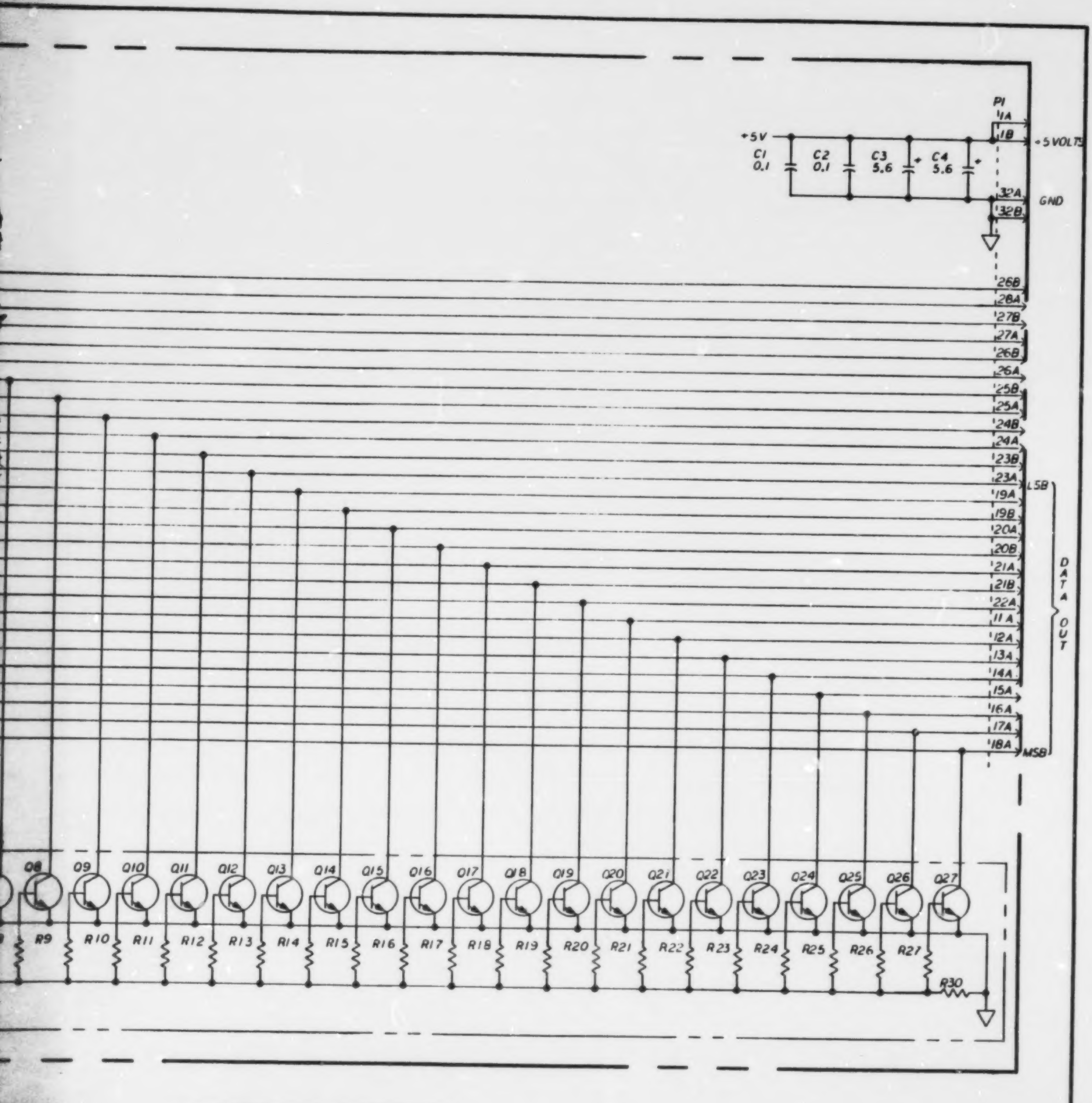
| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| | 83-01-31 | | | 66-0643.027 212.BD-B |



2 MULTIPLIER AND ACCUMULATOR
U4 TDC1009J MULT/ACC
1 SIN OR COS TABLE
3 PRESET CIRCUIT
P1
LSB
MSB
DATA IN
TSC
CLOCK B
CLOCK P
SIN/COS TABLE ADD.
PREL
P1-5A
E1
E2
E3
E4
U3 82S123 (LSB)
U2 82S123 (MSB)
U1 74LS04
+5V
R28 2.2K
Q28 2N2907A
R29
R1
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
R2
R3
R4
R5
R6
R7
R8
R9
R10
X0
X1
X2
X3
X4
X5
X6
X7
X8
X9
X10
X11
IN
TSL
TSM
TSX
CKX
CKY
CKP
ACC
RND
TC
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
P25
P26
PREL
A0
A1
A2
A3
A4
D0
D1
D2
D3
D4
D5
D6
D7
CS

NOTES: UNLESS OTHERWISE SPECIFIED
1- ALL RESISTOR VALUES ARE IN OHMS
2- ALL CAPACITOR VALUES ARE IN MICROFARADS
3- TRANSISTOR Q1 TO Q27 ARE 2N2222A
4- RESISTOR R1 TO R27, R29, R30 ARE 10K OHMS

| HIGHEST DESIGNATION USED | | | | | |
|---|---|---|---|---|---|
| C4 | E4 | P1 | Q28 | R30 | U4 |
| DESIGNATON NOT USED | | | | | |
| | | | | | |


P1
1A
1B
+5 VOLTS
+5V
C1 0.1
C2 0.1
C3 5.6
C4 5.6
32A
32B
GND
28B
28A
27B
27A
26B
26A
25B
25A
24B
24A
23B
23A
19A
19B
20A
20B
21A
21B
22A
11A
12A
13A
14A
15A
16A
17A
18A
LSB
MSB
DATA OUT
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R30

| | U4 |
|---|---|
| | |

| IC'S SUPPLY DISTRIBUTION | | |
|---|---|---|
| DESIGNATION | GND | +5V |
| U1 | 7 | 14 |
| U2, U3 | 8 | 16 |
| U4 | 7,16 | 49 |

BAYLY

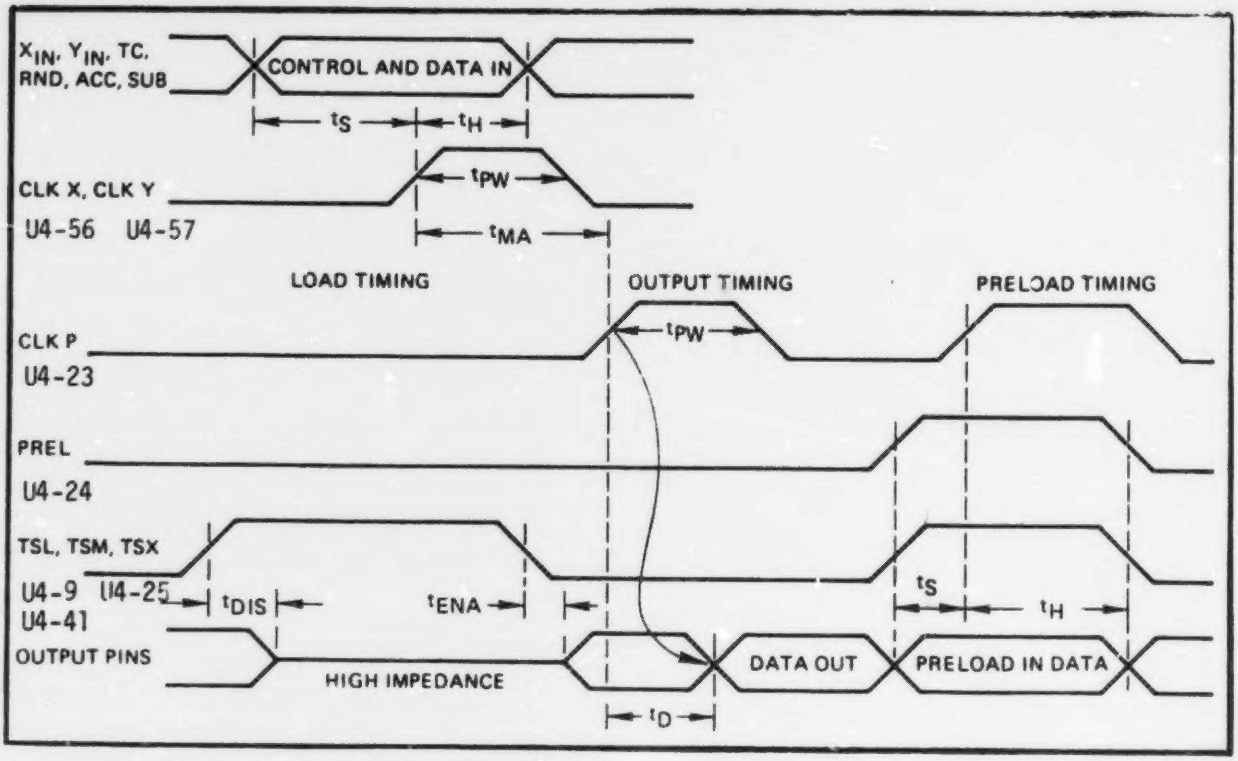
SCHEMATIC DIAGRAM
DFT PROCESSOR (SIN OR COS)

S. B. 83-2-11

56-0643.027 212.CD-D

## 2.4.2.3 TEST

Check that timings between signals correspond to the diagram below.



XIN, YIN, TC, RND, ACC, SUB
CONTROL AND DATA IN
tS
tH
CLK X, CLK Y
U4-56 U4-57
tPW
tMA
LOAD TIMING
OUTPUT TIMING
PRELOAD TIMING
CLK P
U4-23
tPW
PREL
U4-24
TSL, TSM, TSX
U4-9 U4-25
U4-41
tDIS
tENA
tS
tH
OUTPUT PINS
HIGH IMPEDANCE
DATA OUT
PRELOAD IN DATA
tD

## 2.4.2.4 SPECIFICATIONS

### SINE TABLE

| ADDRESS | MSB PROM (U2) | LSB PROM (U3) |
|---|---|---|
| 0 | 00 | 00 |
| 1 | 03 | 10 |
| 2 | 05 | A8 |
| 3 | 07 | 64 |
| 4 | 07 | FF |
| 5 | 07 | 64 |
| 6 | 05 | A8 |
| 7 | 03 | 10 |
| 8 | 00 | 00 |
| 9 | 0C | F0 |
| A | 0A | 58 |
| B | 08 | 9C |
| C | 08 | 00 |
| D | 08 | 9C |
| E | 0A | 58 |
| F | 0C | F0 |

### COSINE TABLE

| ADDRESS | MSB PROM (U2) | LSB PROM (U3) |
|---|---|---|
| 0 | 07 | FF |
| 1 | 07 | 64 |
| 2 | 05 | A8 |
| 3 | 03 | 10 |
| 4 | 00 | 00 |
| 5 | 0C | F0 |
| 6 | 0A | 58 |
| 7 | 08 | 9C |
| 8 | 08 | 00 |
| 9 | 08 | 9C |
| A | 0A | 58 |
| B | 0C | F0 |
| C | 00 | 00 |
| D | 03 | 10 |
| E | 05 | A8 |
| F | 07 | 64 |

## 2.4.3 ANGLE AND AVERAGE

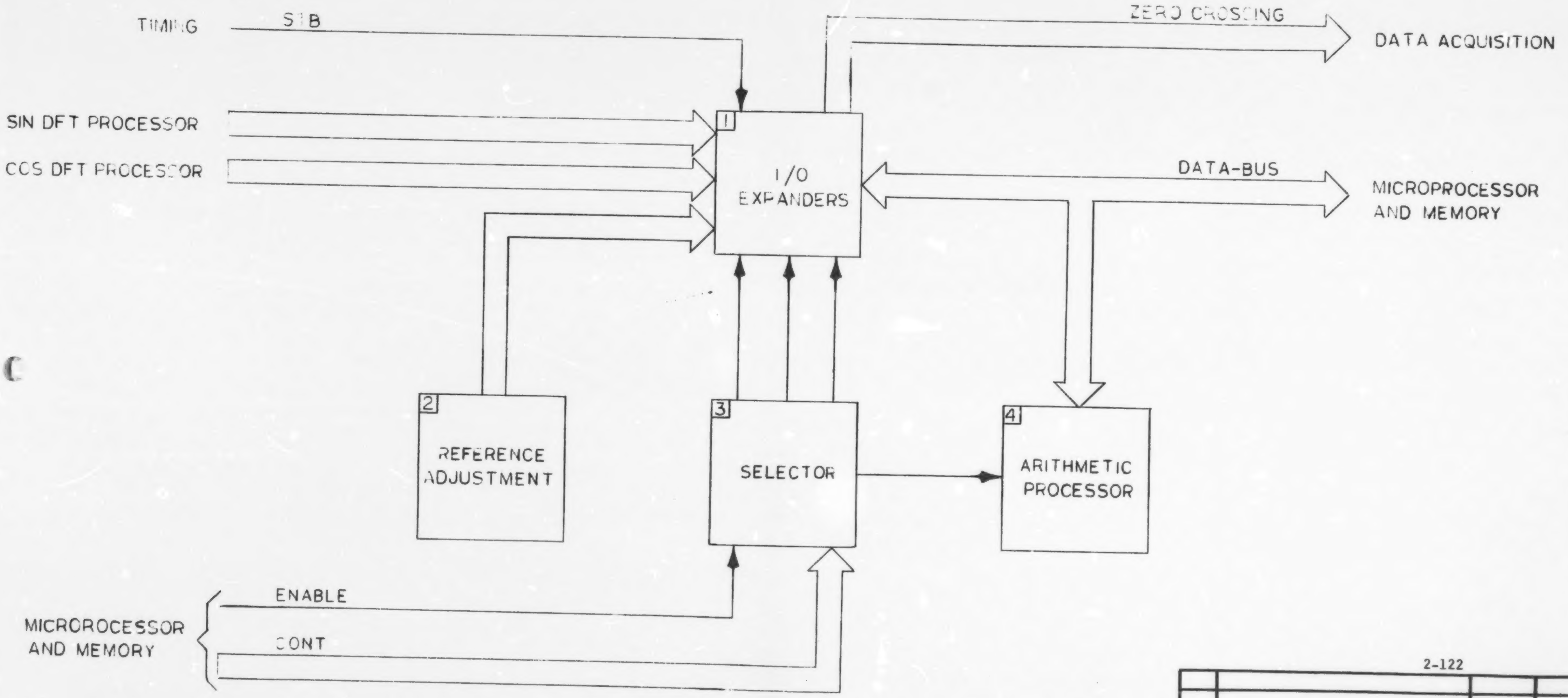
The purpose of the angle and average card is to act as an interface between the DFT processor cards and the microprocessor card.

It is composed of three programmable peripheral interface (PPI) which can be used to read data and output data depending on the state of the control lines.

One PPI is used to read the answer from the DFT sine card. A strobe (STB) signal coming from the timing card identifies the time when the data on the input lines can be read. This produces pulse which interrupts the microprocessor so that it can read the new data. Another PPI is used to read the answer from the DFT cosine card.

The last PPI is used to read the frequency code from synthesizer to select one of the five correction tables in order to correct the site errors and reflection errors.

Finally, provision is made for the implementation of an Arithmetic Processor (APU). Presently the APU is not installed.


TIMING
STB
ZERO CROSSING
DATA ACQUISITION
SIN DFT PROCESSOR
COS DFT PROCESSOR
1
I/O EXPANDERS
DATA-BUS
MICROPROCESSOR AND MEMORY
2
REFERENCE ADJUSTMENT
3
SELECTOR
4
ARITHMETIC PROCESSOR
ENABLE
CONT
MICROROCESSOR AND MEMORY

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH

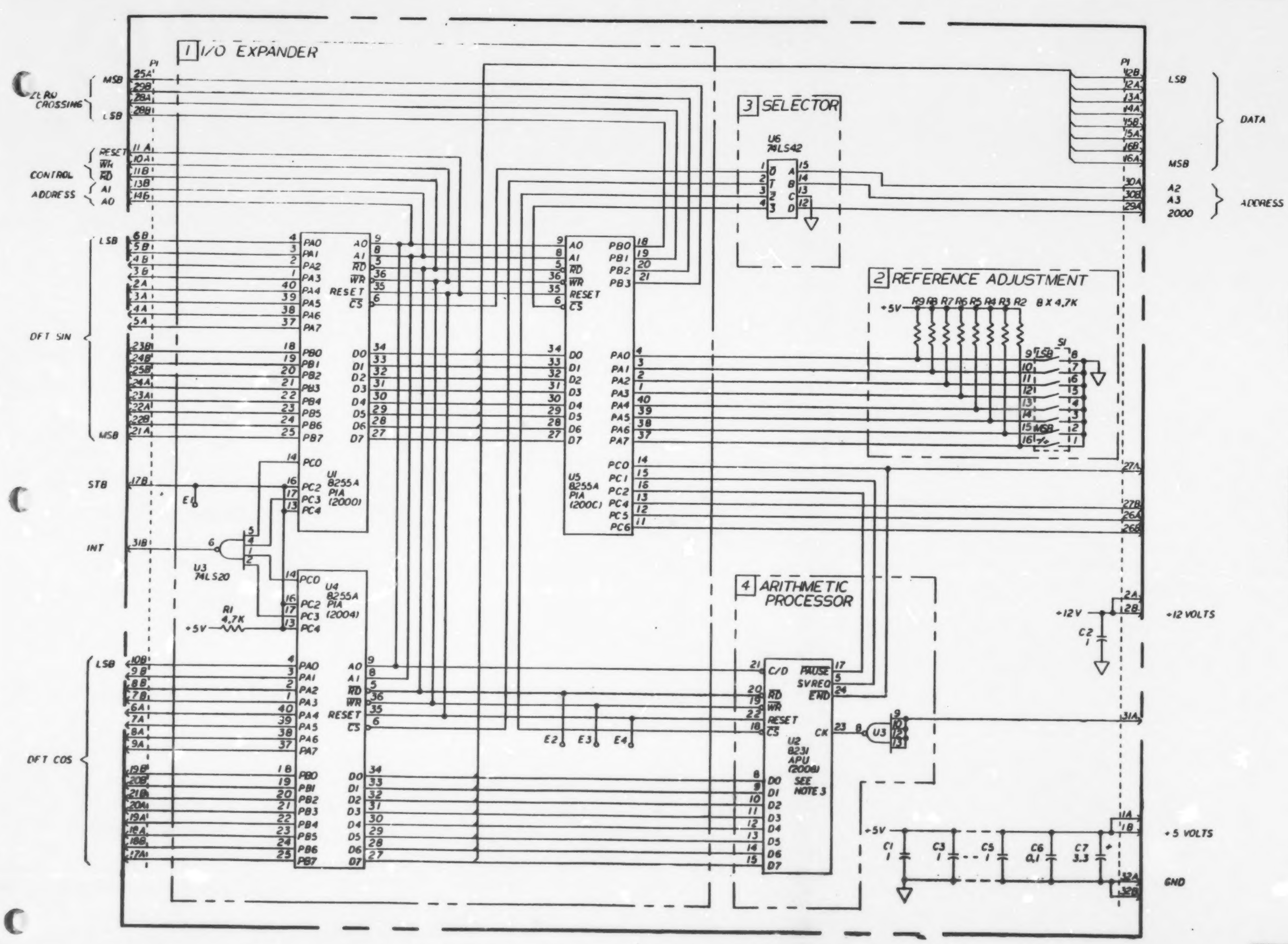
Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

UNLESS OTHERWISE SPECIFIED
TOLERANCES DECIMALS ± ANGLES ± °

BAYLY ENGINEERING LTD a member of

TITLE
BLOCK DIAGRAM
ANGLE AND AVERAGING

DRAWN BY L.T.
DATE 83-02-01
CHECKED BY AA
APPROVED BY
DRAWING NO. 66-0643.027 780.BD-B


1 I/O EXPANDER
2 REFERENCE ADJUSTMENT
3 SELECTOR
4 ARITHMETIC PROCESSOR
P1
ZERO CROSSING
MSB
LSB
CONTROL
RESET
WR
RD
ADDRESS
A1
A0
DFT SIN
DFT COS
STB
INT
E1
E2
E3
E4
U1 8255A PIA (2000)
U4 8255A PIA (2004)
U5 8255A PIA (200C)
U6 74LS42
U3 74LS20
U2 8231 APU (2008) SEE NOTE 3
R1 4.7K
+5V
R9 R8 R7 R6 R5 R4 R3 R2 8 X 4.7K
S1
C/D
PAUSE
SVREQ
END
CK
C1 1
C2 1
C3 1
C5 1
C6 0.1
C7 3.3
+12V
DATA
A2
A3
2000
+12 VOLTS
+5 VOLTS
GND

| HIGHEST DESIGNATION USED | | | | | |
|---|---|---|---|---|---|
| C7 | E4 | P1 | R9 | S1 | U6 |
| DESIGNATION NOT USED | | | | | |
| | | | | | |

NOTES:
1 - ALL RESISTOR VALUES ARE IN OHMS
2 - ALL CAPACITOR VALUES ARE IN MICROFARADS
3 - IC NOT INSTALLED

| IC'S SUPPLY DISTRIBUTION | | | |
|---|---|---|---|
| DESIGNATION | GND | +5V | +12V |
| U1,U4,U5 | 7 | 26 | |
| U2 | 1 | 2 | 16 |
| U3 | 7 | 14 | |
| U6 | 8 | 16 | |

BAYLY

SCHEMATIC DIAGRAM
ANGLE AND AVERAGING

S. B.
33-2-10
36-0843/087 780.CO-D

## 2.4.4 MICROPROCESSOR AND MEMORY

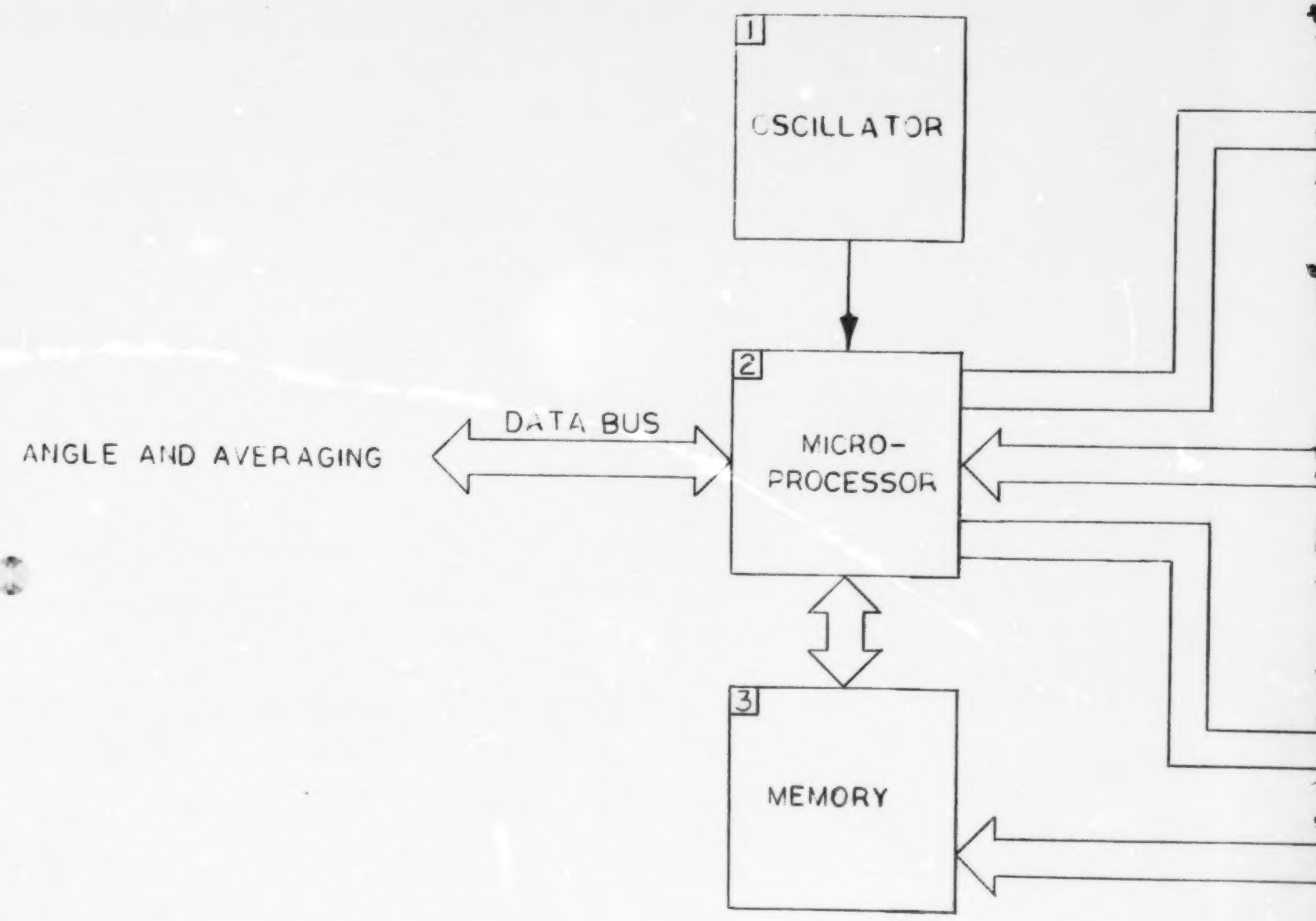
The heart of this board is the microprocessor (Z80). Other modules connected to it are a clock (oscillator), 4 K of EPROM (the program), 1 K of RAM and a programmable peripheral interface port of 24 input-output (I/O) lines.

Address decoding is done on the board to select either the RAM, the EPROM, the I/O or generate enable signal for external uses.

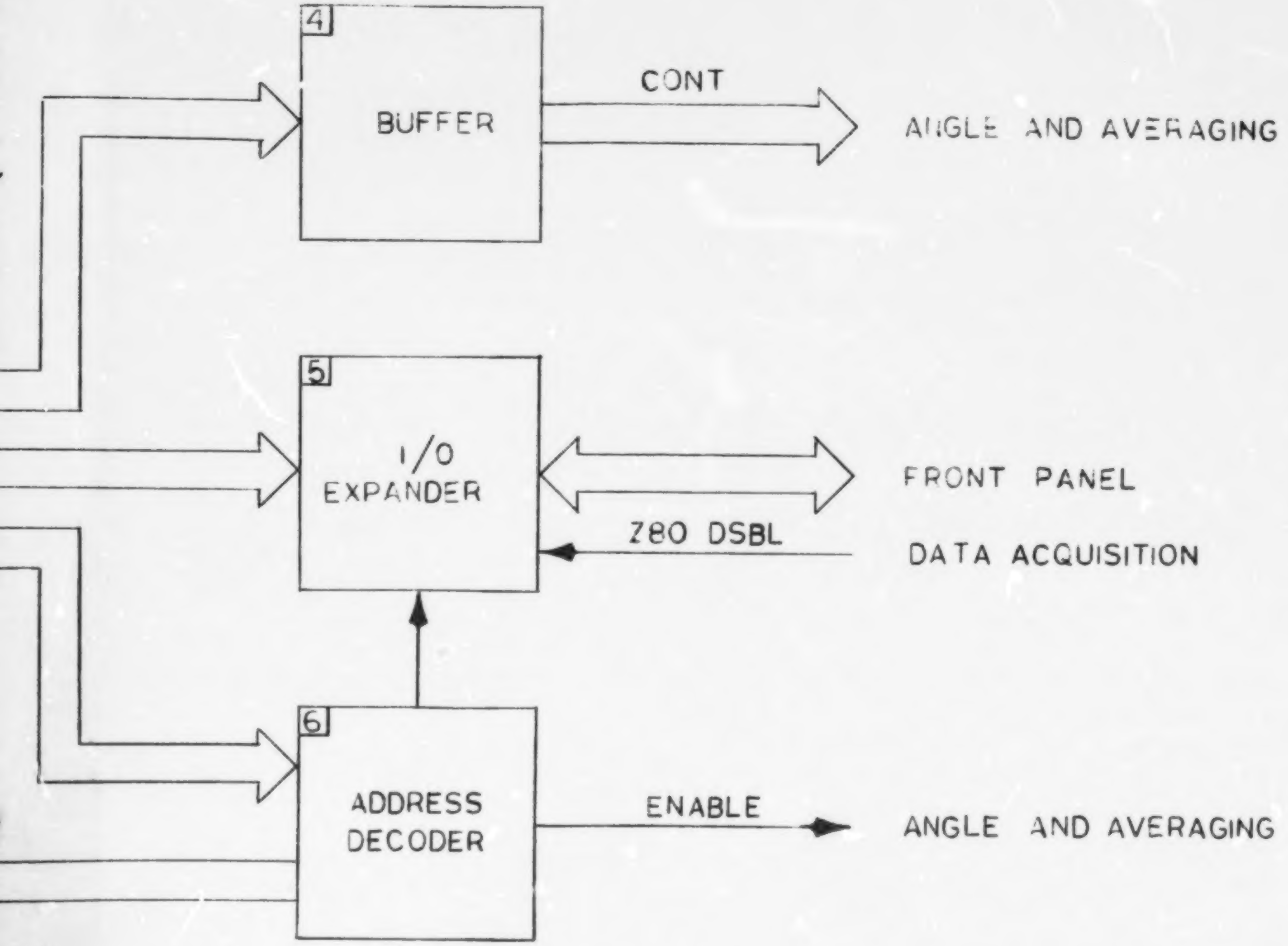
The output supplied by the programmable peripheral interface are:
- display (4 digits of 4 bits each)
- data ready (1 bit)
- data valid (1 bit)
- OHP (Over head pass) (1 bit)

Four other lines are used as input:
- Z80 disable
- QDR/QDM (airplane heading or airport reading)
- Integration constant (2 bits)

On the board there are also buffers for the control lines and part of the address lines, plus a reset circuit.


1
OSCILLATOR
2
MICRO-
PROCESSOR
DATA BUS
ANGLE AND AVERAGING
3
MEMORY

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be
neither used, copied, reproduced or otherwise dealt with,
nor its contents communicated to others.


4
BUFFER
CONT
ANGLE AND AVERAGING
5
I/O
EXPANDER
FRONT PANEL
Z80 DSBL
DATA ACQUISITION
6
ADDRESS
DECODER
ENABLE
ANGLE AND AVERAGING

| REV NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |

SCALE
REMOVE BURR MAX .010R
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED
TOLERANCES DECIMALS ± ANGLES ± °
DRAWN BY E.T.
DATE 83-02-01
CHECKED BY
APPROVED BY

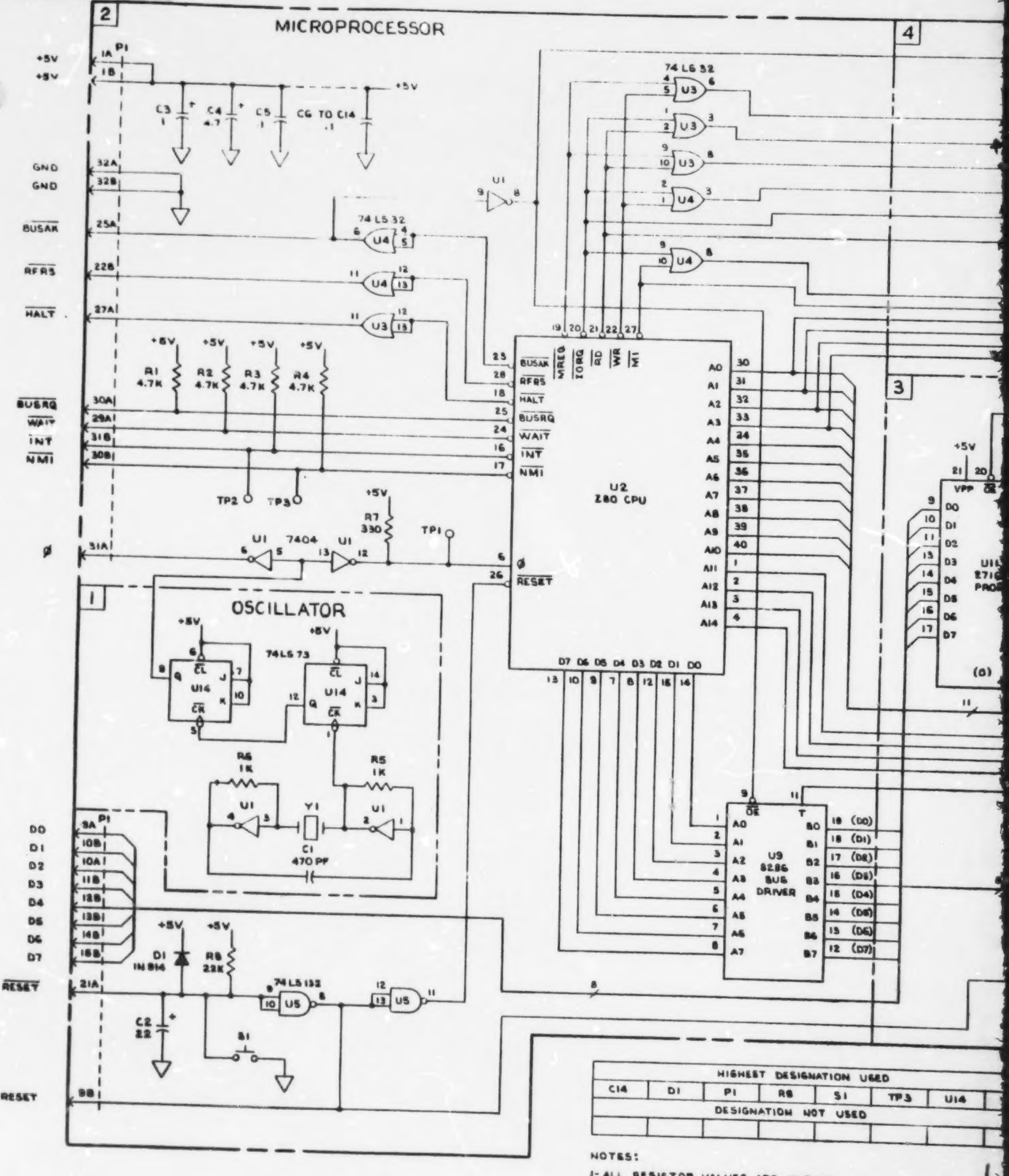
**BAYLY** ENGINEERING LTD
a member of

TITLE
BLOCK DIAGRAM
MICROPROCESSOR AND MEMORY

DRAWING NO.
66-0643.027 282.BD-B

of
document may be
otherwise dealt with,

Without prior written consent of
BAYLY ENGINEERING LIMITED, [illegible]

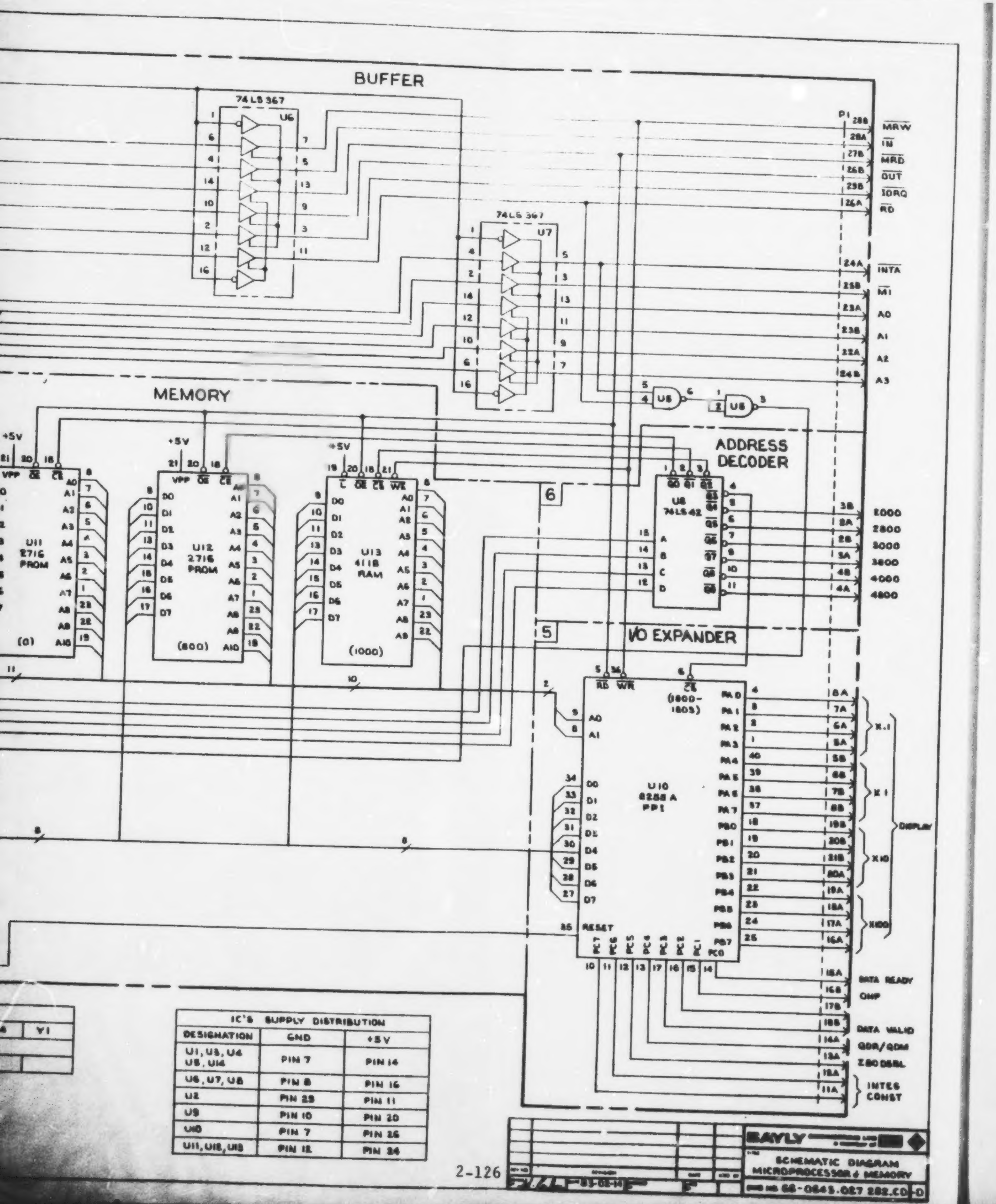

2
MICROPROCESSOR
4
3
1
OSCILLATOR
+5V
+5V
P1
1A
1B
C3 1
C4 4.7
C5 .1
C6 TO C14 .1
GND
GND
32A
32B
BUSAK
25A
RFRS
22B
HALT
27A
74 LS 32
U4
U3
U1
7404
R1 4.7K
R2 4.7K
R3 4.7K
R4 4.7K
BUSRQ
30A
WAIT
29A
INT
31B
NMI
30B
TP1
TP2
TP3
R7 330
ø
31A
U2
Z80 CPU
MREQ
IORQ
RD
WR
M1
RESET
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
D7 D6 D5 D4 D3 D2 D1 D0
74LS73
U14
CL
CK
Q
J
K
R6 1K
R5 1K
Y1
C1 470 PF
D0
D1
D2
D3
D4
D5
D6
D7
3A
10B
10A
11B
12B
13B
14B
15B
D1 IN914
R8 22K
C2 22
74 LS 132
U5
S1
RESET
21A
RESET
9B
U9
8286
BUS DRIVER
OE
T
B0
B1
B2
B3
B4
B5
B6
B7
(D0)
(D1)
(D2)
(D3)
(D4)
(D5)
(D6)
(D7)
VPP
OE
U11
2716
PROM
(0)

| HIGHEST DESIGNATION USED | | | | | | | |
|---|---|---|---|---|---|---|---|
| C14 | D1 | P1 | R8 | S1 | TP3 | U14 | |
| DESIGNATION NOT USED | | | | | | | |
| | | | | | | | |

NOTES:

1- ALL RESISTOR VALUES ARE IN OHMS.

2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.


BUFFER
74LS367
U6
74LS367
U7
MEMORY
+5V
VPP
OE
CE
U11
2716
PROM
(0)
U12
2716
PROM
(800)
U13
4118
RAM
(1000)
ADDRESS
DECODER
U8
74LS42
6
5
I/O EXPANDER
RD
WR
CS
(1800-
1803)
U10
8255 A
PPI
RESET
P1
MRW
IN
MRD
OUT
IORQ
RD
INTA
M1
A0
A1
A2
A3
2000
2800
3000
3800
4000
4800
X.1
X1
X10
X100
DISPLAY
DATA READY
OMP
DATA VALID
QDR/QDM
Z80 DSBL
INTEG
CONST

| IC'S SUPPLY DISTRIBUTION | | |
|---|---|---|
| DESIGNATION | GND | +5V |
| U1, U3, U4<br>U5, U14 | PIN 7 | PIN 14 |
| U6, U7, U8 | PIN 8 | PIN 16 |
| U2 | PIN 23 | PIN 11 |
| U9 | PIN 10 | PIN 20 |
| U10 | PIN 7 | PIN 26 |
| U11, U12, U13 | PIN 12 | PIN 24 |

BAYLY

SCHEMATIC DIAGRAM
MICROPROCESSOR & MEMORY

83-03-14

66-0643.027 282.CD D

## 2.4.4.3 SOFTWARE

The program is divided in two major sections : the main program and the interrupt routine. The main program wait for the signal "cycle complete" which is set in the interrupt routine.

The interrupt is activated by the strobe (STB) line coming from the timing board. This line is synchronized with the end of a complete scan (all 16 dipoles where sampled). At this moment, the sum of sine $\left(\sum_{i=0}^{15} X_i \text{ sine } \Theta_i\right)$ and the sum of cosine $\left(\sum_{i=0}^{15} X_i \cos \Theta_i\right)$ is available at the output of each of the two multipliers/accumulator (on the DFT cards).

With these values, the bearing is computed by doing the arctangent of the sum of sine divided by the sum of cosine.

$$\text{Bearing} = \text{arctg}\left(\sum_{i=0}^{15} X_i \text{ sine } \Theta_i \Big/ \sum_{i=0}^{15} X_i \cos \Theta_i\right)$$

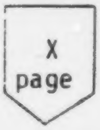
This bearing is then compared with the average value of the last eight reading. If the new value is close to the average value then it is considered as a good bearing. If not, this new bearing is rejected.

The amplitude of the sum of sine and sum of cosine is verified, and if below a certain threshold the OHP signal is turned on.

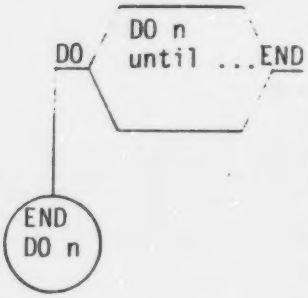
Eight bearings are averaged before asserting the cycle complete signal. This signal will allow the main program to be executed.

The first thing that the main program does is to check how many averaged value must be added and again averaged. The integration constant, which is set by a knob on the front panel of this D.F. set, dictates if 1, 2, 4 or 8 values are needed. This final averaged value is converted to a BCD (Binary Coded Decimal) number and sent to the display.

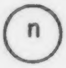
## FLOWCHART SYMBOLS



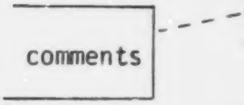
Off-page connector. The letter inside the symbol is used to differentiate between different connection. A letter is related to one specific input point. Page number is also included to ease the search.



Loop This symbol represents a loop, which is identified by number "n". The sequence of instruction which is done repetitevely in the loop is described starting on the side of the symbol marked "DO". The end of the sequence is identified by the termination circle. The number "n" inside the circle relates to the corresponding loop number. This sequence will be repeated as long as the condition specified after the word "until" is not met. When the condition is fulfilled, then the symbol output marked "END" is used.

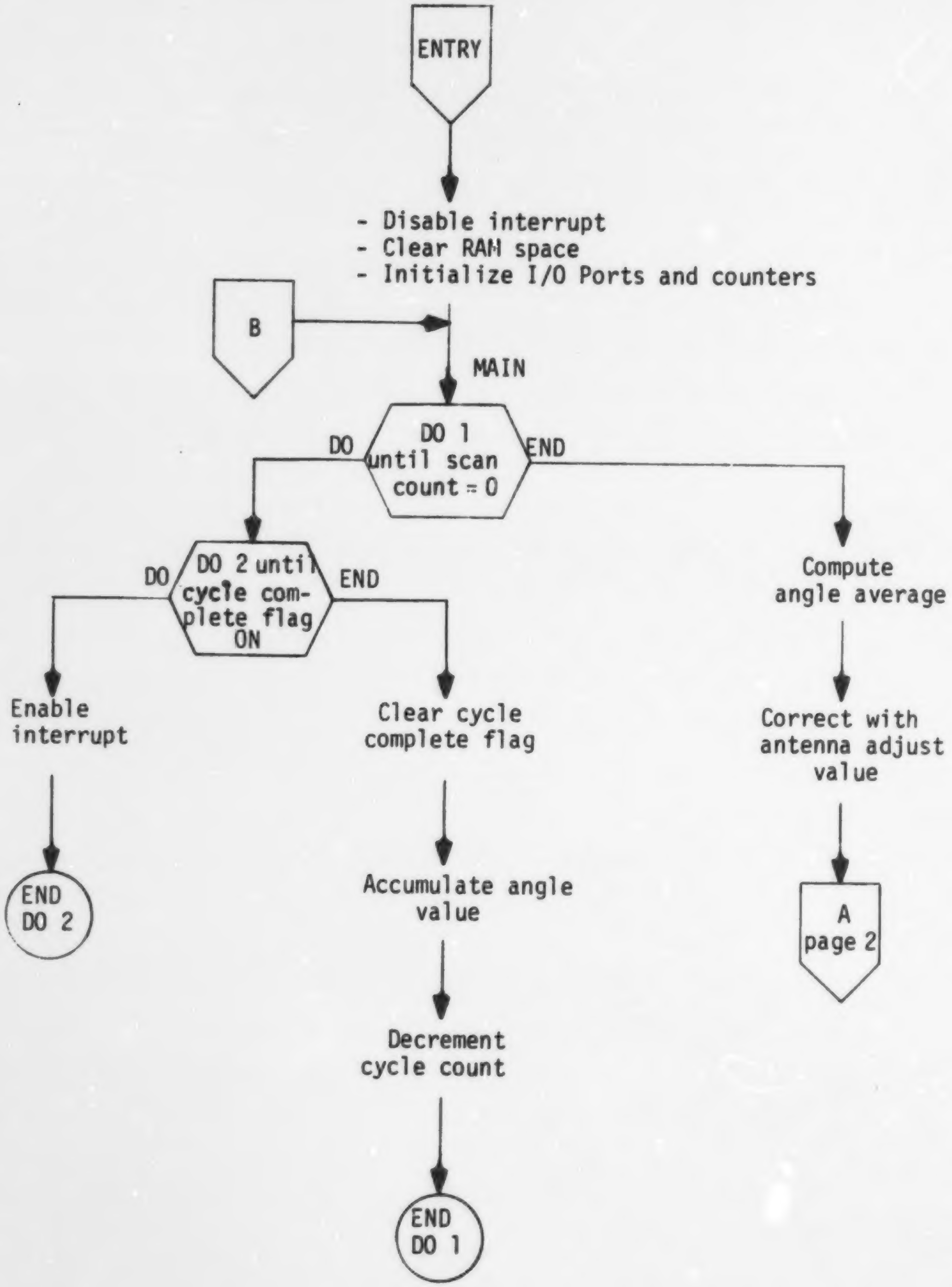


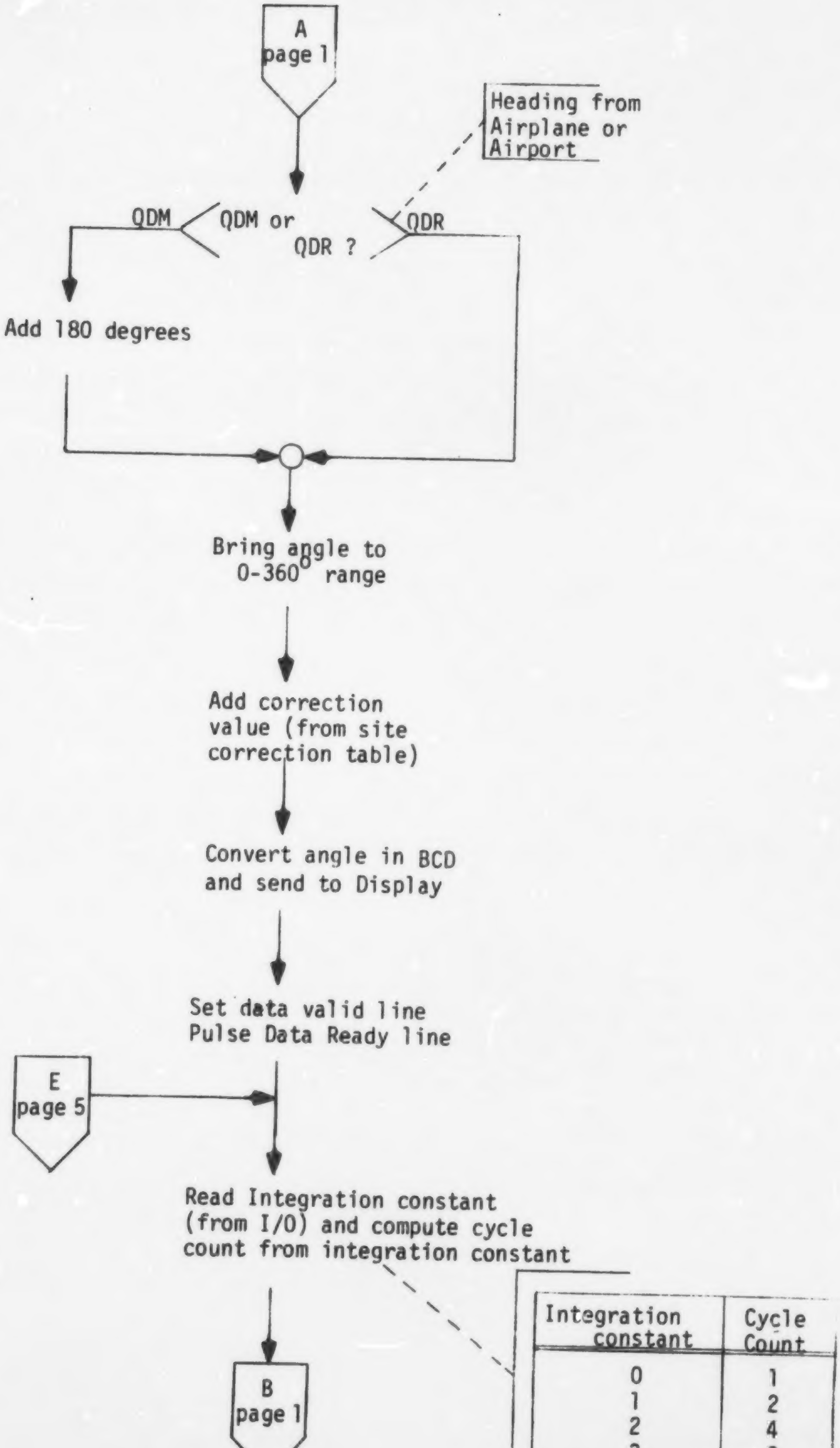
On-page connector. An arrow pointing to or from the bubble identifies the flow path. Connection is always done on the same page.



Dashed line without an arrowhead is used to provide comments.

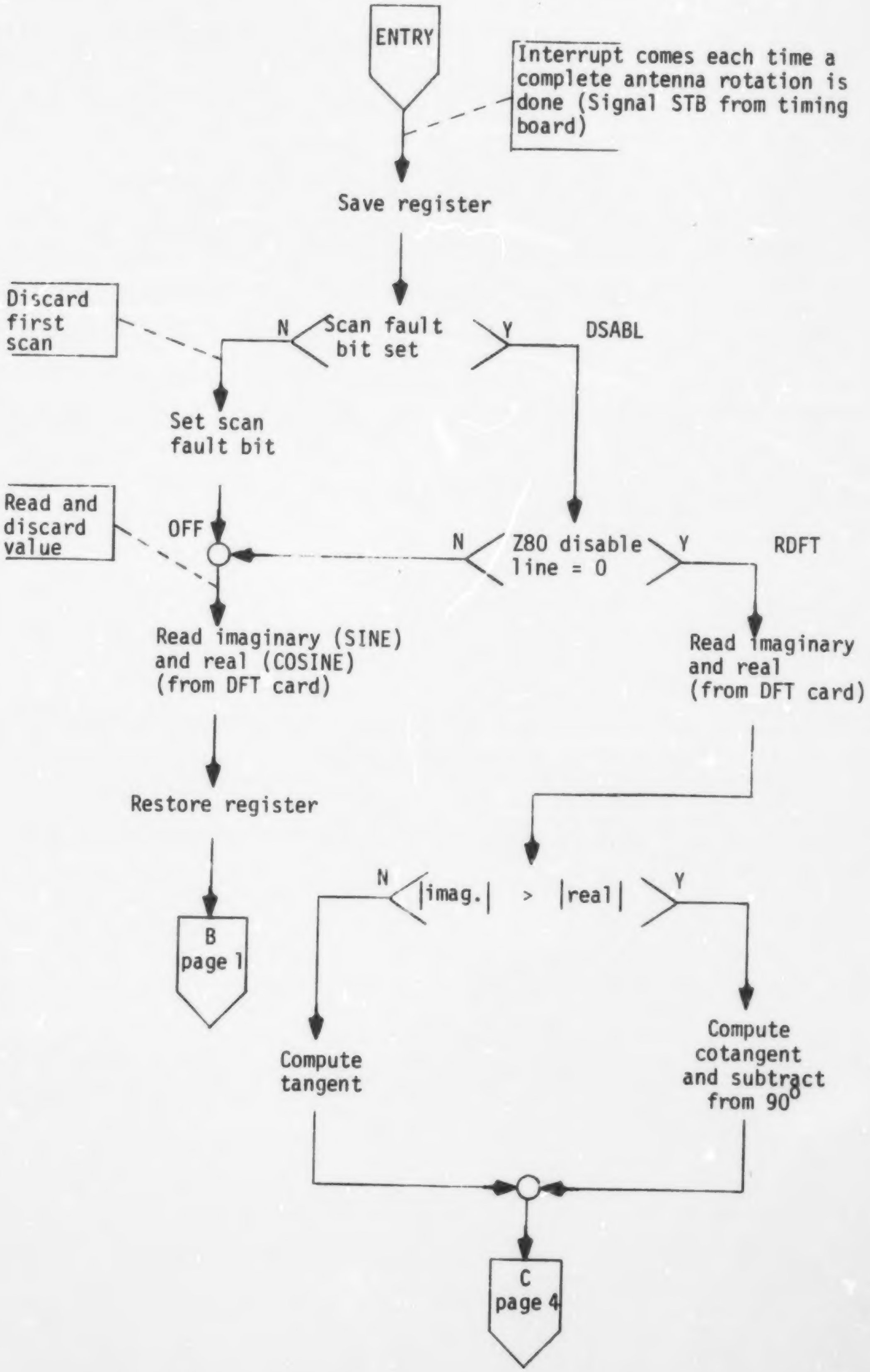
## MICROPROCESSOR AND MEMORY : FLOWCHART

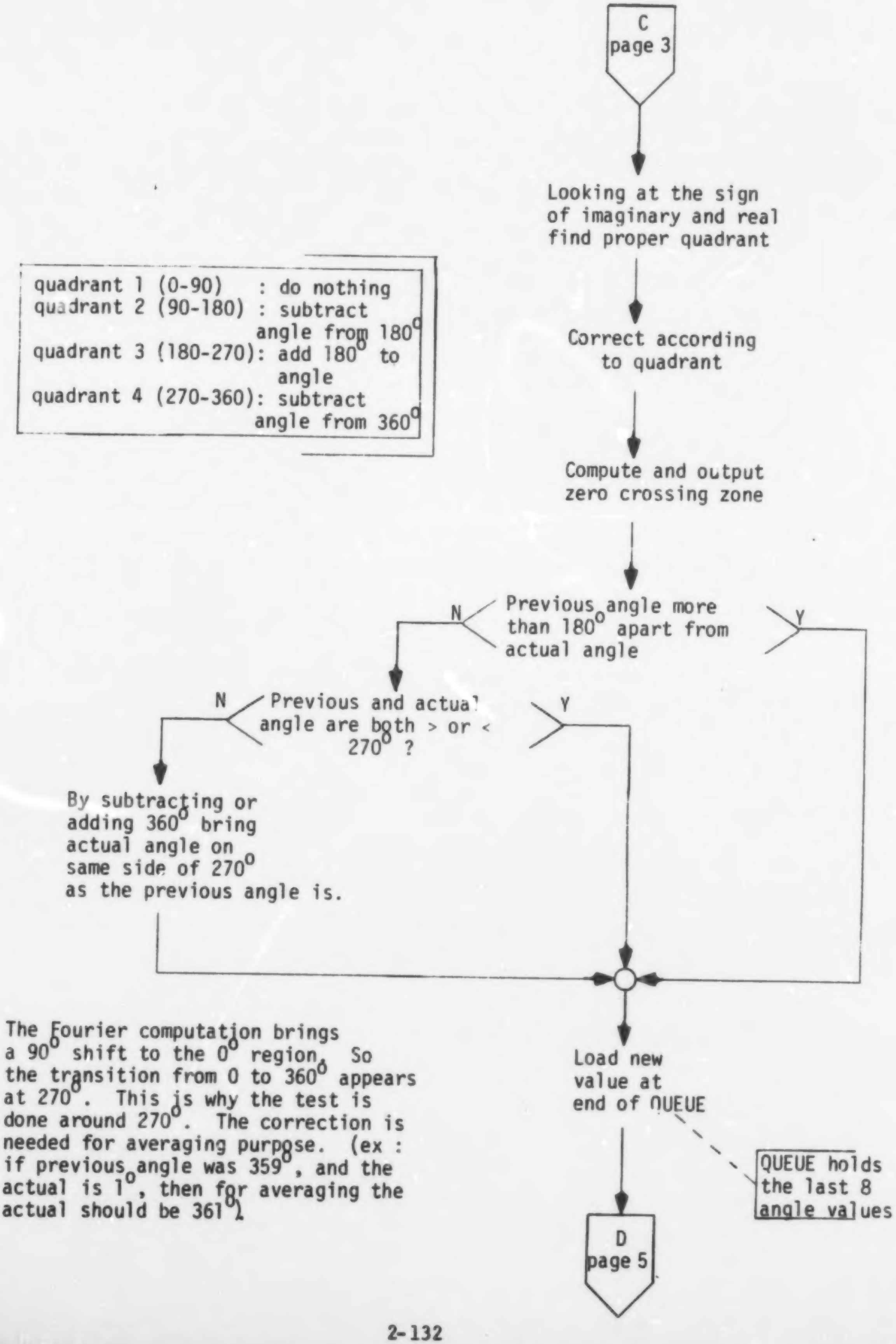

ENTRY
- Disable interrupt
- Clear RAM space
- Initialize I/O Ports and counters
B
MAIN
DO 1 until scan count = 0
DO
END
DO 2 until cycle complete flag ON
DO
END
Compute angle average
Enable interrupt
Clear cycle complete flag
Correct with antenna adjust value
END DO 2
Accumulate angle value
A page 2
Decrement cycle count
END DO 1


A
page 1
Heading from
Airplane or
Airport
QDM
QDM or
QDR ?
QDR
Add 180 degrees
Bring angle to
0-360° range
Add correction
value (from site
correction table)
Convert angle in BCD
and send to Display
Set data valid line
Pulse Data Ready line
E
page 5
Read Integration constant
(from I/O) and compute cycle
count from integration constant
B
page 1

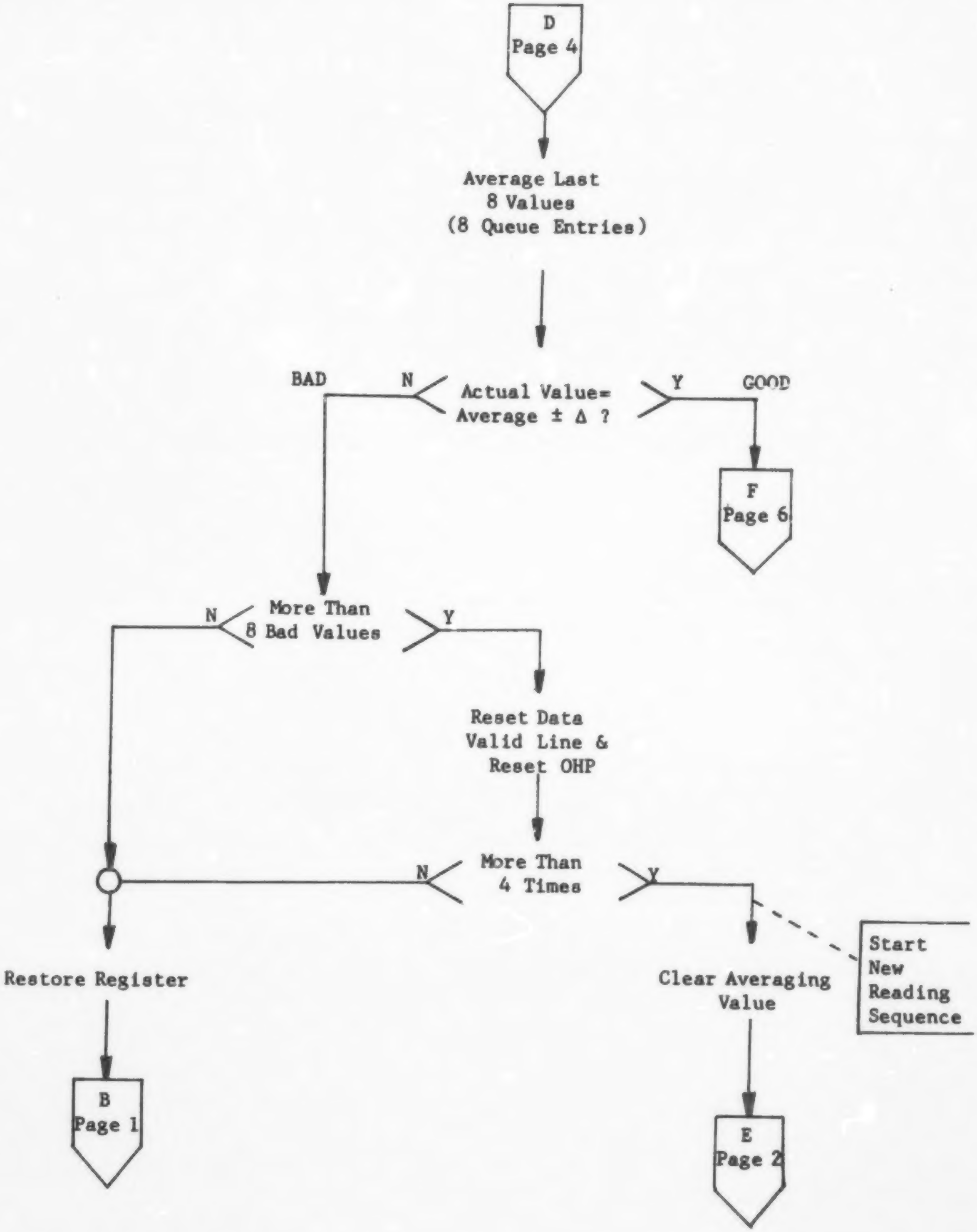
| Integration constant | Cycle Count |
|---|---|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |

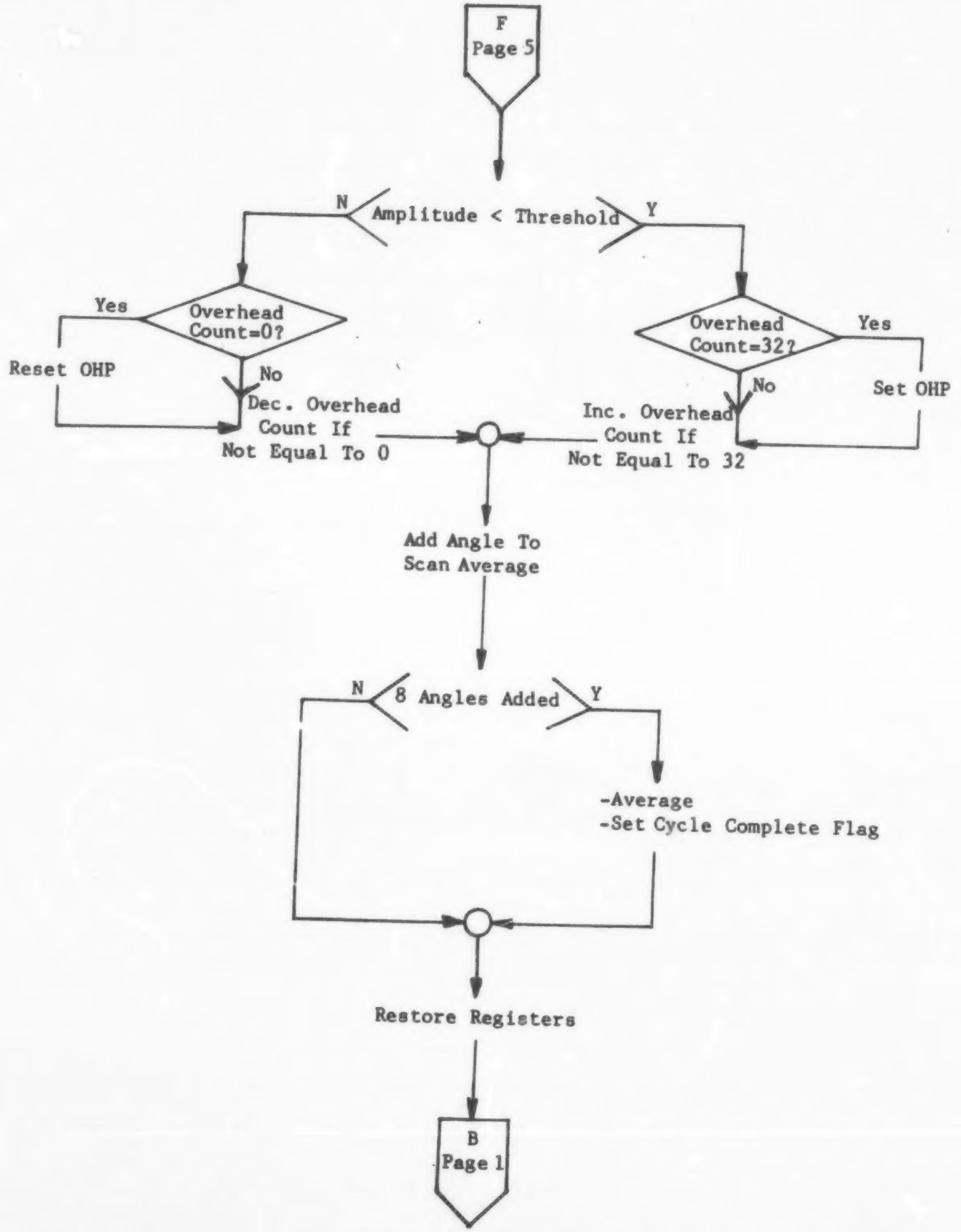
# INTERRUPT ROUTINE


ENTRY
Interrupt comes each time a complete antenna rotation is done (Signal STB from timing board)
Save register
Discard first scan
N
Scan fault bit set
Y
DSABL
Set scan fault bit
Read and discard value
OFF
N
Z80 disable line = 0
Y
RDFT
Read imaginary (SINE) and real (COSINE) (from DFT card)
Read imaginary and real (from DFT card)
Restore register
B page 1
N
|imag.| > |real|
Y
Compute tangent
Compute cotangent and subtract from 90°
C page 4


C
page 3
Looking at the sign of imaginary and real find proper quadrant
quadrant 1 (0-90) : do nothing
quadrant 2 (90-180) : subtract angle from 180°
quadrant 3 (180-270): add 180° to angle
quadrant 4 (270-360): subtract angle from 360°
Correct according to quadrant
Compute and output zero crossing zone
Previous angle more than 180° apart from actual angle
N
Y
Previous and actual angle are both > or < 270° ?
N
Y
By subtracting or adding 360° bring actual angle on same side of 270° as the previous angle is.
Load new value at end of QUEUE
QUEUE holds the last 8 angle values
D
page 5

Note : The Fourier computation brings a 90° shift to the 0° region. So the transition from 0 to 360° appears at 270°. This is why the test is done around 270°. The correction is needed for averaging purpose. (ex : if previous angle was 359°, and the actual is 1°, then for averaging the actual should be 361°)


D
Page 4
Average Last
8 Values
(8 Queue Entries)
BAD
N
Actual Value=
Average ± Δ ?
Y
GOOD
F
Page 6
N
More Than
8 Bad Values
Y
Reset Data
Valid Line &
Reset OHP
N
More Than
4 Times
Y
Start
New
Reading
Sequence
Restore Register
Clear Averaging
Value
B
Page 1
E
Page 2


F
Page 5
N
Amplitude < Threshold
Y
Yes
Overhead Count=0?
Reset OHP
No
Dec. Overhead Count If Not Equal To 0
Overhead Count=32?
Yes
No
Set OHP
Inc. Overhead Count If Not Equal To 32
Add Angle To Scan Average
N
8 Angles Added
Y
-Average
-Set Cycle Complete Flag
Restore Registers
B
Page 1

```
                    ;***************************************************
                    ;*                                                 *
                    ;*  THIS MODULE IS THE START UP PROCEDURE FOR      *
                    ;*  THE DOPPLER D.F BEARING PROCESSOR              *
                    ;*  THE MODULE CONTAINS SYMBOL DEFINITION          *
                    ;*                                                 *
                    ;*                              APR  1982          *
                    ;*                                                 *
                    ;***************************************************

                    ;MEMORY MAPPED I/O
                    ;*****************

          1800      CTRL1  EQU 1800H        ;CONTROL PIO
          1801      CTRL2  EQU 1801H
          1802      CTRL3  EQU 1802H
          1803      CTRL4  EQU 1803H
          2000      IM1    EQU 2000H        ;IMAGINARY PIO
          2001      IM2    EQU 2001H
          2002      IM3    EQU 2002H
          2003      IM4    EQU 2003H
          2004      REAL1  EQU 2004H        ;REAL PIO
          2005      REAL2  EQU 2005H
          2006      REAL3  EQU 2006H
          2007      REAL4  EQU 2007H
          200C      AJST1  EQU 200CH        ;AJST PIO
          200D      AJST2  EQU 200DH
          200E      AJST3  EQU 200EH
          200F      AJST4  EQU 200FH

                    ;CONSTANTS & TABLES ADDRESSES
                    ;****************************

          0900      TABLE1 EQU 900H         ;FOR CORRECTION TABLE
          0A00      TABLE2 EQU 0A00H
          0B00      TABLE3 EQU 0B00H
          0C00      TABLE4 EQU 0C00H
          0D00      TABLE5 EQU 0D00H
          0500      TANO   EQU 500H         ;ATAN TABLE LOOK UP
          0400      CNST   EQU 400H         ;OVER HEAD PASS CONSTANT
          0064      CNST1  EQU 100          ;VARIANCE CONSTAT

                    ;RAM STORAGE
                    ;***********

          1000   >         ORG 1000H
     1000 0040      STACKS BLOCK 64         ;STACK STORAGE SPACE
     1040 0001      STACK  BLOCK 1          ;STACK POINTER
          1040   >  SPVSR  EQU STACK        ;SUPERVISOR (FLAGS)
     1041 0002      REALST BLOCK 2          ;REAL DFT STORAGE
     1043 0002      IMST   BLOCK 2          ;IM DFT STORAGE
     1045 0002      ALFA   BLOCK 2          ;G.D FORMULA STORAGE
     1047 0002      BETA   BLOCK 2          ;AVERAGING STORAGE
```

```
00054 1049 0002          TETA   BLOCK 2           ;RESULT STORAGE (BIN)
00055 104B 0002          GAMA   BLOCK 2           ;1 SCAN ANGLE STORAGE
00056 104D 0002          TETBCD BLOCK 2           ;RESULT STORAGE (BCD)
00057 104F 0001          CTRLST BLOCK 1           ;CTRL PIO OUTPUT STORAGE
00058 1050 0001          CNTCY  BLOCK 1           ;CYCLE COUNTER
00059 1051 0001          CNTSC  BLOCK 1           ;SCAN COUNTER
00060 1052 0002          VAR    BLOCK 2           ;VARIANCE CALCULATION STORAGE
00061 1054 0002          TETVAR BLOCK 2           ;AVERAGE ANGLE FOR VARIANCE
00062 1056 0002          IMABS  BLOCK 2           ;ABS(IM) STORAGE
00063 1058 0002          REABS  BLOCK 2           ;ABS(REAL) STORAGE
00064 105A 0010          QUEUE  BLOCK 16          ; STORAGE FOR LAST 8 SAMPLES
00065 106A 0001          QUECNT BLOCK 1           ;COUNTER FOR QUEUE
00066 106B 0002          TEMP   BLOCK 2           ;TEMPORARITY STARAGE
00067 106D 0001          BLKCNT BLOCK 1           ;COUNTER FOR BLANK OUT THE DISPLAY
00068 106E 0001          FLAG   BLOCK 1           ;EQUAL TO 1 INDICATING BEARING BETWEEN 0 TO 180 DEGREE
00069 106F 0001          CNT    BLOCK 1           ;SECOND COUNTER FOR BLANKING
00070 1070 0001          OVCNT  BLOCK 1           ;OVERHEAD COUNTER
00071
00072
00073      0000   >             ORG 0
00074 0000 C33B00 >             JP RSTRT
00075      0038   >             ORG 38H
00076 0038 C3BC01 >             JP INTRPT
00077
00078 003B F3             RSTRT  DI                ;DISABLE INTERRUPT
00079
00080 003C 0600                 LD B,0            ;CLEAR 256 BYTES RAM
00081 003E 210010               LD HL,1000H       ;(AREA USED FOR STORAGE)
00082 0041 3600          CLR     LD (HL),0
00083 0043 23                   INC HL
00084 0044 10FB                 DJNZ CLR
00085
00086 0046 314010 >             LD SP,STACK       ;INITIATE SP
00087 0049 3E88                 LD A,88H          ;INITIATE PIO'S (8255) FOR MODE 0 WHICH
00088                                             ; PROGRAMS PORT A,B &C low OUTPUT , PORT C up INPUT
00089 004B 320318               LD (CTRL4),A
00090 004E 3EBE                 LD A,0BEH         ;PROGRAM AS MODE 1 FOR 8255 ON ANGLE & AVERAGE
00091                                             ; WHICH MAKE PORT A AND B AS INPUT
00092 0050 320320               LD (IM4),A
00093 0053 320720               LD (REAL4),A
00094 0056 3E05                 LD A,05H
00095 0058 320320               LD (IM4),A
00096 005B 320720               LD (REAL4),A
00097 005E 3E09                 LD A,09H
00098 0060 320320               LD (IM4),A
00099 0063 320720               LD (REAL4),A
00100 0066 3E99                 LD A,99H
00101 0068 320F20               LD (AJST4),A
00102
00103 006B 3E00                 LD A,0            ;INITIATE SPVSR
00104 006D 324010 >             LD (SPVSR),A
00105 0070 3E08                 LD A,8            ;INITIATE SCAN COUNTER
00106 0072 325110 >             LD (CNTSC),A
```

```
00107 0075 3E01            LD A,1          ;INITIATE CYCLE COUNTER
00108 0077 325010  >       LD (CNTCY),A
00109 007A 3E08            LD A,8          ;INITIATE CONTROL OUTPUTS
00110 007C 320218          LD (CTRL3),A
00111 007F 324F10  >       LD (CTRLST),A
00112
00113 0082 210000          LD HL,0
00114 0085 224B10  >       LD (GAMA),HL
00115 0088 ED56            IM 1            ;ENTER INT MODE 1
00116 008A C3BF00  >       JP MAIN         ;GOTO MAIN
```

```
00118                       ;*********************************************
00119                       ;*                                           *
00120                       ;*  THIS MODULE CALCULATES ARITHMATIC AVERAGE *
00121                       ;*  OF SEVERAL CYCLES  (1 CYCLE = 7 SCANS)    *
00122                       ;*  ACCORDING TO THE INTEGRATION CONSTANT AND *
00123                       ;*  DISPLAYS THE BEARING ANGLE IN 4 DIGIT BCD *
00124                       ;*  DISPLAY ACCURACY .1 DEG ( 000.0 - 360.0 ) *
00125                       ;*  DISPLAY INCLUDES ANTENNA AJST AND QDM/QDR *
00126                       ;*                                           *
00127                       ;*********************************************
00128
00129
00130 008D FB             ENINT  EI                ;ENABLE INTERRUPTS
00131 008E 3A4010   >     MAIN   LD A,(SPVSR)      ;CHECK CYCLE COMPLETE FLAG
00132 0091 CB7F                  BIT 7,A           ;IF ZERO CHECK AGAIN
00133 0093 28F8                  JR Z,ENINT        ;ELSE CONTINUE
00134
00135 0095 CBBF                  RES 7,A
00136 0097 324010   >            LD (SPVSR),A      ;RESET FLAG
00137 009A 2A4710   >            LD HL,(BETA)
00138 009D ED5B4510>             LD DE,(ALFA)
00139 00A1 19                    ADD HL,DE         ;ADD ALFA TO BETA
00140 00A2 224710   >            LD (BETA),HL      ;(FOR LATER AVERAGE)
00141 00A5 210000                LD HL,0           ;LOAD 0 TO ALFA
00142 00A8 224510   >            LD (ALFA),HL
00143 00AB 215010   >            LD HL,CNTCY       ;DECREMENT CYCLE COUNT
00144 00AE 35                    DEC (HL)          ;CHECK IF ZERO
00145 00AF 20DD                  JR NZ,MAIN        ;IF NOT GOTO MAIN
00146
00147 00B1 2A4710   >            LD HL,(BETA)      ;DIVIDE BETA BY
00148 00B4 E603                  AND 00000011B     ;NUMBER OF CYCLES
00149 00B6 2807           AVRAGE JR Z,DSPLY        ;(ACCORDING TO INT CNST)
00150 00B8 CB3C                  SRL H
00151 00BA CB1D                  RR L
00152 00BC 3D                    DEC A
00153 00BD 18F7                  JR AVRAGE
00154
00155 00BF 110000         DSPLY  LD DE,0           ;LOAD 0 TO (BETA)
00156 00C2 ED534710>             LD (BETA),DE
00157
00158 00C6 3A0218                LD A,(CTRL3)      ;CHECK QDR/QDM
00159 00C9 CB67                  BIT 4,A
00160 00CB 2804                  JR Z,COR90
00161 00CD 110807                LD DE,1800        ;IF QDM THEN ADD 180 DEG
00162 00D0 19                    ADD HL,DE
00163 00D1 118403         COR90  LD DE,900
00164 00D4 A7                    AND A
00165 00D5 ED52                  SBC HL,DE
00166 00D7 224910   >            LD (TETA),HL
00167
00168 00DA CDA604   >            CALL NORMAL       ;BRING THE ANGL TO 0-360 DEG
00169
00170
```

```
00171                            ; SITE CORRECTION TABLE LOOK-UP ROUTINE
00172
00173
00174
00175 00DD 2A4910  >  BCD    LD HL,(TETA)
00176 00E0 E5                PUSH HL          ;SAVE
00177 00E1 06FF              LD B,-1
00178 00E3 115A00            LD DE,90
00179 00E6 04         LOOPX  INC B
00180 00E7 A7                AND A
00181 00E8 ED52              SBC HL,DE        ;FIND COREC. ADRES
00182 00EA 30FA              JR NC ,LOOPX
00183
00184
00185                 ;      FREQ CODE (8 MSB)       !       FREQ RANGE(M HZ)!       TABLE
00186                 ;      ==============================================================================
00187                 ;      91H - BFH               !       117.5 - 122     !       1
00188                 ;      69H - 91H               !       122 - 126       !       2
00189                 ;      42H- 69H                !       126 -130        !       3
00190                 ;      2DH- 42H                !       130 -132        !       4
00191                 ;      00H- 2DH                !       132 -135        !       5
00192
00193
00194
00195 00EC 3A0C20            LD A,(AJST1)
00196 00EF 0E91              LD C,91H
00197 00F1 A7                AND A
00198 00F2 91                SUB C
00199 00F3 D21701  >         JP NC,T.1        ;TABLE 1 FOR FREQ FROM 117.5 TO 120
00200 00F6 3A0C20            LD A,(AJST1)
00201 00F9 0E69              LD C,69H
00202 00FB A7                AND A
00203 00FC 91                SUB C
00204 00FD D21D01  >         JP NC,T.2        ;TABLE 2 FOR FREQ FROM 122 TO 126
00205 0100 3A0C20            LD A,(AJST1)
00206 0103 0E42              LD C,42H
00207 0105 A7                AND A
00208 0106 91                SUB C
00209 0107 D22301  >         JP NC,T.3        ;TABLE 3 FOR FREQ FROM 126 TO 130
00210 010A 3A0C20            LD A,(AJST1)
00211 010D 0E2D              LD C,2DH
00212 010F A7                AND A
00213 0110 91                SUB C
00214 0111 D22901  >         JP NC,T.4        ;TABLE 4 FOR FREQ FROM 130 TO 132
00215 0114 C32F01  >         JP T.5           ;TABLE 5 FOR FREQ FROM 132 TO 135
00216 0117 210009     T.1    LD HL,TABLE1
00217 011A C33201  >         JP CONT1
00218 011D 21000A     T.2    LD HL,TABLE2
00219 0120 C33201  >         JP CONT1
00220 0123 21000B     T.3    LD HL,TABLE3
00221 0126 C33201  >         JP CONT1
00222 0129 21000C     T.4    LD HL,TABLE4
00223 012C C33201  >         JP CONT1
```

```
00224 012F 210005     T.5    LD HL,TABLE5
00225 0132 78         CONT1  LD A,B
00226 0133 CB27              SLA A
00227 0135 A7                AND A
00228 0136 85                ADD A,L
00229 0137 3001              JR NC,SKIPX
00230 0139 24                INC H
00231 013A 6F         SKIPX  LD L,A
00232 013B 5E                LD E,(HL)          ;LOAD CORREC. TO DE
00233 013C 23                INC HL
00234 013D 56                LD D,(HL)
00235 013E E1                POP HL
00236 013F 19                ADD HL,DE          ;ADD CORR. TO ANGLE
00237 0140 224910  >         LD (TETA),HL
00238 0143 CDA604  >         CALL NORMAL
00239
00240
00241                        ;CONVERT TO BCD
00242
00243
00244 0146 2A4910  >         LD HL,(TETA)
00245 0149 11E803            LD DE,1000
00246 014C CD1204  >         CALL BINBCD     ;CALCULATE DIGIT*1000
00247 014F 78                LD A,B
00248 0150 CB27              SLA A
00249 0152 CB27              SLA A
00250 0154 CB27              SLA A
00251 0156 CB27              SLA A
00252 0158 116400            LD DE,100
00253 015B CD1204  >         CALL BINBCD     ;CALCULATE DIGIT*100
00254 015E 80                ADD A,B
00255 015F 324E10  >         LD (TETBCD+1),A
00256 0162 110A00            LD DE,10
00257 0165 CD1204  >         CALL BINBCD     ;CALCULATE DIGIT*10
00258 0168 78                LD A,B
00259 0169 CB27              SLA A
00260 016B CB27              SLA A
00261 016D CB27              SLA A
00262 016F CB27              SLA A
00263 0171 85                ADD A,L         ;REMAINDER IS LS DIGIT
00264 0172 324D10  >         LD (TETBCD),A   ;STORE BCD ANGLE IN TETBCD
00265
00266 0175 2A4D10  >         LD HL,(TETBCD)  ;DISPLAY ANGLE IN BCD
00267 0178 220018            LD (CTRL1),HL
00268 017B 3E00              LD A,0
00269 017D 326D10  >         LD (BLKCNT),A
00270 0180 214F10  >         LD HL,CTRLST
00271 0183 CBDE              SET 3,(HL)
00272 0185 210218            LD HL,CTRL3     ;OUTPUT DATA READY
00273 0188 CBDE              SET 3,(HL)      ;OUTPUT DATA VALID;;
00274 018A CBC6              SET 0,(HL)
00275 018C 1632              LD D,50
00276 018E CD9F04  >         CALL DELAY
```

```
00277 0191 CB86             RES 0,(HL)
00278
00279
00280
00281
00282                       ;SET CYCLE COUNT ACCORDING TO INTEGRATION CONSTANT
00283                       ; (READ FROM FRONT PANEL)
00284                       ;FOR INT CONSTANT=0, CYCLE COUNT =1
00285                       ;               =1,           =2
00286                       ;               =2,           =4
00287                       ;               =3,           =8
00288
00289
00290 0193 3A4010  >  CC    LD A,(SPVSR)    ;READ INT CONSTANT
00291 0196 CB76             BIT 6,(HL)
00292 0198 2804             JR Z,RES6
00293 019A CBC7             SET 0,A
00294 019C 1802             JR BIT7
00295 019E CB87       RES6  RES 0,A
00296 01A0 CB7E       BIT7  BIT 7,(HL)
00297 01A2 2804             JR Z,RES7
00298 01A4 CBCF             SET 1,A
00299 01A6 1802             JR INITSR
00300 01A8 CB8F       RES7  RES 1,A
00301 01AA 324010  >  INITSR LD (SPVSR),A
00302
00303 01AD 215010  >        LD HL,CNTCY     ;INITIATE CYCLE COUNT
00304 01B0 3601             LD (HL),1       ;ACCORDING TO INT CNST
00305 01B2 E603             AND 00000011B
00306 01B4 CA8F00  >  INITCY JP Z,MAIN      ;GOTO MAIN
00307 01B7 CB26             SLA (HL)
00308 01B9 3D               DEC A
00309 01BA 18F8             JR INITCY
```

```
                       ;*********************************************************
                       ;*                                                       *
                       ;*   THIS MODULE IS ACTIVATED EVERY SCAN BY              *
                       ;*   INTERRUPT FROM DFT CARD                             *
                       ;*   THE MODULE RECEIVES THE FOURIER TRANSFORM           *
                       ;*   OF THE PHASE DETECTOR OUTPUT (MAIN HARMONIC)        *
                       ;*   AND CALCULATES ITS PHASE (PHASE=BEARING ANG)        *
                       ;*   THE MODULE ALSO AVERAGES 8 SCANS                    *
                       ;*   AND CHECKS OVER HEAD PASS (DFT MAGNITUDE)           *
                       ;*                                                       *
                       ;*********************************************************


01BC D9                INTRPT EXX
01BD 08                       EX AF,AF
01BE 3A4010  >                LD A,(SPVSR)     ;CHECK IF SCAN FAULT
01C1 CB67                     BIT 4,A          ;IF TRUE EXIT
01C3 200E                     JR NZ,DSABL
01C5 CBE7                     SET 4,A
01C7 324010  >                LD (SPVSR),A
01CA 2A0020            OFF    LD HL,(IM1)      ;TURN OFF INT
01CD 2A0420                   LD HL,(REAL1)
01D0 C30C04  >                JP RETINT
01D3 210218            DSABL  LD HL,CTRL3
01D6 CB6E                     BIT 5,(HL)       ;Z80 DISABLE?
01D8 20F0                     JR NZ,OFF


                              ;READ SUM OF SINE(IMAGINARY) AND SUM OF COSINE(REAL)


01DA 2A0020            RDFT   LD HL,(IM1)      ;READ IM AND REAL
01DD ED5B0420                 LD DE,(REAL1)
01E1 224310  >                LD (IMST),HL     ;STORE IN IMST,REAL
01E4 ED534110>                LD (REALST),DE
01E8 CD4D04  >                CALL ABS         ;CALCULATE ABS VALUE
01EB 225610  >                LD (IMABS),HL    ;STORE IN IMABS REABS
01EE EB                       EX DE,HL
01EF CD4D04  >                CALL ABS
01F2 225810  >                LD (REABS),HL




                              ;COMPUTE ANGLE (0 TO 90 DEGREE)



01F5 2A5610  >         SIGNAL LD HL,(IMABS)    ;CHECK IF ABS(IM)>ABS(RE)
01F8 ED5B5810>                LD DE,(REABS)
01FC A7                       AND A
01FD ED52                     SBC HL,DE
01FF 3816                     JR C,TNGNT       ;IF NOT GOTO TNGNT
```

```
00364 0201 2001              JR NZ,CTNGNT    ;IF ABS(IM)=ABS(RE) DEC RE
00365 0203 1B                DEC DE
00366
00367 0204 2A5610  >  CTNGNT LD HL,(IMABS)   ;CALCULATE COTANGENT
00368 0207 EB                EX DE,HL
00369 0208 CD1E04  >         CALL DIVIDE
00370 020B CD5C04  >         CALL ATAN       ;FIND ANGLE
00371 020E 118403            LD DE,900       ;RESULT=900-RESULT
00372 0211 EB                EX DE,HL
00373 0212 A7                AND A
00374 0213 ED52              SBC HL,DE
00375 0215 1809              JR FANGLE
00376
00377 0217 2A5610  >  TNGNT  LD HL,(IMABS)   ;CALCULATE TANGENT
00378 021A CD1E04  >         CALL DIVIDE
00379 021D CD5C04  >         CALL ATAN       ;FIND ANGLE
00380
00381
00382
00383                        ;ADJUST ANGLE VALUE ACCORDING TO QUADRANT
00384
00385
00386 0220 EB         FANGLE EX DE,HL        ;CHECK TO WHICH SECTOR
00387 0221 3A4210  >         LD A,(REALST+1) ;THE ANGLE BELONG
00388 0224 CB7F              BIT 7,A         ;(0-90)(90-180)(180-270)(270-360)
00389 0226 2017              JR NZ,NREAL
00390 0228 3A4410  >         LD A,(IMST+1)
00391 022B CB7F              BIT 7,A
00392 022D 2008              JR NZ,NIMPR
00393 022F EB                EX DE,HL
00394 0230 3E01              LD A,1
00395 0232 326E10  >         LD (FLAG),A
00396 0235 1810              JR NORTH        ;ANGLE IN SECTOR 1 (0-90)
00397 0237 21100E     NIMPR  LD HL,3600      ;ANGLE IN SECTOR 4 (270-360)
00398 023A A7                AND A
00399 023B ED52              SBC HL,DE
00400 023D 1815              JR NORTH
00401 023F 210807     NREAL  LD HL,1800
00402 0242 3A4410  >         LD A,(IMST+1)
00403 0245 CB7F              BIT 7,A
00404 0247 200A              JR NZ,NIMNR
00405 0249 A7                AND A           ;ANGLE IN SECTOR 2 (90-180)
00406 024A ED52              SBC HL,DE
00407 024C 3E01              LD A,1
00408 024E 326E10  >         LD (FLAG),A
00409 0251 1801              JR NORTH
00410 0253 19         NIMNR  ADD HL,DE       ;ANGLE IN SECTOR 3 (180-270)
00411
00412 0254 E5         NORTH  PUSH HL         ;MAKE 90 DEGREE ADJECTMENT AND COMPUTE ZERO CROSSING VALUE
00413                                        ;WHICH IS USED TO REPORT TO 8748 SIGLE CHIP MICRO
00414 0255 118403            LD DE,900
00415 0258 A7                AND A
00416 0259 ED52              SBC HL,DE
```

```
00417 025B D26202  >        JP NC,SKIP0
00418 025E 11100E           LD DE,3600
00419 0261 19               ADD HL,DE
00420 0262 06FF      SKIP0  LD B,-1
00421 0264 11E100           LD DE,225
00422 0267 A7        LOOP0  AND A
00423 0268 ED52             SBC HL,DE
00424 026A 04               INC B
00425 026B D26702           JP NC,LOOP0
00426 026E 78               LD A,B
00427 026F 320D20           LD (AJST2),A           ;OUTPUT POINT NUMBER
00428 0272 E1               POP HL
00429
00430
00431                       ;CHECK FOR 270 DEGREE ZONE (FOR AVERARING)
00432
00433
00434
00435 0273 E5        NORTH1 PUSH HL
00436 0274 ED5B4B10>        LD DE,(GAMA)    ;SEE IF IN DANGER ZONE
00437 0278 A7               AND A
00438 0279 ED52             SBC HL,DE
00439 027B CD4D04  >        CALL ABS
00440 027E 110807           LD DE,1800
00441 0281 A7               AND A
00442 0282 ED52             SBC HL,DE
00443 0284 E1               POP HL
00444 0285 DABE02  >        JP C,NOTE
00445 0288 0600      CORECT LD B,0
00446 028A E5               PUSH HL
00447 028B 2A4B10  >        LD HL,(GAMA)
00448 028E 118C0A           LD DE,2700
00449 0291 A7               AND A
00450 0292 ED52             SBC HL,DE
00451 0294 E1               POP HL
00452 0295 3002             JR NC,STFLG
00453 0297 06FF             LD B,0FFH
00454 0299 78        STFLG  LD A,B
00455 029A 2F               CPL
00456 029B 47               LD B,A
00457 029C E5               PUSH HL
00458 029D 118C0A           LD DE,2700
00459 02A0 A7               AND A
00460 02A1 ED52             SBC HL,DE
00461 02A3 E1               POP HL
00462 02A4 DAB502  >        JP C,SMALL
00463 02A7 78               LD A,B
00464 02A8 B7               OR A
00465 02A9 C2BE02  >        JP NZ,NOTE
00466 02AC 11100E           LD DE,3600
00467 02AF A7               AND A
00468 02B0 ED52             SBC HL, DE
00469 02B2 C3BE02  >        JP NOTE
```

```
00470 02B5 78            SMALL  LD A,B
00471 02B6 B7                   OR A
00472 02B7 CABE02  >            JP Z,NOTE
00473 02BA 11100E               LD DE,3600
00474 02BD 19                   ADD HL,DE
00475 02BE 224B10  >     NOTE   LD (GAMA),HL
00476 02C1 226B10  >     REF    LD (TEMP),HL
00477 02C4 ED5B6B10>            LD DE,(TEMP)
00478
00479
00480
00481                           ;UPDATE THE QUEUE BY PLACEING LAST VALUE IN QUEUE
00482
00483
00484 02C8 215A10  >     STORE  LD HL,QUEUE
00485 02CB 3A6A10  >            LD A,(QUECNT)
00486 02CE A7                   AND A
00487 02CF 2805                 JR Z,NEXT2
00488
00489 02D1 47                   LD B,A
00490 02D2 23            LOOP   INC HL
00491 02D3 23                   INC HL
00492 02D4 10FC                 DJNZ LOOP
00493 02D6 73            NEXT2  LD (HL),E
00494 02D7 23                   INC HL
00495 02D8 72                   LD (HL),D
00496 02D9 3A6A10  >            LD A,(QUECNT)
00497 02DC 3C                   INC A
00498 02DD 326A10  >            LD (QUECNT),A
00499 02E0 E6F8                 AND 11111000B
00500 02E2 2805                 JR Z,GG
00501 02E4 3E00                 LD A,0
00502 02E6 326A10  >            LD (QUECNT),A
00503 02E9 00            GG     NOP
00504
00505                           ; DECIDE GOOD SIGNAL OR BAD SIGNAL BY COMPARING THE LAST 8 SAMPLER
00506
00507
00508 02EA 2A5A10  >            LD HL,(QUEUE)   ;COMPUTE RUNNING AVERAGE
00509 02ED ED5B5C10>            LD DE,(QUEUE+2)
00510 02F1 19                   ADD HL,DE
00511 02F2 ED5B5E10>            LD DE,(QUEUE+4)
00512 02F6 19                   ADD HL,DE
00513 02F7 ED5B6010>            LD DE,(QUEUE+6)
00514 02FB 19                   ADD HL,DE
00515 02FC ED5B6210>            LD DE,(QUEUE+8)
00516 0300 19                   ADD HL,DE
00517 0301 ED5B6410>            LD DE,(QUEUE+10)
00518 0305 19                   ADD HL,DE
00519 0306 ED5B6610>            LD DE,(QUEUE+12)
00520 030A 19                   ADD HL,DE
00521 030B ED5B6810>            LD DE,(QUEUE+14)
00522 030F 19                   ADD HL,DE
```

```

0310 0603               LD B,3          ;DIVIDE BY 8
0312 CB3C        LOOP2  SRL H
0314 CB1D               RR L
0316 10FA               DJNZ LOOP2



                        ;VALIDITY CHECK


0318 ED5B6B10>          LD DE,(TEMP)    ;COMPARE WITH PRESENT DATA
031C A7                 AND A
031D ED52               SBC HL,DE
031F CD4D04   >         CALL ABS
0322 116400             LD DE,CNST1
0325 A7                 AND A
0326 ED52               SBC HL,DE       ; >VAR?
0328 D22E03   >         JP NC,BAD               ;IF YES, INC BLKCNT
032B C37B03   >         JP OHP          ;IF NO, DEC BLKCNT
032E 3A6D10   > BAD     LD A,(BLKCNT)
0331 3C                 INC A
0332 326D10   >         LD (BLKCNT),A
0335 CB5F               BIT 3,A
0337 C23D03   >         JP NZ,BLANK
033A C30C04   >         JP RETINT

033D 3E00        BLANK  LD A,0
033F 327010   >         LD (OVCNT),A
0342 3A4F10   >         LD A,(CTRLST)   ;OUTPUT DATA INVALID
0345 CB8F               RES 1,A
0347 CB9F               RES 3,A
0349 324F10   >         LD (CTRLST),A
034C 32021B             LD (CTRL3),A
034F 3E00               LD A,00H
0351 326D10   >         LD (BLKCNT),A
0354 3A6F10   >         LD A,(CNT)
0357 3C                 INC A
0358 326F10   >         LD (CNT),A
035B CB57               BIT 2,A
035D CA0C04   >         JP Z,RETINT
0360 3E00               LD A,0
0362 326F10   >         LD (CNT),A
0365 210000             LD HL,0
0368 224710   >         LD (BETA),HL
036B 224510   >         LD (ALFA),HL
036E 210800             LD HL,8
0371 225110   >         LD (CNTSC),HL
0374 E1                 POP HL
0375 C39301   >         JP CC   ;GO READ INT CONSTANT

                ;;; DECIDE OVERHEAD BY COMPARING THE AMP.

```

```
00576 037B 2A5610  >  OHP    LD HL,(IMABS)
00577 037B CD3404  >         CALL MULT             ;CAL IM ** 2
00578 037E EB                EX DE,HL
00579 037F 2A3B10  >         LD HL,(REABS)         ;CAL RE ** 2
00580 0382 CD3404  >         CALL MULT
00581 0385 19                ADD HL,DE             ;CAL IM **2 + RE **2
00582 0386 3828              JR C,RESOHP
00583 0388 A7                AND A
00584 0389 010004            LD BC,CNST
00585 038C ED42              SBC HL,BC
00586 038E 3020              JR NC,RESOHP
00587
00588 0390 3A7010  >         LD A,(OVCNT)          ;INC OVERHEAD COUNT IF OVERHEAD
00589 0393 CB6F              BIT 5,A
00590 0395 C2A203  >         JP NZ,NOADD
00591 0398 3A7010  >         LD A,(OVCNT)
00592 039B 3C                INC A
00593 039C 327010  >         LD (OVCNT),A
00594 039F C3CF03  >         JP GOOD
00595 03A2 3A4F10  >  NOADD  LD A,(CTRLST)         ;TURN OVERHEAD LIGHT ON
00596 03A5 CBCF              SET 1,A
00597 03A7 320218            LD (CTRL3),A
00598 03AA 324F10  >         LD (CTRLST),A
00599 03AD C3CF03  >         JP GOOD
00600 03B0 3A7010  >  RESOHP LD A,(OVCNT)          ;DEC OVERHEAD COUNTER IF NOT OVERHEAD
00601 03B3 A7                AND A
00602 03B4 CAC103  >         JP Z,NOSUB
00603 03B7 3A7010  >         LD A,(OVCNT)
00604 03BA 3D                DEC A
00605 03BB 327010  >         LD (OVCNT),A
00606 03BE C3CF03  >         JP GOOD
00607 03C1 3A4F10  >  NOSUB  LD A,(CTRLST)         ;TURN OVERHEAD LIGHT OFF
00608 03C4 CB8F              RES 1,A
00609 03C6 324F10  >         LD (CTRLST),A
00610 03C9 320218            LD (CTRL3),A
00611 03CC C3CF03  >         JP GOOD
00612
00613 03CF 00         GOOD   NOP
00614 03D0 3A6D10  >         LD A,(BLKCNT)
00615 03D3 A7                AND A
00616 03D4 CAE103  >         JP Z,CONT11
00617 03D7 3A6D10  >         LD A,(BLKCNT)
00618 03DA 3D                DEC A
00619 03DB 326D10  >         LD (BLKCNT),A
00620 03DE C3E203  >         JP CONT31
00621 03E1 00         CONT11 NOP
00622 03E2 00         CONT31 NOP
00623
00624
00625                 ;;;;;;;;;;;;;;;;;;;;;;
00626 03E3 ED5B6B10>         LD DE,(TEMP)    ;;;
00627 03E7 2A4510  >         LD HL,(ALFA)
00628 03EA 19                ADD HL,DE       ;ELSE ADD ANGLE TO ALFA
```

```
00629 03EB 224510  >        LD (ALFA),HL     ;(FOR 8 SCAN AVERAGE)
00630 03EE 215110  >        LD HL,CNTSC
00631 03F1 35               DEC (HL)         ;DECREMENT SCAN COUNTER
00632 03F2 2018             JR NZ,RETINT     ;IF NOT ZERO EXIT
00633
00634
00635 03F4 2A4510  >        LD HL,(ALFA)     ;DIVIDE BY 8 (AVERAGE)
00636 03F7 0603             LD B,3
00637 03F9 CB3C      SCLOOP SRL H
00638 03FB CB1D             RR L
00639 03FD 10FA             DJNZ SCLOOP
00640 03FF 224510  >        LD (ALFA),HL
00641 0402 215110  >        LD HL,CNTSC      ;INITIATE SCAN COUNTER
00642 0405 3608             LD (HL),8
00643 0407 214010  >        LD HL,SPVSR      ;SET CYCLE COMPLETE FLAG
00644 040A CBFE             SET 7,(HL)       ;FOR MAIN MODULE
00645
00646
00647
00648                       ;RETURN FROM INTERRUPT
00649
00650
00651
00652 040C E1        RETINT POP HL  ;RESTORE REGISTER
00653 040D D9               EXX
00654 040E 08               EX AF,AF
00655 040F C38E00  >        JP MAIN
```

```
                   ;**********************************************
                   ;*                                            *
                   ;*   THIS MODULE CONTAINS THE PROGRAM SUBROUTINES *
                   ;*                                            *
                   ;**********************************************

                   ;BIN TO BCD SUBROUTINE
                   ;*********************

                   ;BINARY INPUT       IN HL
                   ;DECIMAL LOCATION   IN DE  (10,100,1000)
                   ;BINARY REMAINDER   IN HL
                   ;RESULT DEC DIGIT   IN B

0412 0600          BINBCD LD B,0
0414 A7            LOPBCD AND A            ;SUBTRACT DE FROM INPUT
0415 ED52                 SBC HL,DE
0417 3803                 JR C,DIGIT
0419 04                   INC B            ;RESULT IN COUNTER B
041A 18F8                 JR LOPBCD
041C 19            DIGIT  ADD HL,DE        ;RESTORE REMAINDER
041D C9                   RET


                   ;DIVIDE SUBROUTINE
                   ;*****************

                   ;DIVISOR CAN BE 15 BIT MAXIMUM !!!
                   ;DIVIDEND MUST BE SMALLER THEN DIVISOR !!!
                   ;QUOTIENT = (DIVIDEND/DIVISOR)*2**16 !!!

                   ;DIVIDEND  IN HL
                   ;DIVISOR   IN DE
                   ;QUOTIENT  IN DE
                   ;REMAINDER IN HL

041E AF            DIVIDE XOR A            ;CLEAR A AND CARRY
041F 4F                   LD C,A           ;CLEAR C
0420 0610                 LD B,16          ;SET COUNTER
0422 CB11          LOPDIV RL C             ;SHIFT IN RESULT BIT
0424 17                   RLA
0425 29                   ADD HL,HL        ;SHIFT DIVIDEND LEFT
0426 ED52                 SBC HL,DE        ;TRIAL SUBTRACT DIVISOR
0428 3001                 JR NC,COMPL      ;SUB WAS OK
042A 19                   ADD HL,DE        ;RESTORE DIVIDEND
042B 3F            COMPL  CCF              ;COMPLEMENT CARRY (RESULT)
042C 10F4                 DJNZ LOPDIV      ;COUNTER NOT ZERO
042E CB11                 RL C             ;SHIFT IN LAST RESULT BIT
0430 17                   RLA
0431 57                   LD D,A           ;MOVE RESULT FROM AC TO DE
0432 59                   LD E,C
0433 C9                   RET
```

```
00710
00711                   ;MULT SUBROUTINE
00712                   ;****************
00713
00714                   ;8 BIT * 8 BIT MULTIPLICATION !!!
00715
00716                   ;MPR    IN H
00717                   ;MPD    IN C
00718                   ;RESULT IN HL
00719
00720 0434 6C           MULT   LD L,H
00721 0435 2600                LD H,0          ;HL=MULTIPIER
00722 0437 4D                  LD C,L          ;C=MULTIPICAND
00723 0438 0608                LD B,8
00724 043A 37                  SCF
00725 043B 3F                  CCF
00726 043C CB1C         BMPI   RR H
00727 043E CB1D                RR L
00728 0440 D24604              JP NC,BMP3
00729 0443 7C                  LD A,H
00730 0444 81                  ADD A,C
00731 0445 67                  LD H,A
00732 0446 10F4         BMP3   DJNZ BMPI
00733 0448 CB1C                RR H
00734 044A CB1D                RR L
00735 044C C9                  RET
00736
00737
00738
00739                   ;ABS SUBROUTINE
00740                   ;***************
00741
00742                   ;16 BIT TWO'S COMPLEMENT NUMBER !!!
00743
00744                   ;INPUT  IN HL
00745                   ;RESULT IN HL
00746
00747 044D CB7C         ABS    BIT 7,H         ;CHECK IF POSITIVE
00748 044F 280A                JR Z,RETABS     ;IF TRUE RETURN
00749 0451 010100              LD BC,1         ;ELSE COMPLEMENT
00750 0454 7D                  LD A,L
00751 0455 2F                  CPL
00752 0456 6F                  LD L,A
00753 0457 7C                  LD A,H
00754 0458 2F                  CPL
00755 0459 67                  LD H,A
00756 045A 09                  ADD HL,BC
00757 045B C9           RETABS RET
00758
00759
00760                   ;ATAN (BINAY SEARCH) SUBROUTINE
00761                   ;******************************
00762
```

```

                          ;TABLE SPACE 1K BYTES !!!
                          ;RESOLUTION .1 DEG !!!
                          ;TIME ABOUT 1500 T STATES !!!

                          ;TAN    IN DE
                          ;RESULT IN HL

0450 010002         ATAN   LD BC,512      ;LOAD OFFSET WITH 512
045F 210005                LD HL,TANO     ;POINTER WITH TABLE START
0462 09                    ADD HL,BC      ;ADD OFFSET TO POINTER
0463 3E09                  LD A,9         ;LOAD COUNTER
0465 A7             CMPRE  AND A          ;DIVIDE OFFSET BY 2
0466 CB18                  RR B
0468 CB19                  RR C
046A E5                    PUSH HL        ;LOAD (POINTER) TO HL
046B C5                    PUSH BC
046C 4E                    LD C,(HL)
046D 23                    INC HL
046E 46                    LD B,(HL)
046F 210000                LD HL,0
0472 09                    ADD HL,BC
0473 A7                    AND A          ;COMPARE TAN WITH TABLE
0474 ED52                  SBC HL,DE
0476 C1                    POP BC
0477 E1                    POP HL
0478 3804                  JR C,GREAT     ;IF TAN > TABLE THEN
047A ED42                  SBC HL,BC      ;ADD OFFSET TO POINTER
047C 1801                  JR CONT        ;ELSE SUB FROM POINTER
047E 09             GREAT  ADD HL,BC
047F 3D             CONT   DEC A          ;REPEAT LOOP 8 TIMES
0480 20E3                  JR NZ,CMPRE
0482 E5                    PUSH HL        ;LOAD (POINTER) TO HL
0483 C5                    PUSH BC
0484 4E                    LD C,(HL)
0485 23                    INC HL
0486 46                    LD B,(HL)
0487 210000                LD HL,0
048A 09                    ADD HL,BC
048B A7                    AND A
048C ED52                  SBC HL,DE      ;LAST SEARCH
048E C1                    POP BC
048F E1                    POP HL
0490 3802                  JR C,ENDATN
0492 ED42                  SBC HL,BC
0494 010005         ENDATN LD BC,TANO     ;SUB POINTER FROM
0497 A7                    AND A          ;TABLE START
0498 ED42                  SBC HL,BC      ;RESULT=POINTER/2
049A CB3C                  SRL H
049C CB1D                  RR L
049E C9                    RET            ;RETURN


```

```
00816                       ;DELAY SUBROUTINE
00817                       ;*****************
00818
00819                       ;INPUT IN D
00820                       ;T STATES = INPUT*24 + 29
00821
00822 049F 00         DELAY  NOP
00823 04A0 00                NOP
00824 04A1 15                DEC D
00825 04A2 C29F04  >         JP NZ,DELAY
00826 04A5 C9                RET
00827
00828                              ;NORMAL SUBROUTINE
00829                            ;**********************
00830
00831                       ;THIS ROUTINE BRINGS THE ANGLE TO 0-360 RANG
00832
00833                            ;INPUT IN HL OUTPUT IN HL
00834
00835 04A6 2A4910  >  NORMAL LD HL,(TETA)
00836 04A9 11100E            LD DE,3600
00837 04AC CB7C              BIT 7,H
00838 04AE 2803              JR Z,SUB360
00839 04B0 19                ADD HL,DE
00840 04B1 1804              JR EXXX
00841 04B3 A7         SUB360 AND A
00842 04B4 ED52              SBC HL,DE
00843 04B6 D8                RET C
00844 04B7 224910  >  EXXX   LD (TETA),HL
00845 04BA C9                RET
```

```
00847                      ;*********************************************************
00848                      ;*                                                       *
00849                      ;*   THIS MODULE IS THE TANGENT LOOK UP TABLE            *
00850                      ;*   FOR FINDING THE BEARING ANGLE                       *
00851                      ;*   THE TABLE HAS .1 DEG RESOLUTION                     *
00852                      ;*                                                       *
00853                      ;*********************************************************
00854
00855      0500                 ORG TAN0          ;TABLE START ADDRESS
00856 0500 00007200             WORD 0,114,229,334,478,572,686,801
00856 0504 E5004E01
00856 0508 DE013C02
00856 050C AE022103
00857 0510 93030604             WORD 915,1030,1144,1258,1373,1487,1602,1716
00857 0514 7804EA04
00857 0518 5D05CF05
00857 051C 4206B406
00858 0520 27079907             WORD 1831,1945,2060,2174,2289,2403,2571,2632
00858 0524 0C087E08
00858 0528 F1086309
00858 052C 0B0A480A
00859 0530 BB0A2D0B             WORD 2747,2861,2976,3091,3205,3320,3435,3549
00859 0534 A00B130C
00859 0538 850CF80C
00859 053C 6B0DDD0D
00860 0540 500EC30E             WORD 3664,3779,3894,4008,4132,4238,4353,4468
00860 0544 360FA80F
00860 0548 24108E10
00860 054C 01117411
00861 0550 E7115A12             WORD 4583,4698,4813,4928,5043,5158,5273,5388
00861 0554 CD124013
00861 0558 B3132614
00861 055C 99140C15
00862 0560 7F15F215             WORD 5503,5618,5734,5849,5964,6080,6195,6310
00862 0564 6616D916
00862 0568 4C17C017
00862 056C 3318A618
00863 0570 1A198D19             WORD 6426,6541,6657,6772,6888,7004,7120,7235
00863 0574 011A741A
00863 0578 E81A5C1B
00863 057C D01B431C
00864 0580 B71C2B1D             WORD 7351,7467,7583,7699,7815,7931,8047,8163
00864 0584 9F1D131E
00864 0588 871EFB1E
00864 058C 6F1FE31F
00865 0590 5720CB20             WORD 8279,8395,8512,8628,8744,8861,8977,9094
00865 0594 4021B421
00865 0598 28229D22
00865 059C 11238623
00866 05A0 FA236F24             WORD 9210,9327,9444,9561,9678,9794,9911,10028
00866 05A4 E4245925
00866 05A8 CE254226
00866 05AC B7262C27
```

```
00867 05B0 A1271728          WORD 10145,10263,10380,10497,10615,10732,10849,10967
00867 05B4 8C280129
00867 05B8 7729EC29
00867 05BC 612AD72A
00868 05C0 4D2BC22B          WORD 11085,11202,11320,11438,11556,11674,11792,11910
00868 05C4 382CAE2C
00868 05C8 242D9A2D
00868 05CC 102E862E
00869 05D0 FC2E722F          WORD 12028,12146,12265,12383,12502,12620,12739,12858
00869 05D4 E92F5F30
00869 05D8 D6304C31
00869 05DC C3313A32
00870 05E0 B0322733          WORD 12976,13095,13214,13333,13453,13572,13691,13811
00870 05E4 9E331534
00870 05E8 8D340435
00870 05EC 7B35F335
00871 05F0 6A36E236          WORD 13930,14050,14169,14289,14409,14529,14649,14769
00871 05F4 5937D137
00871 05F8 4938C138
00871 05FC 3939B139
00872 0600 293AA23A          WORD 14889,15010,15130,15251,15371,15492,15613,15734
00872 0604 1A3B933B
00872 0608 0B3C843C
00872 060C FD3C763D
00873 0610 EF3D683E          WORD 15855,15976,16097,16219,16340,16462,16583,16705
00873 0614 E13E5B3F
00873 0618 D43F4E40
00873 061C C7404141
00874 0620 BB413542          WORD 16827,16949,17071,17193,17315,17438,17560,17683
00874 0624 AF422943
00874 0628 A3431E44
00874 062C 98441345
00875 0630 8E450946          WORD 17806,17929,18052,18175,18298,18421,18545,18668
00875 0634 8446FF46
00875 0638 7A47F547
00875 063C 7148EC48
00876 0640 6849E449          WORD 18792,18916,19040,19164,19288,19413,19537,19662
00876 0644 604ADC4A
00876 0648 584BD54B
00876 064C 514CCE4C
00877 0650 4A4DC74D          WORD 19786,19911,20036,20161,20287,20412,20538,20663
00877 0654 444EC14E
00877 0658 3F4FBC4F
00877 065C 3A50B750
00878 0660 3551B351          WORD 20789,20915,21040,21168,21294,21420,21547,21674
00878 0664 3052B052
00878 0668 2E53AC53
00878 066C 2B54AA54
00879 0670 2955A855          WORD 21801,21928,22055,22183,22310,22438,22566,22694
00879 0674 2756A756
00879 0678 2657A657
00879 067C 2658A658
00880 0680 2659A659          WORD 22822,22950,23079,23208,23336,23465,23594,23724
```

```
00880 0684 275AA85A
00880 0688 285BA95B
00880 068C 2A5CAC5C
00881 0690 2D5DAF5D          WORD 23853,23983,24113,24242,24373,24503,24633,24764
00881 0694 315EB25E
00881 0698 355FB75F
00881 069C 3960BC60
00882 06A0 3F61C261          WORD 24895,25026,25157,25288,25420,25551,25683,25815
00882 06A4 4562C862
00882 06A8 4C63CF63
00882 06AC 5364D764
00883 06B0 5C65E065          WORD 25948,26080,26212,26345,26478,26611,26745,26878
00883 06B4 6466E966
00883 06B8 6E67F367
00883 06BC 7968FE68
00884 06C0 84690A6A          WORD 27012,27146,27280,27414,27549,27684,27818,27953
00884 06C4 906A166B
00884 06C8 9D6B246C
00884 06CC AA6C316D
00885 06D0 B96D406E          WORD 28089,28224,28360,28496,28632,28768,28905,29042
00885 06D4 C86E506F
00885 06D8 D86F6070
00885 06DC E9707271
00886 06E0 FB718472          WORD 29179,29316,29453,29591,29728,29866,30005,30143
00886 06E4 0D739773
00886 06E8 2074AA74
00886 06EC 3575BF75
00887 06F0 4A76D576          WORD 30282,30421,30560,30699,30839,30979,31119,31259
00887 06F4 6077EB77
00887 06F8 77780379
00887 06FC 8F791B7A
00888 0700 A87A347B          WORD 31400,31540,31681,31823,31964,32106,32248,32390
00888 0704 C17B4F7C
00888 0708 DC7C6A7D
00888 070C F87D867E
00889 0710 147FA37F          WORD 32532,32675,32818,32961,33105,33248,33392,33536
00889 0714 3280C180
00889 0718 5181E081
00889 071C 70820083
00890 0720 91832284          WORD 33681,33826,33971,34116,34261,34407,34553,34700
00890 0724 B3844485
00890 0728 D5856786
00890 072C F9868C87
00891 0730 1E88B188          WORD 34846,34993,35140,35288,35435,35583,35731,35880
00891 0734 4489D889
00891 0738 6B8AFF8A
00891 073C 938B288C
00892 0740 BD8C528D          WORD 36029,36178,36327,36477,36627,36777,36928,37078
00892 0744 E78D7D8E
00892 0748 138FA98F
00892 074C 4090D690
00893 0750 6E910592          WORD 37230,37381,37533,37685,37837,37990,38143,38296
00893 0754 9D923593
```

```
00893 0758 CD936694
00893 075C FF949395
00894 0760 3296CC96           WORD 38450,38604,38758,38912,39067,39223,39378,39534
00894 0764 66970098
00894 0768 9B983799
00894 076C D2996E9A
00895 0770 0A9BA79B           WORD 39690,39847,40003,40161,40318,40476,40634,40793
00895 0774 439CE19C
00895 0778 7E9D1C9E
00895 077C BA9E599F
00896 0780 F79F97A0           WORD 40951,41111,41270,41430,41590,41751,41912,42073
00896 0784 36A1D6A1
00896 0788 76A217A3
00896 078C B8A359A4
00897 0790 FBA49DA5           WORD 42235,42397,42560,42722,42886,43049,43213,43377
00897 0794 40A6E2A6
00897 0798 86A729A8
00897 079C CDA871A9
00898 07A0 16AABBAA           WORD 43542,43707,43873,44038,44205,44371,44538,44706
00898 07A4 61AB06AC
00898 07A8 ADAC53AD
00898 07AC FAADA2AE
00899 07B0 49AFF2AF           WORD 44873,45042,45210,45379,45549,45719,45889,46059
00899 07B4 9AB043B1
00899 07B8 EDB197B2
00899 07BC 41B3EBB3
00900 07C0 97B442B5           WORD 46231,46402,46574,46746,46919,47092,47266,47440
00900 07C4 EEB59AB6
00900 07C8 47B7F4B7
00900 07CC A2B850B9
00901 07D0 FFB9AEBA           WORD 47615,47790,47965,48141,48317,48494,48671,48849
00901 07D4 5DBB0DBC
00901 07D8 BDBC6EBD
00901 07DC 1FBED1BE
00902 07E0 83BF36C0           WORD 49027,49206,49385,49564,49745,49925,50106,50288
00902 07E4 E9C09CC1
00902 07E8 51C205C3
00902 07EC BAC370C4
00903 07F0 26C5DCC5           WORD 50470,50652,50835,51018,51202,51387,51572,51757
00903 07F4 93C64AC7
00903 07F8 02C8BBC8
00903 07FC 74C92DCA
00904 0800 E7CAA2CB           WORD 51943,52130,52317,52504,52692,52881,53070,53260
00904 0804 5DCC18CD
00904 0808 D4CD91CE
00904 080C 4ECF0CD0
00905 0810 CAD089D1           WORD 53450,53641,53832,54024,54216,54409,54603,54797
00905 0814 48D208D3
00905 0818 C8D389D4
00905 081C 4BD50DD6
00906 0820 CFD692D7           WORD 54991,55186,55382,55579,55776,55973,56171,56370
00906 0824 56D81BD9
00906 0828 E0D9A5DA
```

```
00906 082C 6BDB32DC
00907 0830 F9DCC1DD          WORD 56569,56769,56970,57171,57372,57575,57778,57981
00907 0834 8ADE53DF
00907 0838 1CE0E7E0
00907 083C B2E17DE2
00908 0840 4AE316E4          WORD 58186,58390,58596,58802,59009,59216,59424,59633
00908 0844 E4E4B2E5
00908 0848 81E650E7
00908 084C 20E8F1E8
00909 0850 CDE995EA          WORD 59853,60053,60263,60475,60687,60900,61113,61327
00909 0854 67EB3BEC
00909 0858 0FEDE4ED
00909 085C B9EE8FEF
00910 0860 66F03EF1          WORD 61542,61758,61974,62191,62409,62628,62847,63067
00910 0864 16F2EFF2
00910 0868 C9F3A4F4
00910 086C 7FF55BF6
00911 0870 37F715F8          WORD 63287,63509,63731,63954,64178,64402,64627,64853
00911 0874 F3F8D2F9
00911 0878 B2FA92FB
00911 087C 73FC55FD
00912 0880 38FE1CFF          WORD 65080,65308,65535,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00912 0884 FFFFFFFF
00912 0888 FFFFFFFF
00912 088C FFFFFFFF
00913 0890 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00913 0894 FFFFFFFF
00913 0898 FFFFFFFF
00913 089C FFFFFFFF
00914 08A0 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00914 08A4 FFFFFFFF
00914 08A8 FFFFFFFF
00914 08AC FFFFFFFF
00915 08B0 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00915 08B4 FFFFFFFF
00915 08B8 FFFFFFFF
00915 08BC FFFFFFFF
00916 08C0 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00916 08C4 FFFFFFFF
00916 08C8 FFFFFFFF
00916 08CC FFFFFFFF
00917 08D0 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00917 08D4 FFFFFFFF
00917 08D8 FFFFFFFF
00917 08DC FFFFFFFF
00918 08E0 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00918 08E4 FFFFFFFF
00918 08E8 FFFFFFFF
00918 08EC FFFFFFFF
00919 08F0 FFFFFFFF          WORD 0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH,0FFFFH
00919 08F4 FFFFFFFF
00919 08F8 FFFFFFFF
00919 08FC FFFFFFFF
```

```
00920       0900    >         ORG TABLE1      ;TABLE FOR FREQ 117.5M HZ TO 122M HZ
00921 0900 0A000C00          WORD    10,12,  10,10,  10,12,  8,12,   7,12
00921 0904 0A000A00
00921 0908 0A000C00
00921 090C 08000C00
00921 0910 07000C00
00922 0914 0E000A00          WORD    14,10,  4,8,    2,2,    -2,6,   6,8
00922 0918 04000800
00922 091C 02000200
00922 0920 FEFF0600
00922 0924 06000800
00923 0928 0600FCFF          WORD    6,-4,   10,14,  12,14,  12,4,   8,4
00923 092C 0A000E00
00923 0930 0C000E00
00923 0934 0C000400
00923 0938 08000400
00924 093C 06001000          WORD    6,16,   10,10,  11,15,  14,8,   5,7
00924 0940 0A000A00
00924 0944 0B000F00
00924 0948 0E000800
00924 094C 05000700
00925 0950 0A000C00          WORD    10,12,  10,10,  10,12,  8,12,   7,12
00925 0954 0A000A00
00925 0958 0A000C00
00925 095C 08000C00
00925 0960 07000C00
00926
00927
00928
00929       0A00    >         ORG TABLE2
00930 0A00 15001400          WORD    21,20,  19,18,  16,14,  11,10,  9,8
00930 0A04 13001200
00930 0A08 10000E00
00930 0A0C 0B000A00
00930 0A10 09000800
00931 0A14 09000A00          WORD    9,10,   11,15,  17,19,  21,22,  21,20
00931 0A18 0B000F00
00931 0A1C 11001300
00931 0A20 15001600
00931 0A24 15001400
00932 0A28 12001000          WORD    18,16,  15,13,  13,13,  14,15,  16,17
00932 0A2C 0F000D00
00932 0A30 0D000D00
00932 0A34 0E000F00
00932 0A38 10001100
00933 0A3C 12001300          WORD    18,19,  21,22,  23,24,  25,25,  24,23
00933 0A40 15001600
00933 0A44 17001800
00933 0A48 19001900
00933 0A4C 18001700
00934 0A50 15001400          WORD    21,20,  19,18,  16,14,  11,10,  9,8
00934 0A54 13001200
00934 0A58 10000E00
```

```
00934 0A5C 0B000A00
00934 0A60 09000B00
00935
00936
00937      0B00   >         ORG TABLE3
00938 0B00 2A002600         WORD    42,38,  35,32,  20,16,  6,0,    -12,-14
00938 0B04 23002000
00938 0B08 14001000
00938 0B0C 06000000
00938 0B10 F4FFF2FF
00939 0B14 F2FFF4FF         WORD    -14,-12,-6,-12, 18,18,  11,4,   16,4
00939 0B18 FAFFF4FF
00939 0B1C 12001200
00939 0B20 0B000400
00939 0B24 10000400
00940 0B28 04000000         WORD    4,0,    4,10,   14,18,  22,16,  17,28
00940 0B2C 04000400
00940 0B30 0E001200
00940 0B34 16001000
00940 0B38 11001C00
00941 0B3C 1C001A00         WORD    28,26,  28,14,  24,22,  19,18,  25,40
00941 0B40 1C000E00
00941 0B44 18001600
00941 0B48 13001200
00941 0B4C 19002800
00942 0B50 2A002600         WORD    42,38,  35,32,  20,16,  6,0,    -12,-14
00942 0B54 23002000
00942 0B58 14001000
00942 0B5C 06000000
00942 0B60 F4FFF2FF
00943
00944
00945      0C00   >         ORG TABLE4
00946 0C00 1D001F00         WORD    29,31,  29,23,  13,5,   1,-1,   -1,0
00946 0C04 1D001700
00946 0C08 0D000500
00946 0C0C 0100FFFF
00946 0C10 FFFF0000
00947 0C14 00000000         WORD    0,0,    0,-1,   -2,-2,  -2,-1,  -1,-1
00947 0C18 0000FFFF
00947 0C1C FEFFFEFF
00947 0C20 FEFFFFFF
00947 0C24 FFFFFFFF
00948 0C28 00000300         WORD    0,3,    10,15,  16,16,  15,13,  11,9
00948 0C2C 0A000F00
00948 0C30 10001000
00948 0C34 0F000D00
00948 0C38 0B000900
00949 0C3C 07000600         WORD    7,6,    7,9,    13,17,  17,17,  18,23
00949 0C40 07000900
00949 0C44 0D001100
00949 0C48 11001100
00949 0C4C 12001700
```

```
00950 0C50 1D001F00         WORD    29,31,  29,23,  13,5,   1,-1,   -1,0
00950 0C54 1D001700
00950 0C58 0D000500
00950 0C5C 0100FFFF
00950 0D60 FFFF0000
00951
00952
00953
00954      0D00             ORG TABLES
00955 0D00 13001800         WORD    19,24,  6,12,   4,12,   16,14,  24,22
00955 0D04 06000C00
00955 0D08 04000C00
00955 0D0C 10000E00
00955 0D10 18001600
00956 0D14 14001600         WORD    20,22,  10,6,   7,10,   10,4,   2,0
00956 0D18 0A000600
00956 0D1C 07000A00
00956 0D20 0A000400
00956 0D24 02000000
00957 0D28 02000800         WORD    2,8,    10,22,  8,10,   25,0,   6,2
00957 0D2C 0A001600
00957 0D30 08000A00
00957 0D34 19000000
00957 0D38 06000200
00958 0D3C 04001300         WORD    4,19,   16,15,  25,25,  20,10,  8,19
00958 0D40 10000F00
00958 0D44 19001900
00958 0D48 14000A00
00958 0D4C 08001300
00959 0D50 13001800         WORD    19,24,  6,12,   4,12,   16,14,  24,22
00959 0D54 06000C00
00959 0D58 04000C00
00959 0D5C 10000E00
00959 0D60 18001600
00960
```

```
Scalars

   AJST1 -- 200C     AJST2 -- 200D     AJST3 -- 200E     AJST4 -- 200F     CNST --- 0400
   CNST1 -- 0064     CTRL1 -- 1800     CTRL2 -- 1801     CTRL3 -- 1802     CTRL4 -- 1803
   IM1 ---- 2000     IM2 ---- 2001     IM3 ---- 2002     IM4 ---- 2003     REAL1 -- 2004
   REAL2 -- 2005     REAL3 -- 2006     REAL4 -- 2007     TABLE1 - 0900     TABLE2 - 0A00
   TABLE3 - 0B00     TABLE4 - 0C00     TABLE5 - 0D00     TANO --- 0500

% (default) Section (1071)

   ABS ---- 044D     ALFA --- 1045     ATAN --- 045C     AVRAGE - 00B6     BAD ---- 032E
   BCD ---- 00DD     BETA --- 1047     BINBCD - 0412     BIT7 --- 01A0     BLANK -- 033D
   BLKCNT - 106D     BMP3 --- 0446     BMPI --- 043C     CC ----- 0193     CLR ---- 0041
   CMPRE -- 0465     CNT ---- 106F     CNTCY -- 1050     CNTSC -- 1051     COMPL -- 042B
   CONT --- 047F     CONT1 -- 0132     CONT11 - 03E1     CONT31 - 03E2     COR90 -- 00D1
   CORECT - 0288     CTNGNT - 0204     CTRLST - 104F     DELAY -- 049F     DIGIT -- 041C
   DIVIDE - 041E     DSABL -- 01D3     DSPLY -- 00BF     ENDATN - 0494     ENINT -- 00BD
   EXYY --- 04B7     FANGLE - 0220     FLAG --- 106E     GAMA --- 104B     GOOD --- 03CF
   GREAT -- 047E     IMABS -- 1056     INST --- 1043     INITCY - 01B4     INITSR - 01AA
   INTRPT - 01FC     LOOP --- 02D2     LOOPO -- 0267     LOOP2 -- 0312     LOOPX -- 00E6
   LOPBCD - 0414     LOPDIV - 0422     MAIN --- 008E     MULT --- 0434     NEXT2 -- 02D6
   NIMNR -- 0253     NIMPR -- 0237     NOADD -- 03A2     NORMAL - 04A6     NORTH -- 0254
   NORTH1 - 0273     NOSUB -- 03C1     NOTE --- 02BE     NREAL -- 023F     OFF ---- 01CA
   OHP ---- 0378     OVCNT -- 1070     QQ ----- 02E9     QUECNT - 106A     QUEUE -- 105A
   RDFT --- 01DA     REABS -- 1058     REALST - 1041     REF ---- 02C1     RES6 --- 019E
   RES7 --- 01A8     RESOHP - 03B0     RETABS - 045B     RETINT - 040C     RSTRT -- 003B
   SCLOOP - 03F9     SIGNAL - 01F5     SKIPO -- 0262     SKIPX -- 013A     SMALL -- 02B5
   SPVSR -- 1040     STACK -- 1040     STACKS - 1000     STFLG -- 0299     STORE -- 02C9
   SUB360 - 04B3     T.1 ---- 0117     T.2 ---- 011D     T.3 ---- 0123     T.4 ---- 0129
   T.5 ---- 012F     TEMP --- 106B     TETA --- 1049     TETBCD - 104D     TETVAR - 1054
   TNGNT -- 0217     VAR ---- 1052



  960 Source Lines     960 Assembled Lines   43841 Bytes available

             >>> No assembly errors detected <<<
```

## Tangent table : description

This table takes 1K (1024) bytes of memory and holds the value of the tangent function from zero to 90 degrees by increments of 0.1 degree.

Each entry needs two bytes. It can then be seen that exactly 920 bytes are needed for the 0 to 90 degrees range. The remaining part (from 920 to 1024) will be filled with the maximum value (all bits to one).

The exact value place in the table is equal to the tangent value of the corresponding angle, multiplied by 2 to the power of 16 (2**16). This factor of 2**16 comes from the DIVIDE routine which gives an answer multiplied by 2 **16 (providing a better resolution). As the input to the table look up routine comes from that divide routine, then the comparison is simplified.

The search is based on finding an entry in the table equal to the reference value (output of the DIVIDE routine). When a match is found, the index value (number added to the table base address to point to the proper entry) divided by 2 is the angle sought.

## Site correction table : description

An error curve was drawn according to practical measurement done with the Direction Finder Unit. From that curve, correction values were extracted and put in a tabular form.

The first entry of the table consists of the error value for angle zero. The second entry is for an angle of 5 degrees, and so on with an increment of 5 degrees until 360 degrees. A few entries are added at the end of the table corresponding to angles above $360^0$. They are in fact the same value as the first entry (0 degree and up), and are used to ease the loop-up routine.

Each entry is the error value in degrees with 0.1 degree precision. For example, a value of 20 means 2.0 degrees.

## 2.4.5 TIMING AND CONTROL

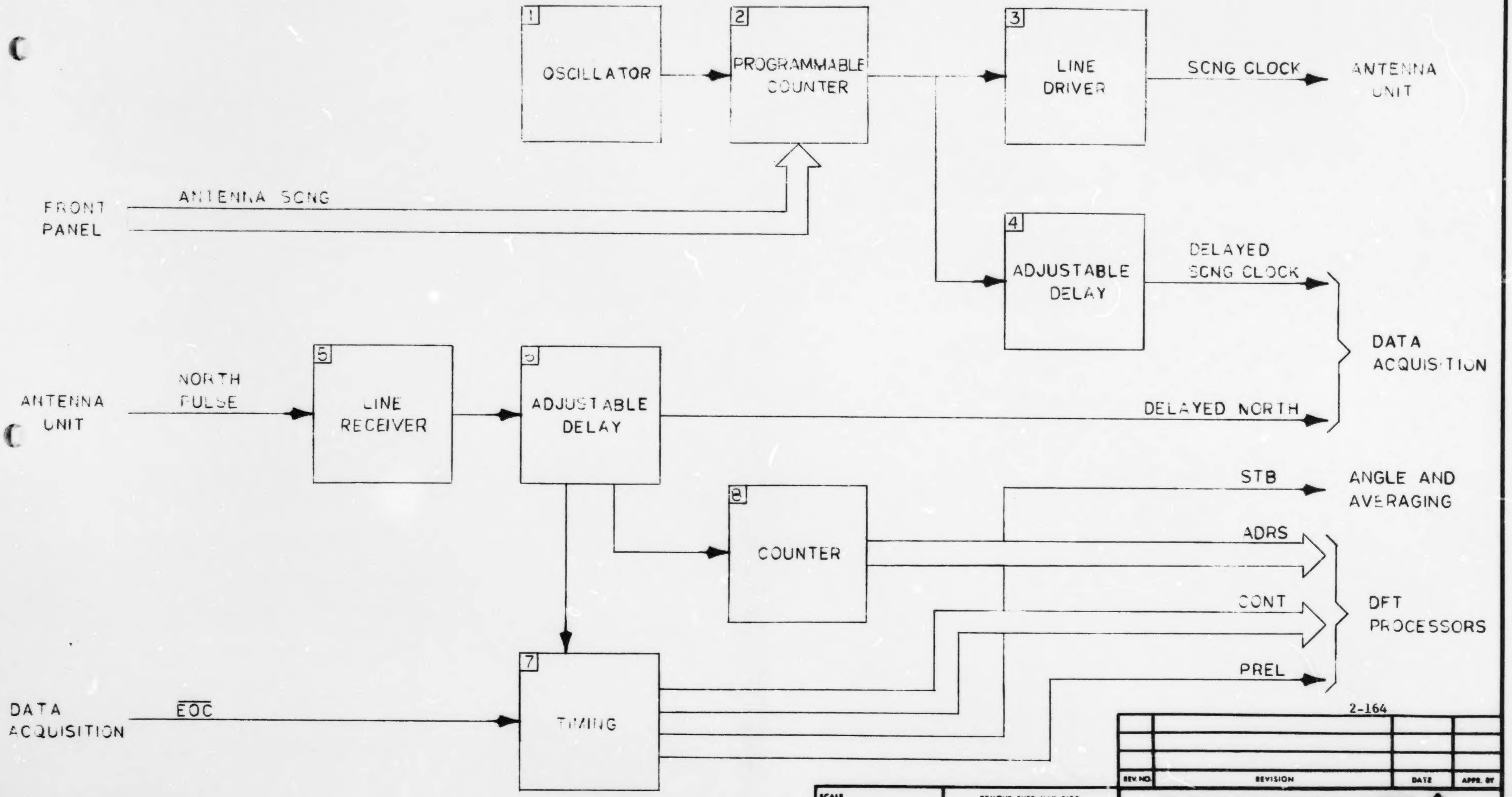
The 'Timing and Control' is used in the system to provide frequencies in a programmable ratio from the master clock located on the card.

The card also generates all the timing pulses used by the other modules in the Bearing Processor Sub-system.

The master clock is divided by 8, 9 or 10 by a programmable counter selected by the control panel. These clock pulses are then amplified to be sent to the Antenna Sub-system. It is also interfaced to the data acquisition sub-system to sample the phase readings of the phase detector module (then called Delay Scan Freq.).

The timing portion of the card receives a North pulse and $\overline{\text{EOC}}$ (End of A to D Conversion) signals from outside, and then generate 'clock B', 'clock P', 'PREL', 'TSC' and 'STB' pulses. These pulses are used to control the flow of information into the DFT processor.

The card also generates the sine-cosine Table Address for the DFT cards.



1
OSCILLATOR
2
PROGRAMMABLE COUNTER
3
LINE DRIVER
SCNG CLOCK
ANTENNA UNIT
FRONT PANEL
ANTENNA SCNG
4
ADJUSTABLE DELAY
DELAYED SCNG CLOCK
DATA ACQUISITION
ANTENNA UNIT
NORTH PULSE
5
LINE RECEIVER
6
ADJUSTABLE DELAY
DELAYED NORTH
STB
ANGLE AND AVERAGING
8
COUNTER
ADRS
CONT
DFT PROCESSORS
PREL
DATA ACQUISITION
$\overline{EOC}$
7
TIMING

| REV. NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |

SCALE

REMOVE BURR MAX 010R

MATERIAL

FINISH

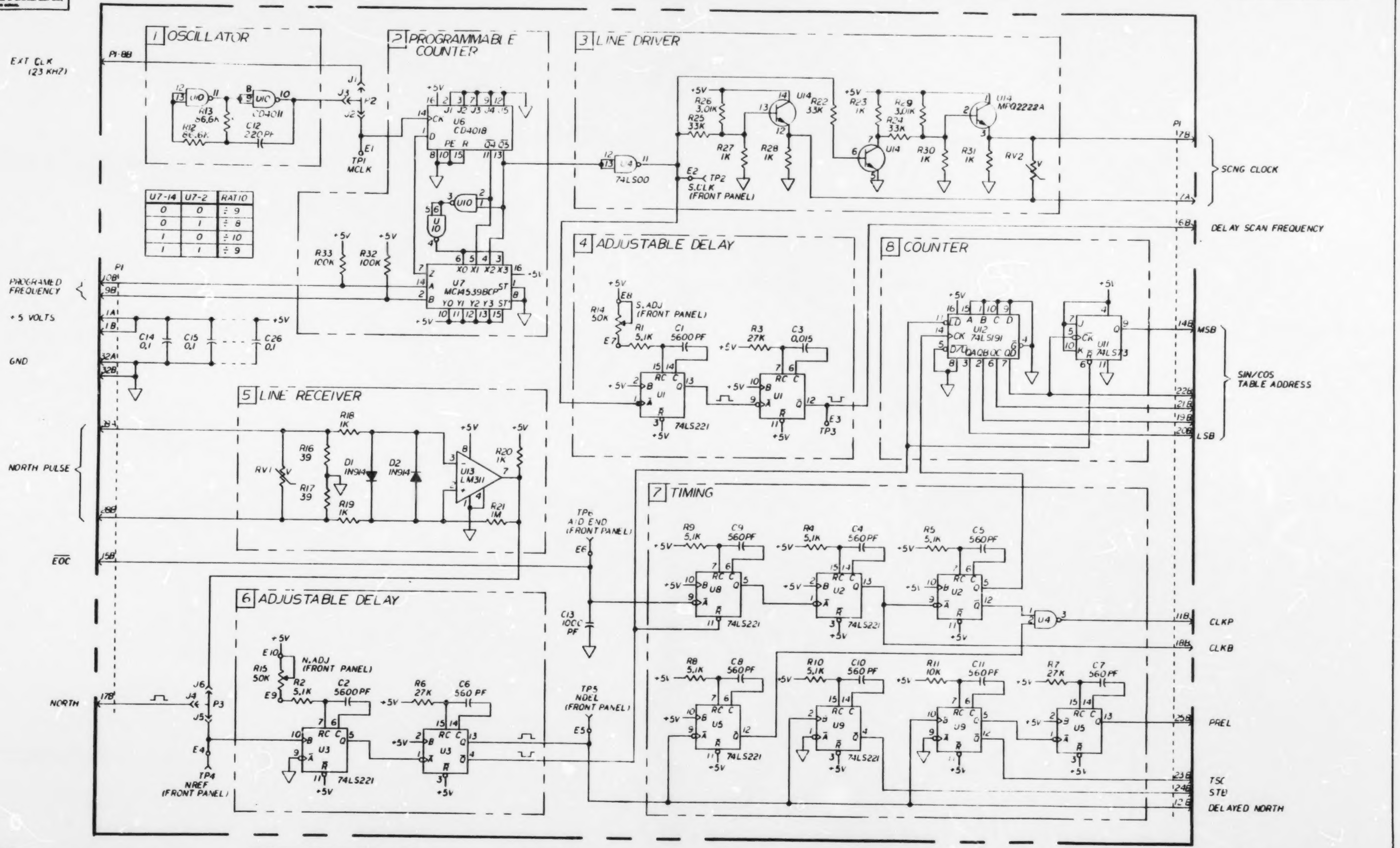
Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

UNLESS OTHERWISE SPECIFIED
TOLERANCES ANGLES
DECIMALS ± ± °

**BAYLY** ENGINEERING LTD a member of

TITLE BLOCK DIAGRAM
TIMING

| DRAWN BY | DATE | CHECKED BY | APPROVED BY | DRAWING NO. |
|---|---|---|---|---|
| F.T. | 83-02-02 | C.H | | 66-0643.029 260.BD-B |


1 OSCILLATOR
2 PROGRAMMABLE COUNTER
3 LINE DRIVER
4 ADJUSTABLE DELAY
5 LINE RECEIVER
6 ADJUSTABLE DELAY
7 TIMING
8 COUNTER
EXT CLK (23 KHZ)
P1-8B
U10
CD4011
R13 56.6K
R12 66.6K
C12 220PF
J1
J2
J3
P2
E1
TP1 MCLK
U6 CD4018
U7 MC14539BCP
R33 100K
R32 100K
PROGRAMED FREQUENCY
+5 VOLTS
GND
C14 0.1
C15 0.1
C26 0.1
U4 74LS00
E2
TP2 S.CLK (FRONT PANEL)
R26 3.01K
R25 33K
R27 1K
R28 1K
U14
R22 33K
R23 1K
R29 3.01K
R24 33K
R30 1K
R31 1K
U14 MPQ2222A
RV2
SCNG CLOCK
DELAY SCAN FREQUENCY
E8
S.ADJ (FRONT PANEL)
R14 50K
E7
R1 5.1K
C1 5600PF
R3 27K
C3 0.015
U1
74LS221
E3
TP3
U12 74LS191
U11 74LS73
MSB
SIN/COS TABLE ADDRESS
LSB
NORTH PULSE
R18 1K
R16 39
R17 39
RV1
D1 1N914
D2 1N914
U13 LM311
R20 1K
R19 1K
R21 1M
EOC
TP6 A/D END (FRONT PANEL)
E6
C13 1000 PF
E10
N.ADJ (FRONT PANEL)
R15 50K
E9
R2 5.1K
C2 5600PF
R6 27K
C6 560 PF
U3
74LS221
NORTH
J4
J5
J6
P3
E4
TP4 NREF (FRONT PANEL)
TP5 NDEL (FRONT PANEL)
E5
R9 5.1K
C9 560PF
U8
R4 5.1K
C4 560PF
U2
R5 5.1K
C5 560PF
U4
CLKP
CLKB
R8 5.1K
C8 560PF
U5
R10 5.1K
C10 560PF
U9
R11 10K
C11 560PF
R7 27K
C7 560PF
PREL
TSC
STB
DELAYED NORTH

| U7-14 | U7-2 | RATIO |
|---|---|---|
| 0 | 0 | ÷ 9 |
| 0 | 1 | ÷ 8 |
| 1 | 0 | ÷ 10 |
| 1 | 1 | ÷ 9 |

NOTES:
1- ALL RESISTOR VALUES ARE IN OHMS
2- ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

| HIGHEST DESIGNATION USED | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| C26 | D2 | E10 | J6 | P3 | R33 | RV2 | TP6 | U14 |
| DESIGNATION NOT USED | | | | | | | | |
| | | | | | | | | |

| IC'S SUPPLY DESIGNATION | | |
|---|---|---|
| DESIGNATION | +5V | GND |
| U1,2,3,5,8,9 | PIN 16 | PIN 8 |
| U4,10 | PIN 14 | PIN 7 |

BAYLY

SCHEMATIC DIAGRAM
TIMING

S B 83-2-9

66-0643.029 260.CD-0

## 2.4.5.3 TEST

a. Oscillator - programmable divider check

1. At TP1, approximately 23 KHz square wave (0 to + 5V).
2. U7-14 and U7-2 connected to GND. U6-13 square wave approximately 2.6 KHz.
3. U7-14 at GND and U7-2 at + 5V. U6-13 square wave approximately 2.9 KHz.
4. U7-14 at + 5V and U7-2 at GND. U6-13 square wave approximately 2.3 KHz.
5. U7-14 and U7-2 at + 5V. U6-13 square wave approximately 2.6 KHz.

b. Adjustment

1. Initial conditions :

   Tuning : 118.250 MHz
   Field strength : 1mV/m
   (received)
   Azimuth : 225°

2. Set-up : See figure 1.

3. Connect oscilloscope's channel 1 to point Ⓐ and channel 2 to point Ⓑ .

   Point Ⓐ is the output of the PHASE DETECTOR.
   Point Ⓑ is U6-14 on DATA ACQUISITION.

   Also connect oscilloscope's external trigger input to NORTH REFERENCE on front panel of TIMING.

4. Setting of oscilloscope :

   Trigger : external (+)
   Horizontal : 300μs/DIV
   Vert. CH.1 : 2V/DIV
   Vert. CH.2 : 0.2V/DIV

   Signal strength : 9V P.-P.

5. Refer to figure 2.

   1. Adjust R14 to get $T_1$ of Ⓐ and Ⓑ aligned as shown.
   2. Disconnect CH.1 of oscilloscope from point Ⓐ and connect it to DELAYED NORTH on front panel of TIMING.

3. Adjust R15 to have the up-going front of DELAYED NORTH PULSE Ⓒ at least 10μs later than point $T_2$.

c. Check that timing between signals correspond to the diagram of figure 3.

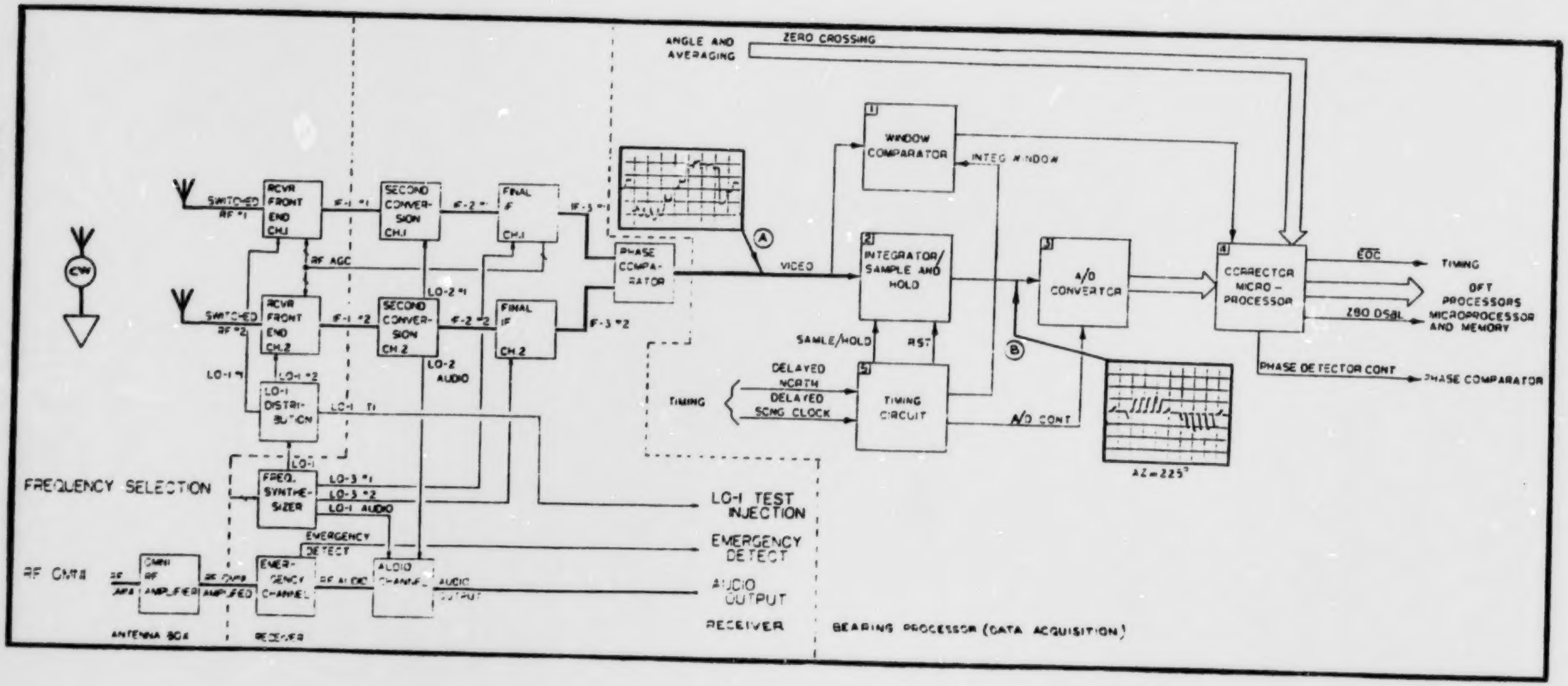

SWITCHED RF #1
SWITCHED RF #2
RCVR FRONT END CH.1
RCVR FRONT END CH.2
RF AGC
IF-1 #1
IF-1 #2
SECOND CONVERSION CH.1
SECOND CONVERSION CH.2
LO-2 #1
LO-2 AUDIO
IF-2 #1
IF-2 #2
FINAL IF CH.1
FINAL IF CH.2
IF-3 #1
IF-3 #2
PHASE COMPARATOR
CW
LO-1 #1
LO-1 #2
LO-1 DISTRIBUTION
LO-1 TI
LO-1
FREQUENCY SELECTION
FREQ. SYNTHESIZER
LO-3 #1
LO-3 #2
LO-1 AUDIO
EMERGENCY DETECT
RF OMNI
RF AMP
OMNI RF AMPLIFIER
RF OMNI AMPLIFIED
EMERGENCY CHANNEL
RF AUDIO
AUDIO CHANNEL
AUDIO OUTPUT
ANTENNA BOX
RECEIVER
LO-1 TEST INJECTION
EMERGENCY DETECT
AUDIO OUTPUT
RECEIVER
ANGLE AND AVERAGING
ZERO CROSSING
A
VIDEO
TIMING
DELAYED NORTH
DELAYED SCNG CLOCK
1 WINDOW COMPARATOR
INTEG WINDOW
2 INTEGRATOR/ SAMPLE AND HOLD
SAMLE/HOLD
RST
5 TIMING CIRCUIT
B
A/D CONT
3 A/D CONVERTOR
AZ=225°
4 CORRECTOR MICRO-PROCESSOR
$\overline{EOC}$
TIMING
DFT PROCESSORS
Z80 DSBL
MICROPROCESSOR AND MEMORY
PHASE DETECTOR CONT
PHASE COMPARATOR
BEARING PROCESSOR (DATA ACQUISITION)

Figure 1

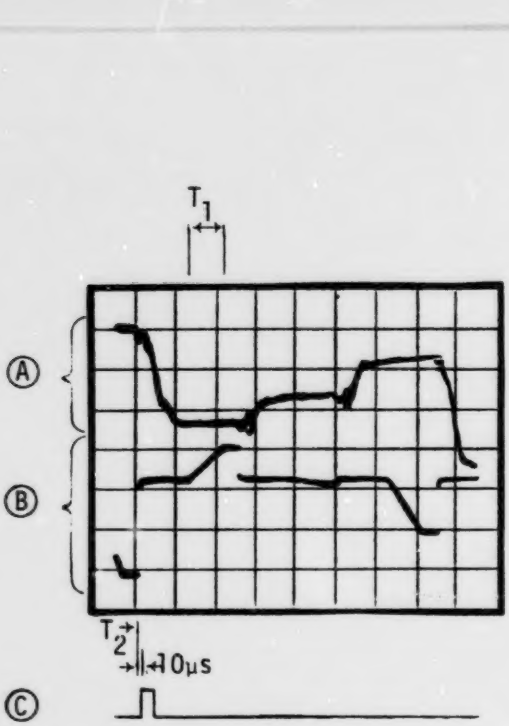


Figure 2

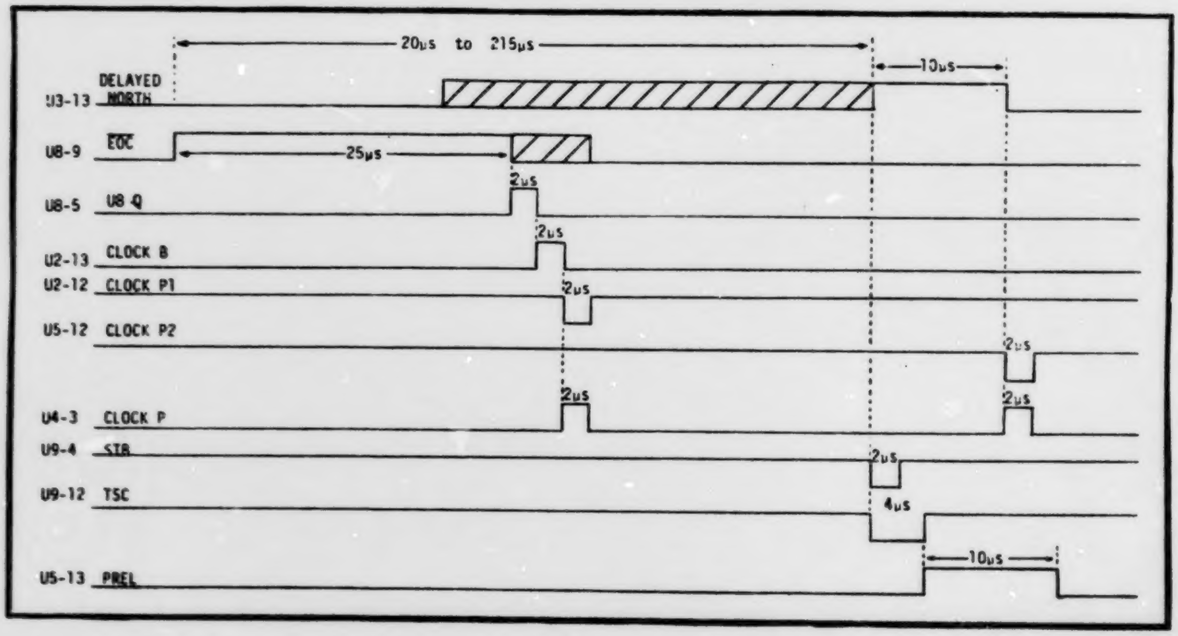
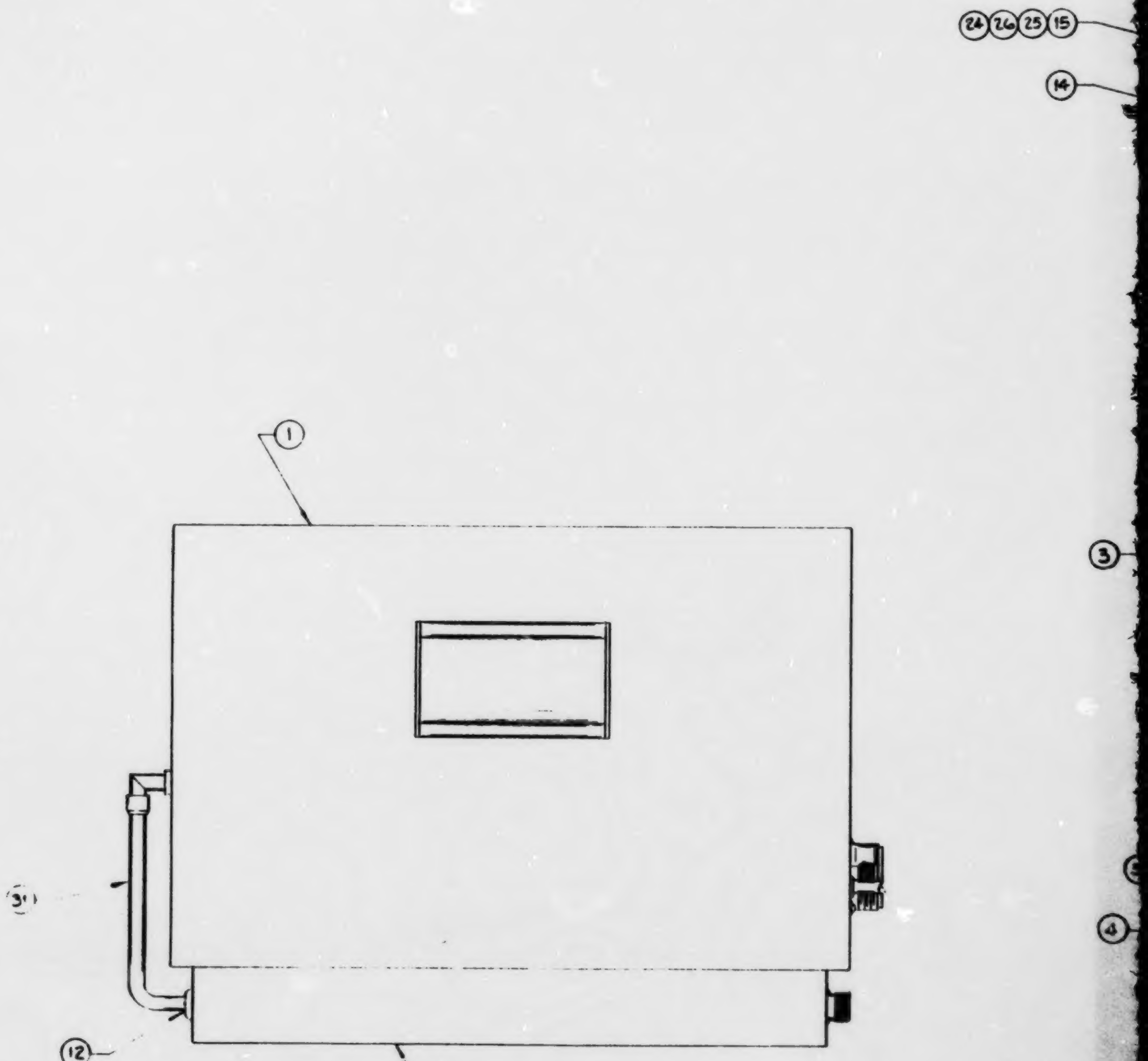

20μs to 215μs
10μs
U3-13 DELAYED NORTH
U8-9 EOC
25μs
U8-5 U8 Q
2μs
U2-13 CLOCK B
2μs
U2-12 CLOCK P1
2μs
U5-12 CLOCK P2
2μs
U4-3 CLOCK P
2μs
2μs
U9-4 STB
2μs
U9-12 TSC
4μs
U5-13 PREL
10μs

Figure 3

## 2.5 POWER SUPPLY AND INTERCONNECTIONS

### Index

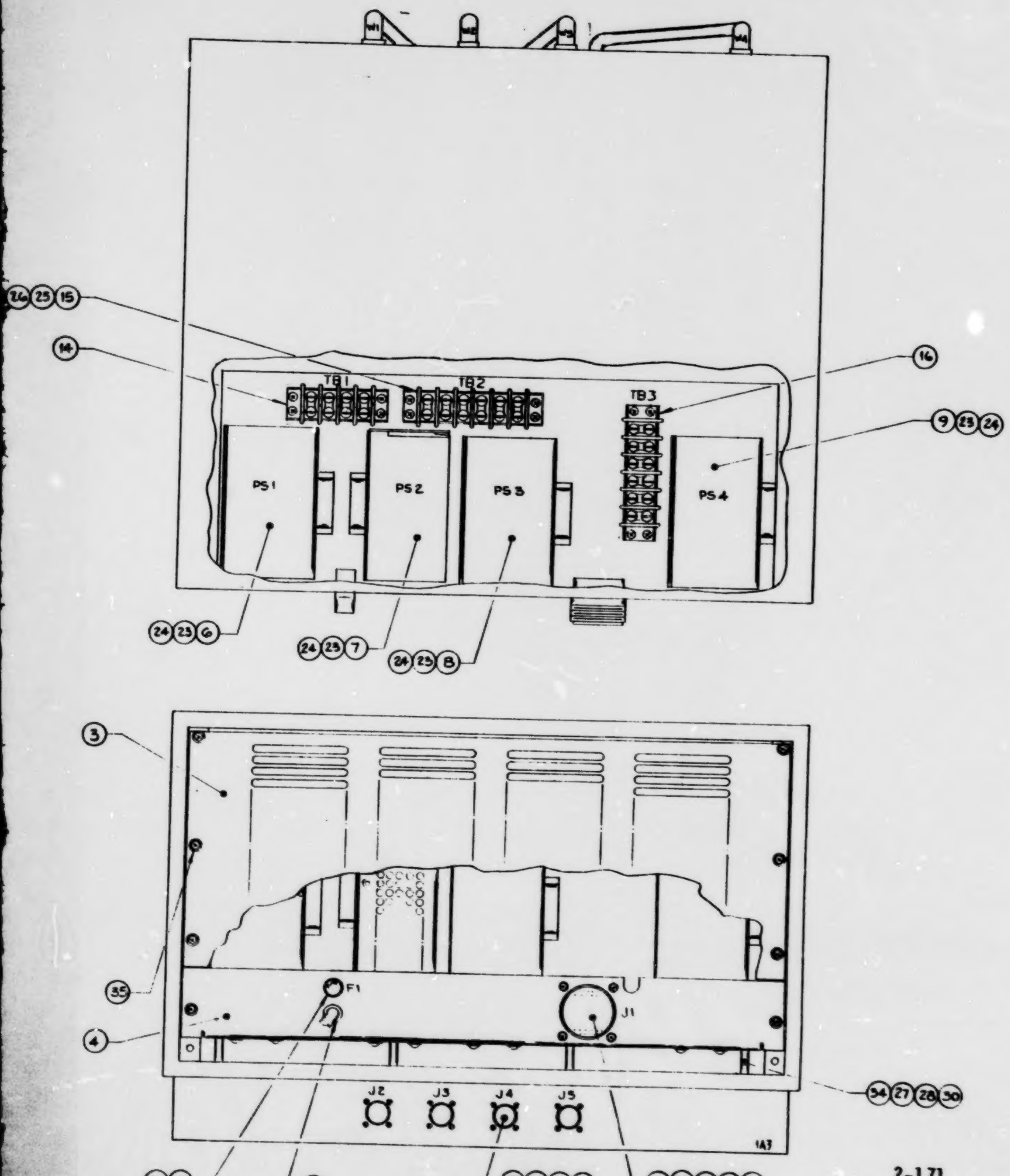
2.5.1 Power Supply Assembly
2.5.2 Antenna Unit Interconnections
2.5.3 Receiver Unit Interconnections
2.5.4 Receiver Control/Display Wiring
2.5.5 Operator's Control/Display Unit Wiring



1
2
12
31
24
26
25
15
14
3
4

NOTE

1. FOR PARTS LIST SEE 031 356 PL-A.
2. RUBBER STAMP CHARACTERS BLACK .25 HIGH IN APROX. POSITION SHOWN.
* FOR WIRING SEE 031 227 WD-D.


W1
W2
W3
W4
26 25 15
14
TB1
TB2
TB3
16
9 23 24
PS1
PS2
PS3
PS4
24 23 6
24 23 7
24 23 8
3
35
4
F1
J1
J2
J3
J4
J5
1A3
34 27 28 30
11 10
13
18 31 32 33
17 27 28 29 30

SCALE 2:1

BAYLY

CASE ASSEMBLY

# Specifications—LN series

**DC Output**

Voltage range shown in tables.

*REGULATED VOLTAGE*

| | |
|---|---|
| regulation, line | 0.1% (0.15% for LN-Z) |
| regulation, load | 0.1% (0.15% for LN-Z) |
| ripple and noise | 1.5 mV RMS, 5 mV pk-pk (5 mV RMS, 15 mV pk-pk for LNS-P-48) with either positive or negative terminal grounded. |
| temperature coefficient | 0.03%/° C |
| remote programming resistance | 200 ohms per volt nominal (LNS models only) |
| remote programming voltage | volt per volt (LNS models only) |

**AC Input**

| | |
|---|---|
| line | 105-127 VAC, 210-254 VAC (by transformer tap change) 47-440 Hz. Consult factory for operation at frequencies other than 57-63 Hz. |
| Efficiency (Typical) | 30%-5 V and 6 V models, 42% 12 V and 15 V models, 49%-20 V, 24 V, and 28 V models, 52% for 48 V model, 42% for LN duals except LND-MPU which are 34%. |

**Ambient Operating Temperature Range**

Continuous duty from 0° to +71° C with corresponding load current ratings for all modes of operation.

**Storage Temperature Range**

—55° C to 85° C.

**Overload Protection**

*ELECTRICAL*

External overload protection, automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

*THERMAL*

Thermostat—automatically reset when overtemperature condition is eliminated.

**Overshoot**

No overshoot on turn-on, turn-off or power failure.

**Overvoltage Protection**

Overvoltage protection module crowbars output when trip level is exceeded—standard on all 5 V models and both outputs of models LND-X-MPU and LND-P-MPU.

**Input and Output Connections**

Heavy-duty screw terminals on printed circuit board.

**DC Output Controls**

Simple screwdriver adjustment over the entire voltage range.

**Tracking Accuracy (Dual Tracking Models Only)**

3% absolute voltage difference, 0.2% change for all conditions of line, load and temperature.

**Remote Sensing**

Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.

**Mounting**

Three Mounting surfaces, three mounting positions. One mounting position for LN-P models.

**Convection Cooled**

No external heat sinking or forced air required.

**Transformer**

MIL-T-27C, Grade 6; Electrostatic shield; 4000 VAC input/output isolation.

**Isolation Rating**

Minimum, 10 Megohm isolation from DC to ground at 750 VDC.

**Fungus Proof**

No fungi nutrient material used.

**Military Specifications**

The LN series has passed the following tests in accordance with MIL-STD-810C.

1) Low Pressure—Method 500.1, Procedure I.
2) High Temperature—Method 501.1, Procedure I & II.
3) Low Temperature—Method 502.1, Procedure I.
4) Temperature Shock—Method 503.1, Procedure I.
5) Temperature—Altitude—Method 504.1, Procedure I. Class 2 (0° C operating)
6) Humidity—Method 507.1, Procedure I & II.
7) Fungus—Method 508.1, Procedure I.
8) Vibration—Method 514.2, Procedures X & XI.
9) Shock—Method 516.2, Procedures I & III.

MIL-I-6181D—Conducted and radiated EMI with one output terminal grounded.

**Physical Data**

| Package Model | Weight Lbs. Net | Weight Lbs. Ship | Size Inches |
|---|---|---|---|
| LN-Z | 3 | 3-1/4 | 4-7/8 x 4 x 1-3/4 (w/cover)<br>4-7/8 x 4 x 1-5/8 (w/o cover) |
| LN-Y | 5 | 5-1/2 | 5-5/8 x 4-7/8 x 2-5/8 (w/cover)<br>5-5/8 x 4-7/8 x 2-1/2 (w/o cover) |
| LN-X | 7-3/4 | 8-1/4 | 7 x 4-7/8 x 2-7/8 (w/cover)<br>7 x 4-7/8 x 2-3/4 (w/o cover) |
| LN-W | 9 | 9-1/2 | 9 x 5 x 2-7/8 (w/cover)<br>9 x 4-7/8 x 2-3/4 (w/o cover) |
| LNS-P | 14 | 15-1/2 | 11 x 4-7/8 x 4-13/32 (w & w/o cover) |
| LND-P | 15-1/2 | 17 | 11 x 4-7/8 x 4-13/32 (w & w/o cover) |

**Finish**

Gray, Fed. Std. 595 No. 26081.

**RU/CSA**

UL Recognized
CSA Certified

**Accessories**

Overvoltage protectors (standard on 5 V models and models LND-X-MPU and LND-P-MPU). See page 62.

| POWER SUPPLY SERIES | OV SERIES |
|---|---|
| LNS-Z | L-6-OV |
| LNS-Y | L-6-OV |
| LNS-X | L-12-OV |
| LNS-W | L-20-OV |
| LNS-P | L-35-OV for 5 & 6V Models<br>L-20-OV for others |
| LND (All Series) | L-12-OV |

**Guaranteed for 5 Years**

5-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

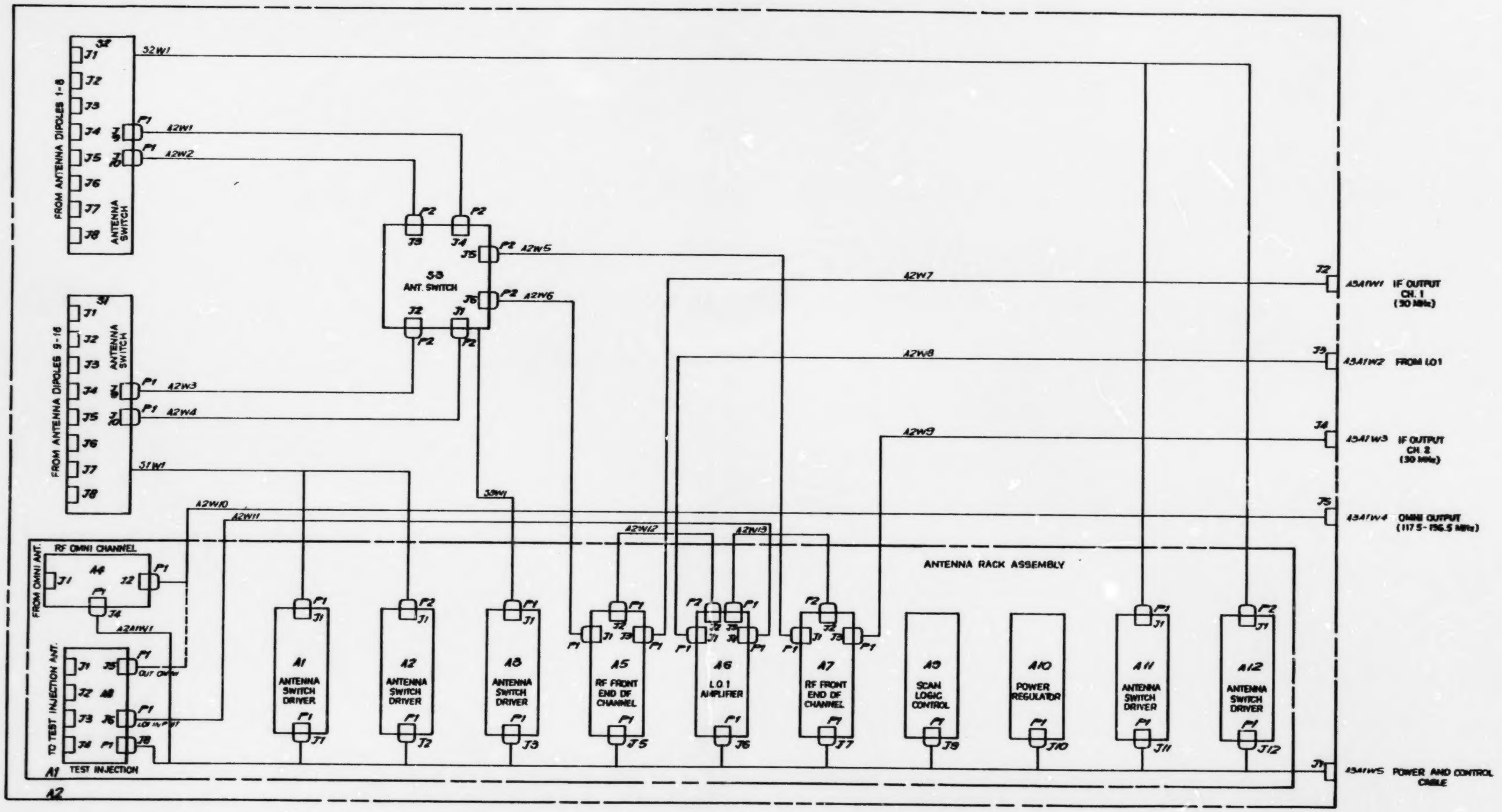
|  |  |  | MAX. AMPS AT AMBIENT OF |  |  |  |
|---|---|---|---|---|---|---|
| **MODEL** | **REGULATION (Line Load)** | **RIPPLE (RMS)** | **40°C** | **50°C** | **60°C** | **71°C** |
| LNS-X-5-OV | 0.1%, 0.1% | 1.5 mV | 10.5(8.5) | 8.9(7.6) | 7.3(6.2) | 5.3(4.5) |
| LNS-Y-24 | 0.1%, 0.1% | 1.5 mV | 2.3(2.1) | 2.1(1.9) | 1.7(1.5) | 1.1(1.0) |
| LNS-X-24 | 0.1%, 0.1% | 1.5 mV | 3.8(3.25) | 3.2(2.75) | 2.4(2.0) | 1.4(1.2) |
| LND-X-152 | 0.1%, 0.1% | 1.5 mV | 2.3(2.0) | 1.9(1.6) | 1.4(1.2) | 0.9(0.8) |

Note: Ratings in parenthesis apply when cover is being used

## 2.5.2 WIRING LIST

Antenna Control Cable (Doppler Direction Finder)

| Pin Designation | Function |
|---|---|
| A | Test Injection Bit 1 |
| B | Test Injection Bit, Ground |
| H | Test Injection Bit 0 |
| J | Test Injection Bit, Ground |
| K | System Test |
| L | System Test, Ground |
| M | Omni Antenna Test |
| N | Omni Antenna Test, Ground |
| V | +24V |
| W | Ground |
| X | Telephone Line, Conductor #1 |
| Y | Telephone Line, Conductor #2 |
| Z | Telephone Line, Ground |
| c | -24V |
| h | Ground |
| g | +15V |
| k | Ground |
| j | Scan Clock, 9b |
| l | Scan Clock, 8b |
| m | Ground |
| d | North Pulse, 6b |
| e | North Pulse, 5b |
| f | Ground |


S2
J1
J2
J3
J4
J5
J6
J7
J8
FROM ANTENNA DIPOLES 1-8
ANTENNA SWITCH
S2W1
P1
A2W1
A2W2
S1
FROM ANTENNA DIPOLES 9-16
ANTENNA SWITCH
A2W3
A2W4
S1W1
S3
ANT. SWITCH
P2
J3
J4
J5
J6
J2
J1
A2W5
A2W6
A2W7
A2W8
A2W9
A2W10
A2W11
A2W12
A2W13
S3W1
J2
A3A1W1
IF OUTPUT
CH. 1
(30 MHz)
J3
A3A1W2
FROM LO1
J4
A3A1W3
IF OUTPUT
CH. 2
(30 MHz)
J5
A3A1W4
OMNI OUTPUT
(117.5-156.5 MHz)
J1
A3A1W5
POWER AND CONTROL
CABLE
RF OMNI CHANNEL
FROM OMNI ANT.
A4
J4
A2A1W1
TO TEST INJECTION ANT.
A8
OUT OMNI
LO1 INPUT
A1
TEST INJECTION
A2
ANTENNA RACK ASSEMBLY
A1
ANTENNA SWITCH DRIVER
A2
ANTENNA SWITCH DRIVER
A3
ANTENNA SWITCH DRIVER
A5
RF FRONT END OF CHANNEL
A6
LO 1 AMPLIFIER
A7
RF FRONT END OF CHANNEL
A9
SCAN LOGIC CONTROL
A10
POWER REGULATOR
A11
ANTENNA SWITCH DRIVER
A12
ANTENNA SWITCH DRIVER
J5
J6
J7
J9
J10
J11
J12

S1W1
S2W1 } 769-0643 027 805 WL-A
S3W1 769-0643 030 843 WL-A
A2W1
A2W2
A2W3
A2W4 } 030 805 SET OF 4 CABLES. PHASE MATCHED

A2W5
A2W6 } 030 802 SET OF 2 CABLES. PHASE MATCHED
A2W12
A2W13 } SET OF 2 CABLES. PHASE MATCHED

A2W7
A2W8
A2W9
A2W10 } SET OF 4 CABLES. PHASE MATCHED
A2W11

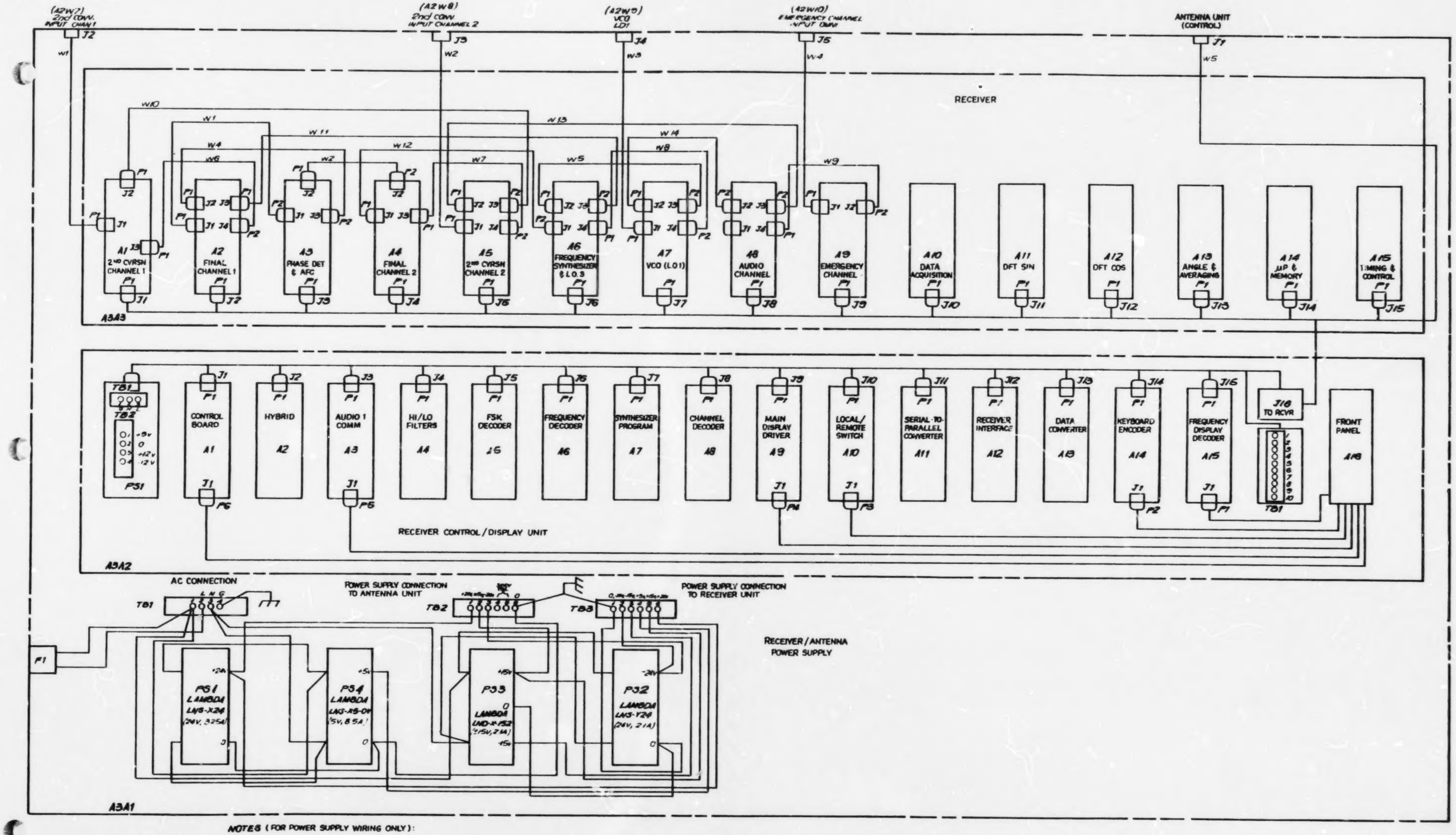
B REVISED

BAYLY

WIRING DIAGRAM
ANTENNA UNIT INTERCONNECTION

883-0643.031228 WD-B B

601-0643 031 227 wo-0


(A2W7) 2nd CONV. INPUT CHAN 1
J2
W1
(A2W8) 2nd CONV INPUT CHANNEL 2
J3
W2
(A2W9) VCO LO1
J4
W3
(A2W10) EMERGENCY CHANNEL INPUT CHAN
J5
W4
ANTENNA UNIT (CONTROL)
J7
W5
RECEIVER
W10
W1
W11
W4
W6
W2
W12
W7
W13
W5
W14
W8
W9
A1 2ND CVRSN CHANNEL 1
A2 FINAL CHANNEL 1
A3 PHASE DET & AFC
A4 FINAL CHANNEL 2
A5 2ND CVRSN CHANNEL 2
A6 FREQUENCY SYNTHESIZER & LO 3
A7 VCO (LO1)
A8 AUDIO CHANNEL
A9 EMERGENCY CHANNEL
A10 DATA ACQUISITION
A11 DFT SIN
A12 DFT COS
A13 ANGLE & AVERAGING
A14 µP & MEMORY
A15 TIMING & CONTROL
P1
P2
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
A3A3
TB1
TB2
+5V
0
+12V
-12V
PS1
CONTROL BOARD A1
HYBRID A2
AUDIO 1 COMM A3
HI/LO FILTERS A4
FSK DECODER A5
FREQUENCY DECODER A6
SYNTHESIZER PROGRAM A7
CHANNEL DECODER A8
MAIN DISPLAY DRIVER A9
LOCAL/REMOTE SWITCH A10
SERIAL-TO-PARALLEL CONVERTER A11
RECEIVER INTERFACE A12
DATA CONVERTER A13
KEYBOARD ENCODER A14
FREQUENCY DISPLAY DECODER A15
J16 TO RCVR
FRONT PANEL A16
TB1
P6
P5
P4
P3
P2
P7
RECEIVER CONTROL/DISPLAY UNIT
A3A2
AC CONNECTION
TB1
L N G
POWER SUPPLY CONNECTION TO ANTENNA UNIT
TB2
POWER SUPPLY CONNECTION TO RECEIVER UNIT
TB3
RECEIVER/ANTENNA POWER SUPPLY
F1
PS1 LAMBDA LNS-X24 (24V, 32.5A)
PS4 LAMBDA LNS-X5-OV (5V, 8.5A)
PS3 LAMBDA LND-X-152 (±15V, 2.1A)
PS2 LAMBDA LNS-Y24 (24V, 2.1A)
+24
0
+5V
+15V
-15V
-24V
A3A1

**NOTES** (FOR POWER SUPPLY WIRING ONLY):

1. COLOR CODE AC L - RED
N - WHITE
G - GREEN
DC +24V - RED
+15V - ORANGE
+5V - YELLOW
0(GND) - GREEN
-15V - BLACK
-24V BLUE
2. ALL WIRE 16G STRANDED

2-176

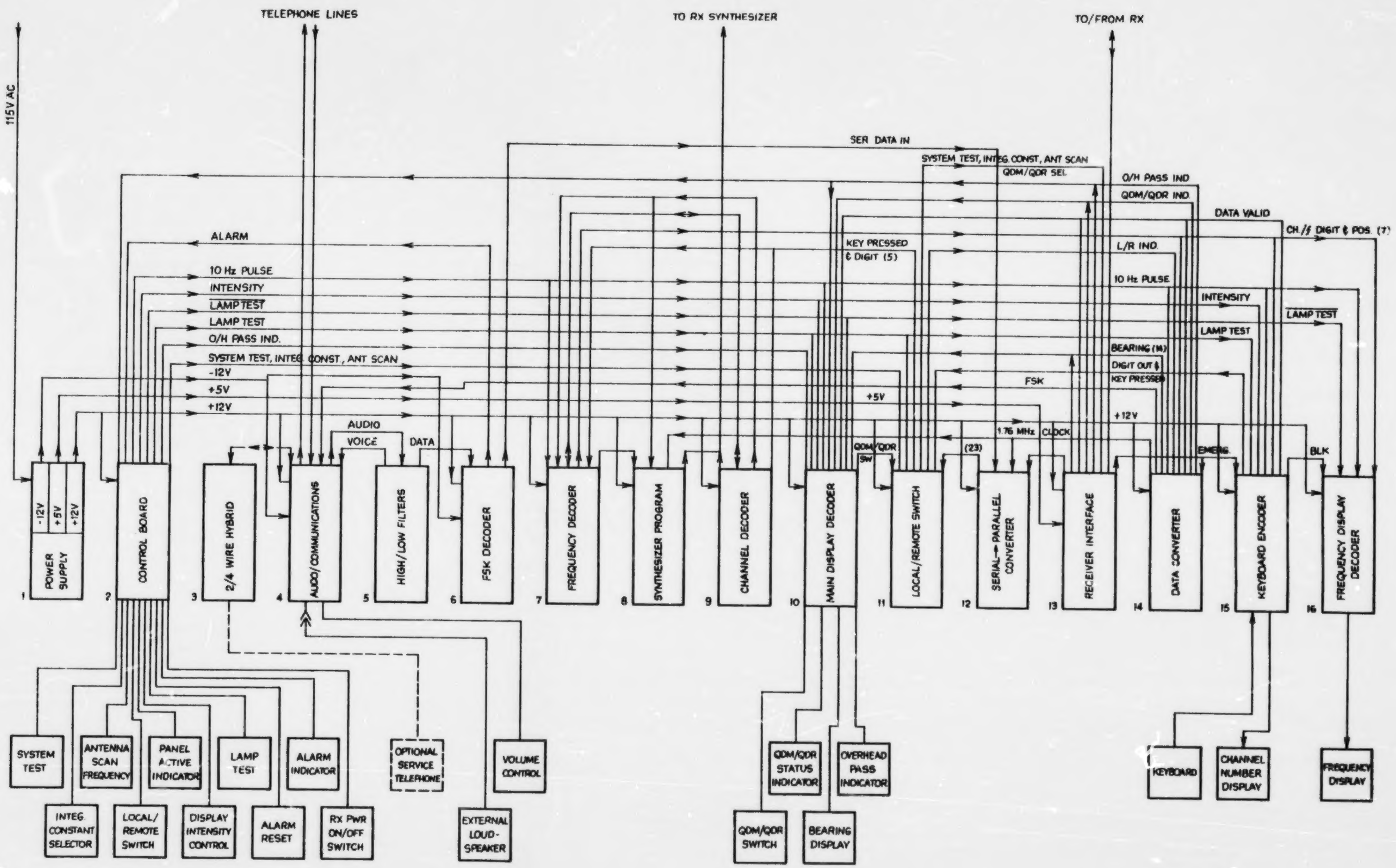
BAYLY

WIRING DIAGRAM
RECEIVER UNIT INTERCONNECTION

B REVISED 83 05 10

V P 12 04 82

DWG NO 601-0643 031 227 wo-0 B


115V AC
TELEPHONE LINES
TO RX SYNTHESIZER
TO/FROM RX
SER DATA IN
SYSTEM TEST, INTEG. CONST, ANT SCAN
QDM/QDR SEL
O/H PASS IND
QDM/QDR IND.
DATA VALID
CH./f DIGIT & POS. (7)
ALARM
KEY PRESSED & DIGIT (5)
L/R IND.
10 Hz PULSE
INTENSITY
$\overline{\text{LAMP TEST}}$
LAMP TEST
O/H PASS IND.
SYSTEM TEST, INTEG CONST, ANT SCAN
-12V
+5V
+12V
BEARING (14)
DIGIT OUT & KEY PRESSED
FSK
1.76 MHz CLOCK
(23)
QDM/QDR SW
EMERG.
BLK
AUDIO
VOICE
DATA
1 POWER SUPPLY -12V +5V +12V
2 CONTROL BOARD
3 2/4 WIRE HYBRID
4 AUDIO/COMMUNICATIONS
5 HIGH/LOW FILTERS
6 FSK DECODER
7 FREQUENCY DECODER
8 SYNTHESIZER PROGRAM
9 CHANNEL DECODER
10 MAIN DISPLAY DECODER
11 LOCAL/REMOTE SWITCH
12 SERIAL→PARALLEL CONVERTER
13 RECEIVER INTERFACE
14 DATA CONVERTER
15 KEYBOARD ENCODER
16 FREQUENCY DISPLAY DECODER
SYSTEM TEST
ANTENNA SCAN FREQUENCY
PANEL ACTIVE INDICATOR
LAMP TEST
ALARM INDICATOR
INTEG. CONSTANT SELECTOR
LOCAL/REMOTE SWITCH
DISPLAY INTENSITY CONTROL
ALARM RESET
RX PWR ON/OFF SWITCH
OPTIONAL SERVICE TELEPHONE
VOLUME CONTROL
EXTERNAL LOUD-SPEAKER
QDM/QDR STATUS INDICATOR
OVERHEAD PASS INDICATOR
QDM/QDR SWITCH
BEARING DISPLAY
KEYBOARD
CHANNEL NUMBER DISPLAY
FREQUENCY DISPLAY

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| | | | |
|---|---|---|---|
| A | ORIGINATED | 83.05.26 | |
| REV. NO | REVISION | DATE | APPD BY |

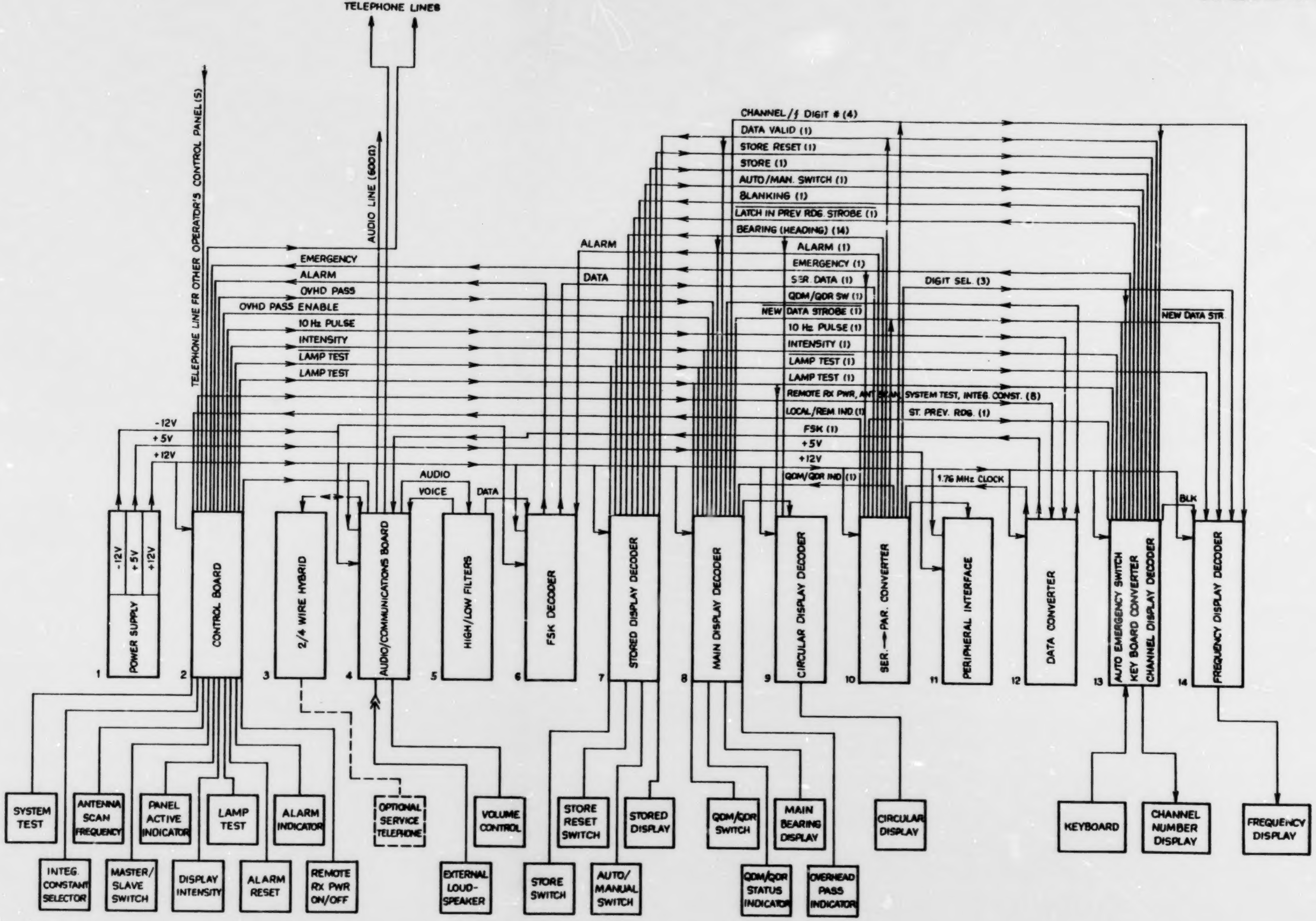
DRAWN BY: Rg  DATE: 83.5.26  CHECKED BY:  APPD BY:

BAYLY ENGINEERING LTD a member of

INTERCONNECTION DIAGRAM
RECEIVER CONTROL/DISPLAY

DWG NO 603-0643.037 653.WD-C  A

603-0643.031 407.WD-C



TELEPHONE LINES
TELEPHONE LINE FR OTHER OPERATOR'S CONTROL PANEL (5)
AUDIO LINE (600Ω)
EMERGENCY
ALARM
OVHD PASS
OVHD PASS ENABLE
10 Hz PULSE
INTENSITY
LAMP TEST
LAMP TEST
-12V
+5V
+12V
AUDIO
VOICE
DATA
ALARM
DATA
CHANNEL/ƒ DIGIT # (4)
DATA VALID (1)
STORE RESET (1)
STORE (1)
AUTO/MAN. SWITCH (1)
BLANKING (1)
LATCH IN PREV RDG. STROBE (1)
BEARING (HEADING) (14)
ALARM (1)
EMERGENCY (1)
SER. DATA (1)
QDM/QDR SW (1)
NEW DATA STROBE (1)
10 Hz PULSE (1)
INTENSITY (1)
LAMP TEST (1)
LAMP TEST (1)
REMOTE RX PWR, ANT SCAN, SYSTEM TEST, INTEG. CONST. (8)
LOCAL/REM IND (1)
ST. PREV. RDG. (1)
FSK (1)
+5V
+12V
QDM/QDR IND (1)
DIGIT SEL. (3)
NEW DATA STR.
1.76 MHz CLOCK
BLK
1
-12V
+5V
+12V
POWER SUPPLY
2
CONTROL BOARD
3
2/4 WIRE HYBRID
4
AUDIO/COMMUNICATIONS BOARD
5
HIGH/LOW FILTERS
6
FSK DECODER
7
STORED DISPLAY DECODER
8
MAIN DISPLAY DECODER
9
CIRCULAR DISPLAY DECODER
10
SER. → PAR. CONVERTER
11
PERIPHERAL INTERFACE
12
DATA CONVERTER
13
AUTO EMERGENCY SWITCH
KEY BOARD CONVERTER
CHANNEL DISPLAY DECODER
14
FREQUENCY DISPLAY DECODER
SYSTEM TEST
ANTENNA SCAN FREQUENCY
PANEL ACTIVE INDICATOR
LAMP TEST
ALARM INDICATOR
INTEG. CONSTANT SELECTOR
MASTER/SLAVE SWITCH
DISPLAY INTENSITY
ALARM RESET
REMOTE RX PWR ON/OFF
OPTIONAL SERVICE TELEPHONE
EXTERNAL LOUD-SPEAKER
VOLUME CONTROL
STORE RESET SWITCH
STORE SWITCH
AUTO/MANUAL SWITCH
STORED DISPLAY
QDM/QDR SWITCH
QDM/QDR STATUS INDICATOR
MAIN BEARING DISPLAY
OVERHEAD PASS INDICATOR
CIRCULAR DISPLAY
KEYBOARD
CHANNEL NUMBER DISPLAY
FREQUENCY DISPLAY

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV NO | REVISION | DATE | APPD BY |
|---|---|---|---|
| A | ORIGINATED | 83 05 26 | |

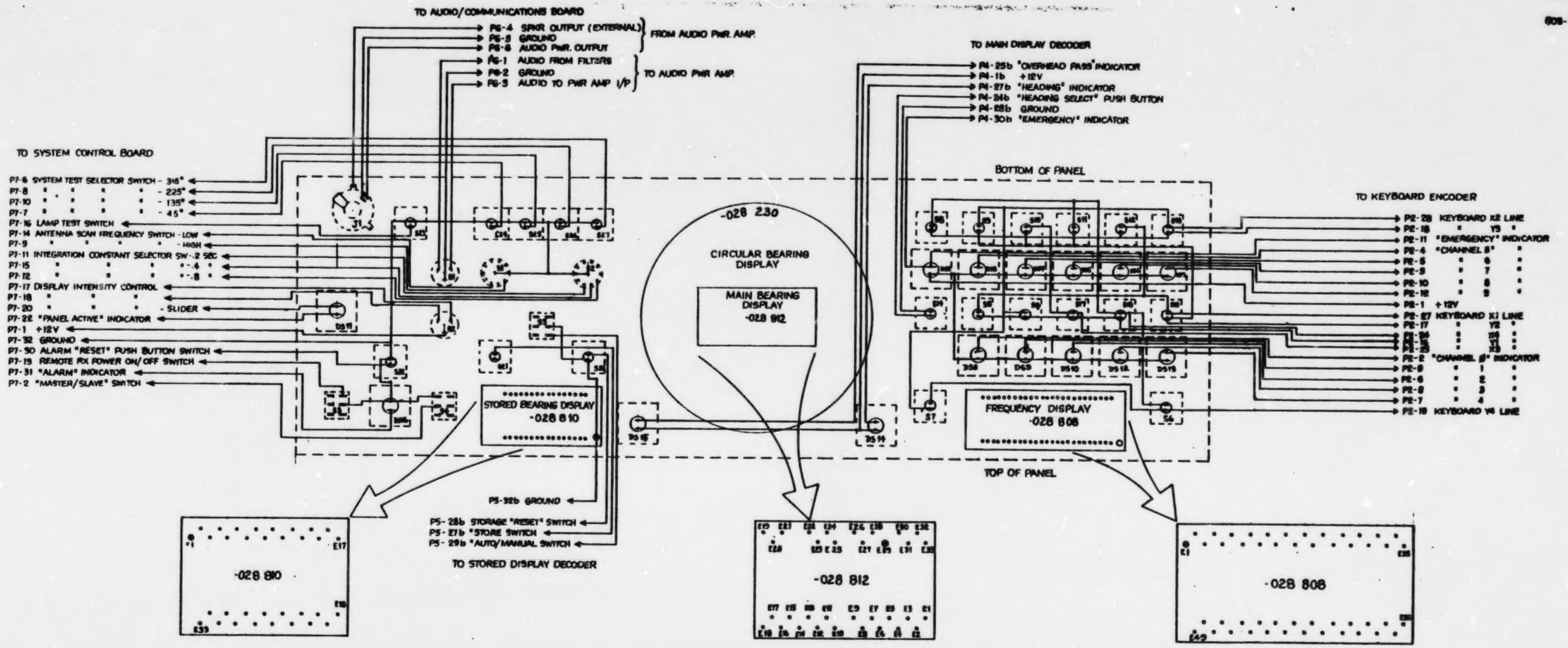
DRAWN BY Pg DATE 83.5.26

**BAYLY** ENGINEERING LTD

TITLE INTERCONNECTION DIAGRAM
OPERATOR'S CONTROL/DISPLAY UNIT

DWG NO 603-0643.031 407.WD-C A

809-0845.032 881.WD-D


TO AUDIO/COMMUNICATIONS BOARD
P6-4 SPKR OUTPUT (EXTERNAL)
P6-5 GROUND
P6-6 AUDIO PWR. OUTPUT
FROM AUDIO PWR. AMP.
P6-1 AUDIO FROM FILTERS
P6-2 GROUND
P6-3 AUDIO TO PWR AMP I/P
TO AUDIO PWR AMP.
TO MAIN DISPLAY DECODER
P4-25b "OVERHEAD PASS" INDICATOR
P4-1b +12V
P4-27b "HEADING" INDICATOR
P4-24b "HEADING SELECT" PUSH BUTTON
P4-28b GROUND
P4-30b "EMERGENCY" INDICATOR
TO SYSTEM CONTROL BOARD
P7-6 SYSTEM TEST SELECTOR SWITCH - 315°
P7-8 " " " " - 225°
P7-10 " " " " - 135°
P7-7 " " " " - 45°
P7-16 LAMP TEST SWITCH
P7-14 ANTENNA SCAN FREQUENCY SWITCH - LOW
P7-9 " " " " - HIGH
P7-11 INTEGRATION CONSTANT SELECTOR SW - .2 SEC
P7-15 " " " " - .4 "
P7-12 " " " " - .8 "
P7-17 DISPLAY INTENSITY CONTROL
P7-18 " " "
P7-20 " " " - SLIDER
P7-22 "PANEL ACTIVE" INDICATOR
P7-1 +12V
P7-32 GROUND
P7-30 ALARM "RESET" PUSH BUTTON SWITCH
P7-19 REMOTE RX POWER ON/OFF SWITCH
P7-31 "ALARM" INDICATOR
P7-2 "MASTER/SLAVE" SWITCH
BOTTOM OF PANEL
TOP OF PANEL
-028 230
CIRCULAR BEARING DISPLAY
MAIN BEARING DISPLAY -028 812
STORED BEARING DISPLAY -028 810
FREQUENCY DISPLAY -028 808
TO KEYBOARD ENCODER
P2-28 KEYBOARD X2 LINE
P2-18 " Y3 "
P2-11 "EMERGENCY" INDICATOR
P2-4 "CHANNEL 5" "
P2-5 " 6 "
P2-3 " 7 "
P2-10 " 8 "
P2-12 " 9 "
P2-1 +12V
P2-27 KEYBOARD X1 LINE
P2-17 " Y2 "
P2-16 " Y1 "
P2-15 " X1 "
P2-25 " X3 "
P2-2 "CHANNEL 0" INDICATOR
P2-9 " 1 "
P2-6 " 2 "
P2-8 " 3 "
P2-7 " 4 "
P2-19 KEYBOARD Y4 LINE
DS8 DS9 DS10 DS11 DS12 DS13 DS14 DS15
S1 S6
P5-32b GROUND
P5-28b STORAGE "RESET" SWITCH
P5-27b "STORE" SWITCH
P5-29b "AUTO/MANUAL" SWITCH
TO STORED DISPLAY DECODER
-028 810
E1 E17 E18 E39
-028 812
-028 808
E1 E26 E27 E49

| NO. | WIRE |  |  | FROM | TO |
|---|---|---|---|---|---|
|  | TYPE | COLOUR | LENGTH |  |  |
| 1 | #28 STRANDED | BLK | 2' | 028 810 E17 | P5-2b |
| 2 | #28 STRANDED | BRN | 2' | E16 | P5-3a |
| 3 | #28 STRANDED | RED | 2' | E15 | P5-4b |
| 4 | #28 STRANDED | ORANGE | 2' | E14 | P5-3b |
| 5 | #28 STRANDED | YELLOW | 2' | " E18 | P5-6b |
| 6 | #28 STRANDED | GRN | 2' | " E19 | P5-2a |
| 7 |  |  |  | " E20 |  |
| 8 | #28 STRANDED | VIO | 2' | " E21 | P5-5b |
| 9 | #28 STRANDED | BLK | 2' | " E13 | P5-7a |
| 10 | #28 STRANDED | BRN | 2' | " E12 | P5-8b |
| 11 | #28 STRANDED | RED | 2' | " E11 | P5-9b |
| 12 | #28 STRANDED | ORN | 2' | " E10 | P5-8a |
| 13 | #28 STRANDED | YEL | 2' | " E22 | P5-10b |
| 14 | #28 STRANDED | GRN | 2' | " E23 | P5-7b |
| 15 |  |  |  | " E24 |  |
| 16 | #28 STRANDED | VIO | 2' | " E25 | P5-9a |
| 17 | #28 STRANDED | BLK | 2' | " E9 | P5-11b |
| 18 | #28 STRANDED | BRN | 2' | " E8 | P5-11a |
| 19 | #28 STRANDED | RED | 2' | " E7 | P5-12a |
| 20 | #28 STRANDED | ORN | 2' | " E6 | P5-12b |
| 21 | #28 STRANDED | YEL | 2' | " E26 | P5-13a |
| 22 | #28 STRANDED | GRN | 2' | " E27 | P5-14a |
| 23 | #28 STRANDED | BLU | 2' | " E28 | P5-20b |
| 24 | #28 STRANDED | VIO | 2' | " E29 | P5-15b |
| 25 | #28 STRANDED | BLK | 2' | " E5 | P5-19b |
| 26 | #28 STRANDED | BRN | 2' | " E4 | P5-16b |
| 27 | #28 STRANDED | RED | 2' | " E3 | P5-18b |
| 28 | #28 STRANDED | ORN | 2' | " E2 | P5-17b |
| 29 | #28 STRANDED | YEL | 2' | " E30 | P5-20b |
| 30 | #28 STRANDED | GRN | 2' | " E31 | P5-14b |
| 31 |  |  |  | " E32 |  |
| 32 | #28 STRANDED | VIO | 2' | " E33 | P5-13b |
| 33 | #28 STRANDED | BLK | 2' | 028 808 E22 | P1-27a |
| 34 | #28 STRANDED | BRN | 2' | " E23 | P1-28b |
| 35 | #28 STRANDED | RED | 2' | " E24 | P1-27b |
| 36 | #28 STRANDED | ORN | 2' | " E25 | P1-26a |
| 37 | #28 STRANDED | YEL | 2' | " E26 | P1-26b |
| 38 | #28 STRANDED | GRN | 2' | " E21 | P1-23b |
| 39 |  |  |  | " E20 |  |
| 40 | #28 STRANDED | VIO | 2' | " E24 | P1-25a |
| 41 | #28 STRANDED | BLK | 2' | " E18 | P1-19a |
| 42 | #28 STRANDED | BRN | 2' | " E19 | P1-25b |
| 43 | #28 STRANDED | RED | 2' | 028 808 E20 | P1-13b |
| 44 | #28 STRANDED | GRN | 2' | " E21 | P1-18a |
| 45 | #28 STRANDED | YEL | 2' | " E33 | P1-18b |
| 46 | #28 STRANDED | GRN | 2' | " E31 | P1-17b |
| 47 |  |  |  | " E32 |  |
| 48 | #28 STRANDED | VIO | 2 | " E30 | P1-17a |
| 49 | #28 STRANDED | BLK | 2' | " E14 | P1-23a |
| 50 | #28 STRANDED | BRN | 2' | " E15 | P1-24b |
| 51 | #28 STRANDED | RED | 2' | " E16 | P1-23b |
| 52 | #28 STRANDED | ORN | 2' | " E17 | P1-22a |
| 53 | #28 STRANDED | YEL | 2' | " E37 | P1-22b |
| 54 | #28 STRANDED | GRN | 2' | " E36 | P1-21b |
| 55 | #28 STRANDED | BLU | 2' | " E34 | P1-24a |
| 56 | #28 STRANDED | VIO | 2' | " E35 | P1-21a |
| 57 | #28 STRANDED | BLK | 2' | " E10 | P1-15a |
| 58 | #28 STRANDED | BRN | 2' | " E11 | P1-16b |
| 59 | #28 STRANDED | RED | 2' | " E12 | P1-15b |
| 60 | #28 STRANDED | GRN | 2' | " E13 | P1-14a |
| 61 | #28 STRANDED | YEL | 2' | " E41 | P1-14b |
| 62 | #28 STRANDED | GRN | 2' | " E39 | P1-19b |
| 63 |  |  |  | " E40 |  |
| 64 | #28 STRANDED | VIO | 2' | " E38 | P1-13a |
| 65 | #28 STRANDED | BLK | 2' | " E6 | P1-7a |
| 66 | #28 STRANDED | BRN | 2' | " E7 | P1-8b |
| 67 | #28 STRANDED | RED | 2' | " E8 | P1-7b |
| 68 | #28 STRANDED | ORN | 2' | " E9 | P1-6a |
| 69 | #28 STRANDED | YEL | 2' | " E48 | P1-6b |
| 70 | #28 STRANDED | GRN | 2' | " E43 | P1-5b |
| 71 |  |  |  | " E44 |  |
| 72 | #28 STRANDED | VIO | 2' | " E42 | P1-5a |
| 73 | #28 STRANDED | BLK | 2' | " E2 | P1-11a |
| 74 | #28 STRANDED | BRN | 2' | " E3 | P1-12b |
| 75 | #28 STRANDED | RED | 2' | " E4 | P1-11b |
| 76 | #28 STRANDED | ORN | 2' | " E5 | P1-10a |
| 77 | #28 STRANDED | YEL | 2' | " E49 | P1-10b |
| 78 | #28 STRANDED | GRN | 2' | " E47 | P1-9b |
| 79 |  |  |  | " E45 |  |
| 80 | #28 STRANDED | VIO | 2' | " E46 | P1-9a |
| 81 | #28 STRANDED | BLK | 2' | 028 230 E1 | P3-24 |
| 82 | #28 STRANDED | BRN | 2' | " E2 | P3-23 |
| 83 | #28 STRANDED | RED | 2' | " E3 | P3-3 |
| 84 | #28 STRANDED | ORN | 2' | " E4 | P3-4 |
| 85 | #28 STRANDED | YEL | 2' | 028 230 E5 | P3-7 |
| 86 | #28 STRANDED | GRN | 2' | " E6 | P3-8 |
| 87 | #28 STRANDED | BLU | 2' | " E7 | P3-11 |
| 88 | #28 STRANDED | VIO | 2' | " E8 | P3-12 |
| 89 | #28 STRANDED | BLK | 2' | " E9 | P3-17 |
| 90 | #28 STRANDED | BRN | 2' | " E10 | P3-18 |
| 91 | #28 STRANDED | RED | 2' | " E11 | P3-19 |
| 92 | #28 STRANDED | ORN | 2' | " E12 | P3-20 |
| 93 | #28 STRANDED | YEL | 2' | " E13 | P3-22 |
| 94 | #28 STRANDED | GRN | 2' | " E14 | P3-21 |
| 95 | #28 STRANDED | BLU | 2' | " E15 | P3-27 |
| 96 | #28 STRANDED | VIO | 2' | " E16 | P3-28 |
| 97 | #28 STRANDED | BLK | 2' | " E17 | P3-29 |
| 98 | #28 STRANDED | BRN | 2' | " E18 | P3-30 |
| 99 | #28 STRANDED | RED | 2' | 028 812 E1 | P4-2b |
| 100 | #28 STRANDED | ORN | 2' | " E2 | P4-3b |
| 101 | #28 STRANDED | YEL | 2' | " E3 | P4-4b |
| 102 |  |  | 2' | " E4 |  |
| 103 | #28 STRANDED | BLU | 2' | " E33 | P4-5b |
| 104 | #28 STRANDED | VIO | 2' | " E32 | P4-6b |
| 105 | #28 STRANDED | BLK | 2' | " E31 | P4-7a |
| 106 | #28 STRANDED | BRN | 2' | " E30 | P4-7b |
| 107 | #28 STRANDED | RED | 2' | " E5 | P4-8a |
| 108 | #28 STRANDED | ORN | 2' | " E6 | P4-9a |
| 109 | #28 STRANDED | YEL | 2' | " E7 | P4-10b |
| 110 | #28 STRANDED | GRN | 2' | " E8 | P4-9b |
| 111 |  |  | 2' | " E29 |  |
| 112 | #28 STRANDED | VIO | 2' | " E28 | P4-12a |
| 113 | #28 STRANDED | BLK | 2' | " E27 | P4-11a |
| 114 | #28 STRANDED | BRN | 2' | " E26 | P4-11b |
| 115 |  |  | 2' | " E9 |  |
| 116 | #28 STRANDED | ORN | 2' | " E10 | [illegible] |
| 117 | #28 STRANDED | YEL | 2' | " E11 | [illegible] |
| 118 | #28 STRANDED | GRN | 2' | " E12 | [illegible] |
| 119 | #28 STRANDED | BLU | 2' | " E25 | P4-21a |
| 120 | #28 STRANDED | VIO | 2' | " E24 | [illegible] |
| 121 | #28 STRANDED | BLK | 2' | " E23 | P4-22a |
| 122 | #28 STRANDED | BRN | 2' | " E22 | P4-22b |
| 123 | #28 STRANDED | RED | 2' | " E13 | P4-21b |
| 124 | #28 STRANDED | ORN | 2' | " E14 | [illegible] |
| 125 | #28 STRANDED | YEL | 2' | " E15 | [illegible] |
| 126 | #28 STRANDED | GRN | 2' | " E16 | P4-16b |
| 127 | #28 STRANDED | BLU | 2' | 028 812 E17 | P4-14b |
| 128 |  |  | 2' | " E18 |  |
| 129 | #28 STRANDED | BLK | 2' | " E21 | P4-15b |
| 130 | #28 STRANDED | BRN | 2' | " E20 | P4-17b |
| 131 | #28 STRANDED | RED | 2' | " E19 | P4-18b |

NOTE: 1 FOR MECHANICAL ASSEMBLY SEE-081 407.MA-C

A ORIGINATED

BAYLY

OPERATOR'S CONTROL UNIT
FRONT PANEL WIRING DIAGRAM

DWG NO 809-0845 032 881 WD-D A

## 2.6 CONTROL AND DISPLAY MODULES

**Index**

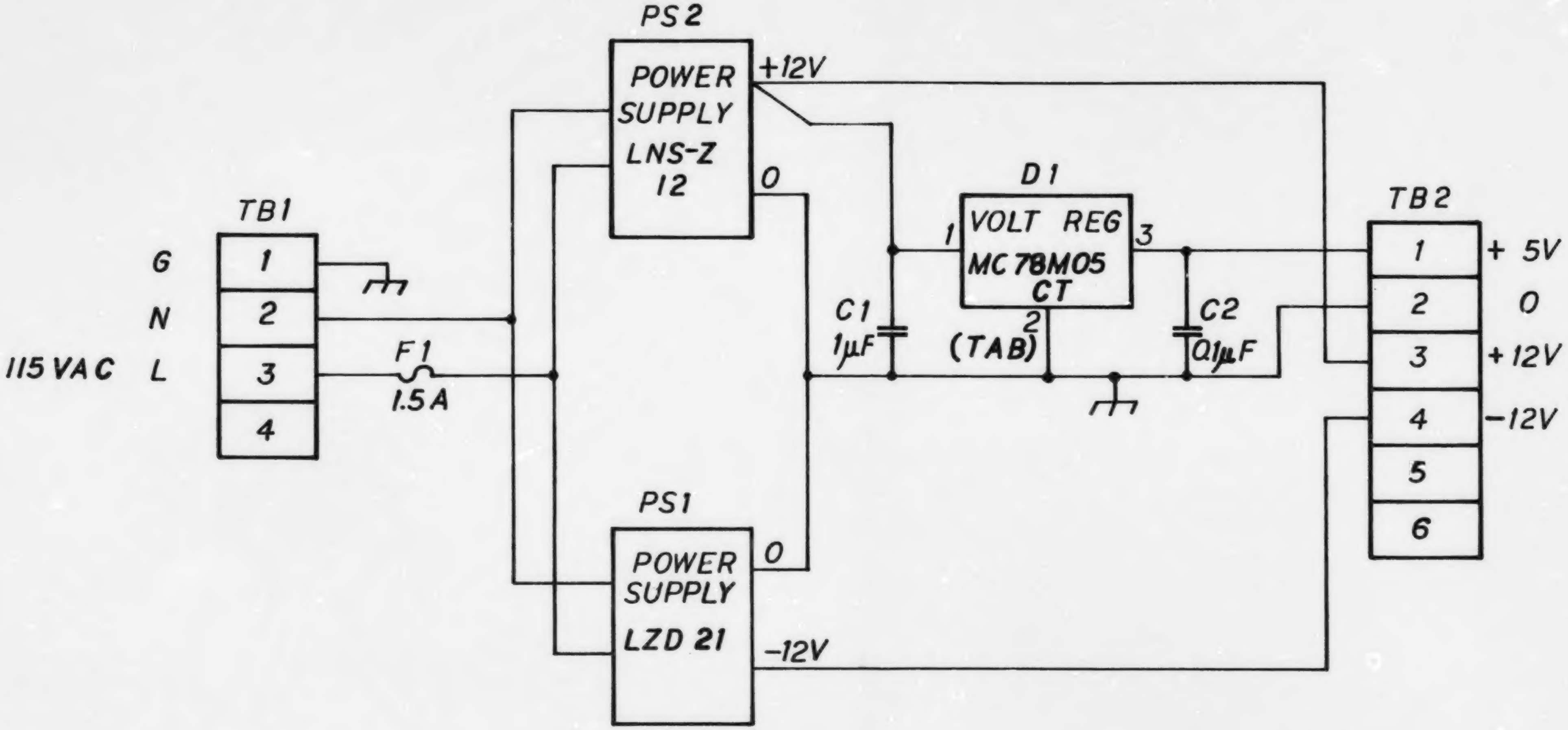
2.6.1 Power Supply
2.6.2 DF System Control Board
2.6.3 Circular Bearing Display Decoder
2.6.4 Circular Bearing Display
2.6.5 Frequency Decoder
2.6.6 Channel Decoder
2.6.7 Synthesizer Program
2.6.8 Local/Remote Switch
2.6.9 Stored Display Decoder
2.6.10 Main Display Decoder
2.6.11 Peripheral Interface
2.6.12 Receiver Interface
2.6.13 Keyboard Encoder
2.6.14 Frequency Display Decoder

### 2.6.1 Power Supply

The control panels have their own power supplies, independent of the power supplies used for the receiver circuits. This allows the data link, display and control functions to be operational while the receiver itself is switched off and also allows the receiver power to be controlled from the Operator's Control Panel.

All displays, and practically all control circuits, need +12V, while the interface circuits need +5V as well. The operational amplifiers used for the FSK Decoder, the audio amplifier, the mixer and the telephone line drivers also need -12V.

To provide all these voltages, the power supply module contains a +12V supply (PS2) and a -12V supply (PS1). The +5V supply is derived from the +12V supply using a 5V 3-Terminal Regulator.


PS2
POWER SUPPLY LNS-Z 12
+12V
0
D1
VOLT REG MC78M05 CT
1
2
3
(TAB)
TB2
1
2
3
4
5
6
+ 5V
0
+12V
−12V
TB1
1
2
3
4
G
N
L
115 VAC
F1
1.5A
C1
1µF
C2
0.1µF
PS1
POWER SUPPLY LZD 21
0
−12V

This drawing is the property of BAYLY ENGINEERING LIMITED and may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others without written permission.

| REV NO | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |

DRAWN BY M.P.
DATE 16-03-82
CHECKED BY
APPR. BY

BAYLY ENGINEERING LTD
a member of

TITLE SCHEMATIC DIAGRAM
POWER SUPPLY– D.F.

DWG NO. 734-0643.031 406 CD-B

# Specifications—LN series

**DC Output**

Voltage range shown in tables.

*REGULATED VOLTAGE*

| | |
|---|---|
| regulation, line | 0.1% (0.15% for LN-Z) |
| regulation, load | 0.1% (0.15% for LN-Z) |
| ripple and noise | 1.5 mV RMS, 5 mV pk-pk (5 mV RMS, 15 mV pk-pk for LNS-P-48) with either positive or negative terminal grounded. |
| temperature coefficient | 0.03%/° C |
| remote programming resistance | 200 ohms per volt nominal (LNS models only) |
| remote programming voltage | volt per volt (LNS models only) |

**AC Input**

| | |
|---|---|
| line | 105-127 VAC, 210-254 VAC (by transformer tap change) 47-440 Hz. Consult factory for operation at frequencies other than 57-63 Hz. |
| Efficiency (Typical) | 30%-5 V and 6 V models, 42% 12 V and 15 V models, 49%-20 V, 24 V, and 28 V models, 52% for 48 V model, 42% for LN duals except LND-MPU which are 34%. |

**Ambient Operating Temperature Range**

Continuous duty from 0° to +71° C with corresponding load current ratings for all modes of operation.

**Storage Temperature Range**

—55° C to 85° C.

**Overload Protection**

*ELECTRICAL*

External overload protection, automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

*THERMAL*

Thermostat—automatically reset when overtemperature condition is eliminated

**Overshoot**

No overshoot on turn-on, turn-off or power failure.

**Overvoltage Protection**

Overvoltage protection module crowbars output when trip level is exceeded—standard on all 5 V models and both outputs of models LND-X-MPU and LND-P-MPU

**Input and Output Connections**

Heavy-duty screw terminals on printed circuit board.

**DC Output Controls**

Simple screwdriver adjustment over the entire voltage range.

**Tracking Accuracy (Dual Tracking Models Only)**

**3% absolute voltage difference, 0.2% change for all conditions of line, load and temperature.**

**Remote Sensing**

**Provision is made for remote sensing to eliminate effect of power output lead resistance on DC regulation.**

**Mounting**

**Three Mounting surfaces, three mounting positions. One mounting position for LN-P models.**

**Convection Cooled**

No external heat sinking or forced air required.

**Transformer**

MIL-T-27C, Grade 6; Electrostatic shield; 4000 VAC input/output isolation.

**Isolation Rating**

Minimum, 10 Megohm isolation from DC to ground at 750 VDC.

**Fungus Proof**

No fungi nutrient material used.

**Military Specifications**

The LN series has passed the following tests in accordance with MIL-STD-810C.

1) Low Pressure—Method 500.1, Procedure I.
2) High Temperature—Method 501.1, Procedure I & II.
3) Low Temperature—Method 502.1, Procedure I.
4) Temperature Shock—Method 503.1, Procedure I.
5) Temperature—Altitude—Method 504.1, Procedure I. Class 2 (0° C operating)
6) Humidity—Method 507.1, Procedure I & II.
7) Fungus—Method 508.1, Procedure I.
8) Vibration—Method 514.2, Procedures X & XI.
9) Shock—Method 516.2, Procedures I & III.

MIL-I-6181D—Conducted and radiated EMI with one output terminal grounded.

**Physical Data**

| Package Model | Weight Lbs. Net | Weight Lbs. Ship | Size Inches |
|---|---|---|---|
| LN-Z | 3 | 3-1/4 | 4-7/8 x 4 x 1-3/4 (w/cover)<br>4-7/8 x 4 x 1-5/8 (w/o cover) |
| LN-Y | 5 | 5-1/2 | 5-5/8 x 4-7/8 x 2-5/8 (w/cover)<br>5-5/8 x 4-7/8 x 2-1/2 (w/o cover) |
| LN-X | 7-3/4 | 8-1/4 | 7 x 4-7/8 x 2-7/8 (w/cover)<br>7 x 4-7/8 x 2-3/4 (w/o cover) |
| LN-W | 9 | 9-1/2 | 9 x 5 x 2-7/8 (w/cover)<br>9 x 4-7/8 x 2-3/4 (w/o cover) |
| LNS-P | 14 | 15-1/2 | 11 x 4-7/8 x 4-13/32 (w & w/o cover) |
| LND-P | 15-1/2 | 17 | 11 x 4-7/8 x 4-13/32 (w & w/o cover) |

**Finish**

Gray, Fed. Std. 595 No. 26081.

**ЯU/CSA**

UL Recognized

CSA Certified

**Accessories**

Overvoltage protectors (standard on 5 V models and models LND-X-MPU and LND-P-MPU). See page 62.

| POWER SUPPLY SERIES | OV SERIES |
|---|---|
| LNS-Z | L-6-OV |
| LNS-Y | L-6-OV |
| LNS-X | L-12-OV |
| LNS-W | L-20-OV |
| LNS-P | L-35-OV for 5 & 6V Models<br>L-20-OV for others |
| LND (All Series) | L-12-OV |

**Guaranteed for 5 Years**

**5-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.**

# Specifications — LZ series

**Regulation**
0.15% — line or load, models LZS-10, LZS-30, LZD-21 have load regulation of 0.15% + 5 mV

**Ripple and Noise**
1.5 mV RMS, 5 mV, pk-pk.

**Temperature Coefficient**
0.03%/° C.

***OVERSHOOT***
No overshoot on turn-on, turn-off, or power failure

**Tracking Accuracy**
2% absolute voltage difference for dual output models only. 0.2% change for all conditions of line, load and temperature.

**Ambient Operating Temperature Range**
Continuous duty from 0° C to + 50° C.

**Wide AC Input Voltage Range**
105 to 132 VAC, 57-63 Hz.

**Storage Temperature Range**
25° C to + 85° C.

**Overload Protection**
Fixed automatic electronic current limiting circuit limits the output current upon external overloads, including short circuit, thereby providing protection for load as well as power supply.

**Options**

**AC Input**

| Add Suffix | For Operation At: |
|---|---|
| —V | 187-242 VAC, 47-63 Hz |

**Price Adder for 'V' option which is available for these models only**

| | |
|---|---|
| $ 5 | LZS-10, LZD-23. |
| $10 | LZS-30, LZS-33,<br>LZD-32, LZD-35 |

Derate current 10%.

**Input & Output Connections**
Printed circuit solder pins on lower surface of unit

**Controls**
Screwdriver voltage adjustment over entire voltage range.

**Mounting**
Two 4 x 40 tapped holes on lower surface of LZ-10 series three 4 x 40 tapped holes on lower surface LZ-20 and LZ-30 series. (Outline drawings see page 107.)

**Physical Data**

| Model | Weight (oz.) net | Weight (oz.) ship | Size (inches) |
|---|---|---|---|
| LZ-10 | 10 | 18 | 2-1/2 x 3-1/2 x 7/8 |
| LZ-20 | 17 | 25 | 2-1/2 x 3-1/2 x 1-1/4 |
| LZ-30 | 24 | 32 | 2-1/2 x 3-1/2 x 1-7/8 |

**90-day Guarantee**
90-day guarantee includes labor as well as parts.

**Accessories**
See pages 62-64 for overvoltage protectors.

# Selector Guide

**DUAL TRACKING OUTPUTS**

| MODEL | MAX. CURRENT (mA) AT 50° C | PKG. SIZE |
|---|---|---|
| **±5 VOLTS ADJ.[1]** | | |
| LZD-21 | 300 | 20 |
| **±6 VOLTS ADJ.[1]** | | |
| LZD-21 | 300 | 20 |
| **±10 VOLTS ADJ.[1]** | | |
| LZD-22 | 61 | 20 |
| LZD-23 | 114 | 20 |
| LZD-32 | 163 | 30 |
| LZD-35 | 200 | 30 |
| **±12 VOLTS ADJ.[1]** | | |
| LZD-22 | 73 | 20 |
| LZD-23 | 129 | 20 |
| LZD-32 | 186 | 30 |
| LZD-35 | 240 | 30 |
| **±15 VOLTS ADJ.[1]** | | |
| LZD-22 | 90 | 20 |
| LZD-23 | 150 | 20 |
| LZD-32 | 220 | 30 |
| LZD-35 | 300 | 30 |

**SINGLE OUTPUT**

| MODEL | MAX. CURRENT (mA) AT 50° C | PKG. SIZE |
|---|---|---|
| **5 VOLTS ADJ.[1]** | | |
| LZS-10 | 450 | 10 |
| LZS-30 | 900 | 30 |
| **6 VOLTS ADJ.[1]** | | |
| LZS-10 | 450 | 10 |
| LZS-30 | 900 | 30 |
| **10 VOLTS ADJ.[1]** | | |
| LZS-11 | 225 | 10 |
| LZS-33 | 293 | 30 |
| LZD-21[2] | 300 | 20 |
| **12 VOLTS ADJ.[1]** | | |
| LZS-11 | 195 | 10 |
| LZD-21[2] | 300 | 20 |
| LZS-33 | 336 | 30 |
| **15 VOLTS ADJ.[1]** | | |
| LZS-11 | 150 | 10 |
| LZS-33 | 400 | 30 |
| **20 VOLTS ADJ.[1]** | | |
| LZD-22[2] | 61 | 20 |
| LZD-23[2] | 114 | 20 |
| LZD-32[2] | 163 | 30 |
| **24 VOLTS ADJ.[1]** | | |
| LZD-22[2] | 73 | 20 |
| LZD-23[2] | 129 | 20 |
| LZD-32[2] | 186 | 30 |
| LZD-35[2] | 240 | 30 |
| **28 VOLTS ADJ.[1]** | | |
| LZD-22[2] | 84 | 20 |
| LZD-23[2] | 143 | 20 |
| LZD-32[2] | 208 | 30 |
| LZD-35[2] | 280 | 30 |

NOTES [1] All LZ models are adjustable between the following limits. LZS-10 2.5 to 6 V, LZS-11 8.0 to 15 V, LZS-30 2.5 to 6 V, LZS-33 8.0 to 15 V, LZD-21 ±2.5 to ±6 V, LZD-22 ±8.0 to ±15 V, LZD-23 ±8.0 to ±15 V, LZD-32 ±8.0 to 15 V, LZD-35 ±8.0 to 15 V. Contact factory for current ratings at voltage setting not indicated in above tables

[2] Single output ratings for dual-output models connected in series

|  |  |  | MAX. AMPS AT AMBIENT OF |  |  |  |
|---|---|---|---|---|---|---|
| **MODEL** | **REGULATION (Line Load)** | **RIPPLE (RMS)** | **40°C** | **50°C** | **60°C** | **71°C** |
| LNS-Z-12 | 0.15%, 0.15% | 1.5 mV | 1.7(1.55) | 1.6(1.45) | 1.5(1.4) | 1.3(1.2) |
| LZD-21 | 0.15%, 0.15% | 1.5 mV |  | 300 mA |  |  |

Note: Ratings in parenthesis apply when cover is being used

### 2.6.2 DF System Control Board

The Control board contains a number of circuits having the following functions:

#### System Test

This circuit decodes the four front panel pushbutton switches for the system test function into a SYSTEM TEST ON line which is switched high anytime one of the four buttons is pressed to signify that the system test function is desired. Also, a binary signal is created which signifies which of the four buttons is pressed (00=45°, 01=135°, 10=225°, and 11=315°). These are called the 'position information bits, 0 and 1'. The circuit is made up of 3 sections of U1, one section of U2 and one section of U3.

#### 10 Hz Pulse Generator

All three sections of Triple 3-input NOR Gate U4 are used to form a 10 Hz oscillator with a 1% duty cycle. This oscillator can be used to provide the start pulse for the parallel-to-serial conversion. The first two sections of the IC are the actual oscillator, while the third acts as a buffer and may also be used to disable the oscillator output. A +12V signal applied to the DISABLE input will disable the output. This input may be able to stop the data transmission for any reason, either from a local control, or a remote location. This could be used for maintenance purposes as certain tests might make it necessary to suppress transmission of data.

#### Integration Constant Select

Similar to the SYSTEM TEST function this circuit, consisting of two sections of U5, decodes 4 positions of a front panel mounted rotary switch into a 2-bit binary code: 00=.1 sec., 01=.2 sec., 10=.4 sec., and 11=.8 sec. integration constant.

#### Antenna Scan Frequency

A 3-position front panel mounted rotary switch will determine the output of two sections of buffer U3. The default (centre) position is 'both outputs low'. A setting to 'LOW' will produce an output on the ANT. SCAN f LOW line and a 'HIGH' setting will produce an output on the ANT. SCAN f HIGH line.

## Master/Slave Switch

Closing the switch to ground produces a LOW level on the MASTER/SLAVE output. This signal is used elsewhere in the system to control the white front panel lamp which shows that the panel is in control of the system. Also, the signal is first inverted in one section of U3 and then used to control the transmitting line switch-over relay K1. This control enables the operator to switch from the 'Control' mode to the 'Monitor' mode.

## Display Intensity Control

An oscillator similar to the one used in the 10 Hz pulse generator is used to generate pulses with a variable duty cycle for the control of the intensity of all displays on the front panel. A front panel mounted potentiometer is used to control the duty cycle. The first two sections of U6 form the actual oscillator and the third section acts as a buffer. An inverter (one section of U9) is used to provide an inverted output in addition to the true output from U6, so that either polarity is available for the system.

## Alarm

This is a fairly complex circuit which enables the alarm, either from a remotely or locally initiated alarm circuit.

The alarm is initiated from an input on pin 28a of the rear connector. The signal is passed through an inverter (one section of U8) and thus appears as a low signal on R17 and R18. C14, which is normally charged will slowly discharge through R18 and reach the lower threshold of the second inverter (another section of U2) in about one second. R17 and diode D9 provide a fast charge path for C14. Thus, the alarm condition has to exist for at least one second before the alarm will trip, but the cancellation of the alarm will return C14 to the pre-alarm condition almost instantaneously. Tripping of the alarm can be suppressed by applying a +12V signal to front connector pin #28 (ALARM DISABLE).

The output of the second inverter is used in both sections of the Dual Flip-Flop U11. The first section, together with two sections of U8, resistors R20, R21 and diode D8 forms a 6-7 second timer, which will disable the audible alarm once it has timed out.

The second section of U11 has its Q output taken high when the +12V signal is applied to the SET input. Q will stay High as long as there is an input on the SET input, regardless of the level at the RESET input. Thus, as long as the alarm condition persists, the alarm indication cannot be cancelled by pushing the ALARM RESET button on the front panel.

Two sections of U7 form a low frequency oscillator with the actual values of R22 and R23 controlling the frequency and the ratio of their values setting the duty cycle. The third section of U7 is used as a buffer and enable switch for this oscillator. The output of this oscillator is used to flash the alarm light on the front panel and to interrupt the audible alarm. The audible alarm may also be enabled by the overhead pass output, if a switch is provided that will connect this output (front connector pin #26) to the appropriate input (front connector pin #4).

### Overhead Pass

Two sections of U10 form a low frequency oscillator with the duty cycle set by the ratio of the values of R29 and R30. The third section of U10 is used as a buffer and enable switch. One of the outputs of U10 is taken to pin #26 of the front connector to be used for enabling the audible alarm, and the other is taken to pin #25a of the rear connector to enable the overhead pass indicator elsewhere in the system.

### Remote Power

The output from this circuit may be used, either locally or remotely, to turn the receiver power off.

### Panel Active Indicator

A lamp enable and driver circuit to activate or extinguish the white front panel lamp which shows that the panel is in control of the system.

### Lamp Test

A pushbutton switch on the front panel of the control housing can cause all displays of the control system to be lit regardless of their present status. An inverter (1/6 of U9) provides an active high output (LAMP TEST) while the original line is active low (LAMP TEST).

## Master/Slave Switch

Closing the switch to ground produces a LOW level on the MASTER/SLAVE output. This signal is used elsewhere in the system to control the white front panel lamp which shows that the panel is in control of the system. Also, the signal is first inverted in one section of U3 and then used to control the transmitting line switch-over relay K1. This control enables the operator to switch from the 'Control' mode to the 'Monitor' mode.

## Display Intensity Control

An oscillator similar to the one used in the 10 Hz pulse generator is used to generate pulses with a variable duty cycle for the control of the intensity of all displays on the front panel. A front panel mounted potentiometer is used to control the duty cycle. The first two sections of U6 form the actual oscillator and the third section acts as a buffer. An inverter (one section of U9) is used to provide an inverted output in addition to the true output from U6, so that either polarity is available for the system.

## Alarm

This is a fairly complex circuit which enables the alarm, either from a remotely or locally initiated alarm circuit.

The alarm is initiated from an input on pin 28a of the rear connector. The signal is passed through an inverter (one section of U8) and thus appears as a low signal on R17 and R18. C14, which is normally charged will slowly discharge through R18 and reach the lower threshold of the second inverter (another section of U2) in about one second. R17 and diode D9 provide a fast charge path for C14. Thus, the alarm condition has to exist for at least one second before the alarm will trip, but the cancellation of the alarm will return C14 to the pre-alarm condition almost instantaneously. Tripping of the alarm can be suppressed by applying a +12V signal to front connector pin #28 (ALARM DISABLE).

The output of the second inverter is used in both sections of the Dual Flip-Flop U11. The first section, together with two sections of U8, resistors R20, R21 and diode D8 forms a 6-7 second timer, which will disable the audible alarm once it has timed out.

The second section of U11 has its Q output taken high when the +12V signal is applied to the SET input. Q will stay High as long as there is an input on the SET input, regardless of the level at the RESET input. Thus, as long as the alarm condition persists, the alarm indication cannot be cancelled by pushing the ALARM RESET button on the front panel.

Two sections of U7 form a low frequency oscillator with the actual values of R22 and R23 controlling the frequency and the ratio of their values setting the duty cycle. The third section of U7 is used as a buffer and enable switch for this oscillator. The output of this oscillator is used to flash the alarm light on the front panel and to interrupt the audible alarm. The audible alarm may also be enabled by the overhead pass output, if a switch is provided that will connect this output (front connector pin #26) to the appropriate input (front connector pin #4).

### Overhead Pass

Two sections of U10 form a low frequency oscillator with the duty cycle set by the ratio of the values of R29 and R30. The third section of U10 is used as a buffer and enable switch. One of the outputs of U10 is taken to pin #26 of the front connector to be used for enabling the audible alarm, and the other is taken to pin #25a of the rear connector to enable the overhead pass indicator elsewhere in the system.

### Remote Power

The output from this circuit may be used, either locally or remotely, to turn the receiver power off.

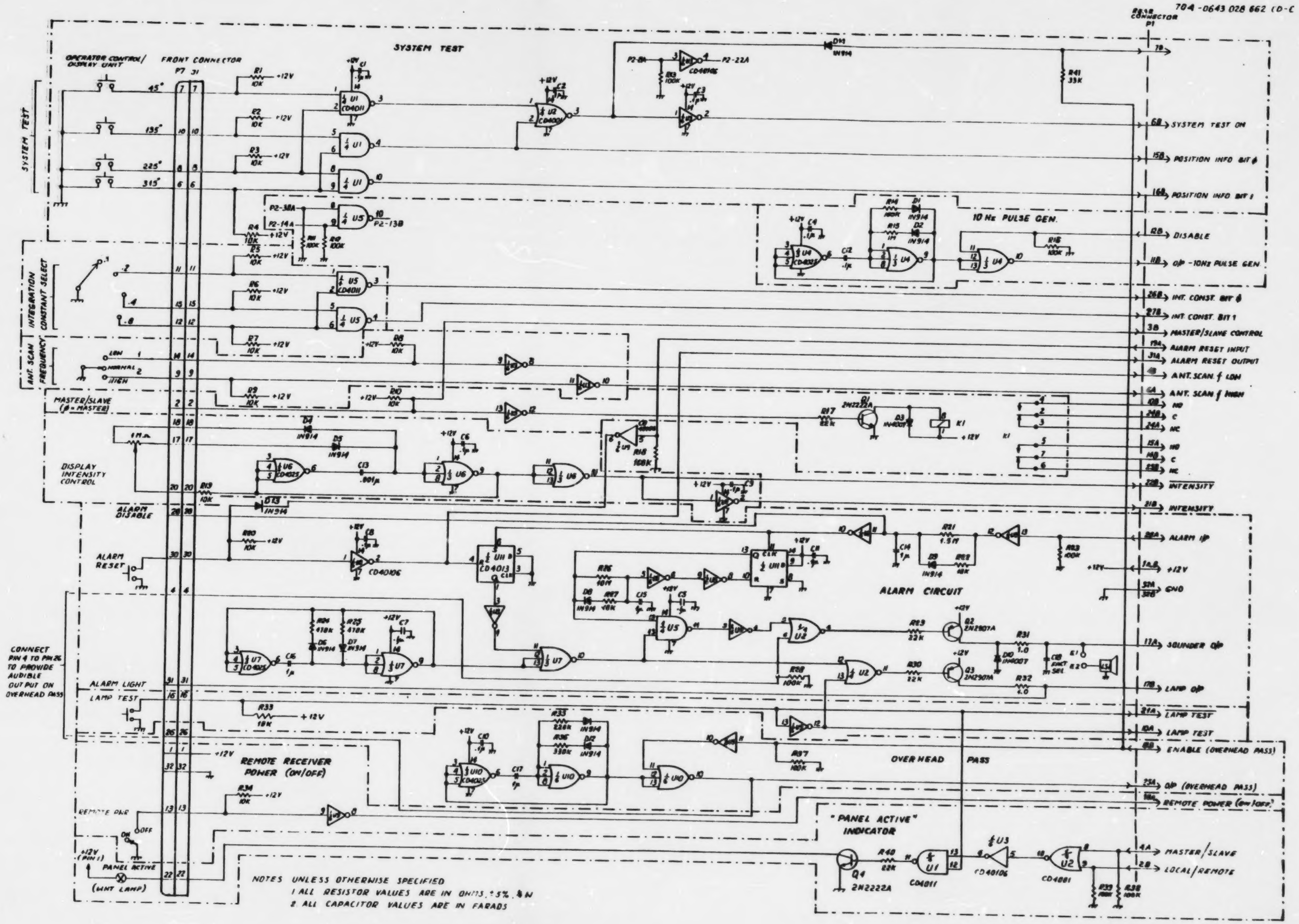
### Panel Active Indicator

A lamp enable and driver circuit to activate or extinguish the white front panel lamp which shows that the panel is in control of the system.

### Lamp Test

A pushbutton switch on the front panel of the control housing can cause all displays of the control system ~~to~~ be lit regardless of their present status. An inverter (1/6 of U9) provides an active high output (LAMP TEST) while the original line is active low (LAMP TEST).

704-0643 028 662 CD-C


SYSTEM TEST
OPERATOR CONTROL/DISPLAY UNIT
FRONT CONNECTOR
P7 J1
REAR CONNECTOR P1
45°
135°
225°
315°
U1 CD4011
U2 CD4001
CD40106
U5 CD4011
P2-8A
P2-22A
P2-38A
P2-14A
P2-13B
DISABLE
SYSTEM TEST ON
POSITION INFO BIT 0
POSITION INFO BIT 1
10 Hz PULSE GEN.
O/P - 10Hz PULSE GEN
INTEGRATION CONSTANT SELECT
INT. CONST. BIT 0
INT. CONST. BIT 1
MASTER/SLAVE CONTROL
ALARM RESET INPUT
ALARM RESET OUTPUT
ANT. SCAN FREQUENCY
LOW
NORMAL
HIGH
ANT. SCAN f LOW
ANT. SCAN f HIGH
MASTER/SLAVE (0 = MASTER)
DISPLAY INTENSITY CONTROL
INTENSITY
Q1 2N2222A
K1
NO
C
NC
ALARM DISABLE
ALARM RESET
ALARM I/P
+12V
GND
ALARM CIRCUIT
CD4013
Q2 2N2907A
Q3 2N2907A
SOUNDER O/P
LAMP O/P
CONNECT PIN 4 TO PIN 26 TO PROVIDE AUDIBLE OUTPUT ON OVERHEAD PASS
ALARM LIGHT
LAMP TEST
OVERHEAD PASS
ENABLE (OVERHEAD PASS)
O/P (OVERHEAD PASS)
REMOTE RECEIVER POWER (ON/OFF)
REMOTE POWER (ON/OFF)
REMOTE PWR
ON
OFF
+12V (PIN 1)
PANEL ACTIVE
(WNT LAMP)
"PANEL ACTIVE" INDICATOR
Q4 2N2222A
CD4011
CD40106
CD4081
MASTER/SLAVE
LOCAL/REMOTE

NOTES UNLESS OTHERWISE SPECIFIED
1 ALL RESISTOR VALUES ARE IN OHMS ±5% ¼W
2 ALL CAPACITOR VALUES ARE IN FARADS

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV NO | REVISION | DATE | APPD BY |
|---|---|---|---|
| 01 | RELEASED | | |

DRAWN BY A SMITH | DATE APR 6.81 | CHK'D BY

BAYLY ENGINEERING LTD a member of

TITLE SCHEMATIC DIAGRAM
DF SYSTEM CONTROL BOARD

DWG NO 704-0643. 028 662.CD-C 01

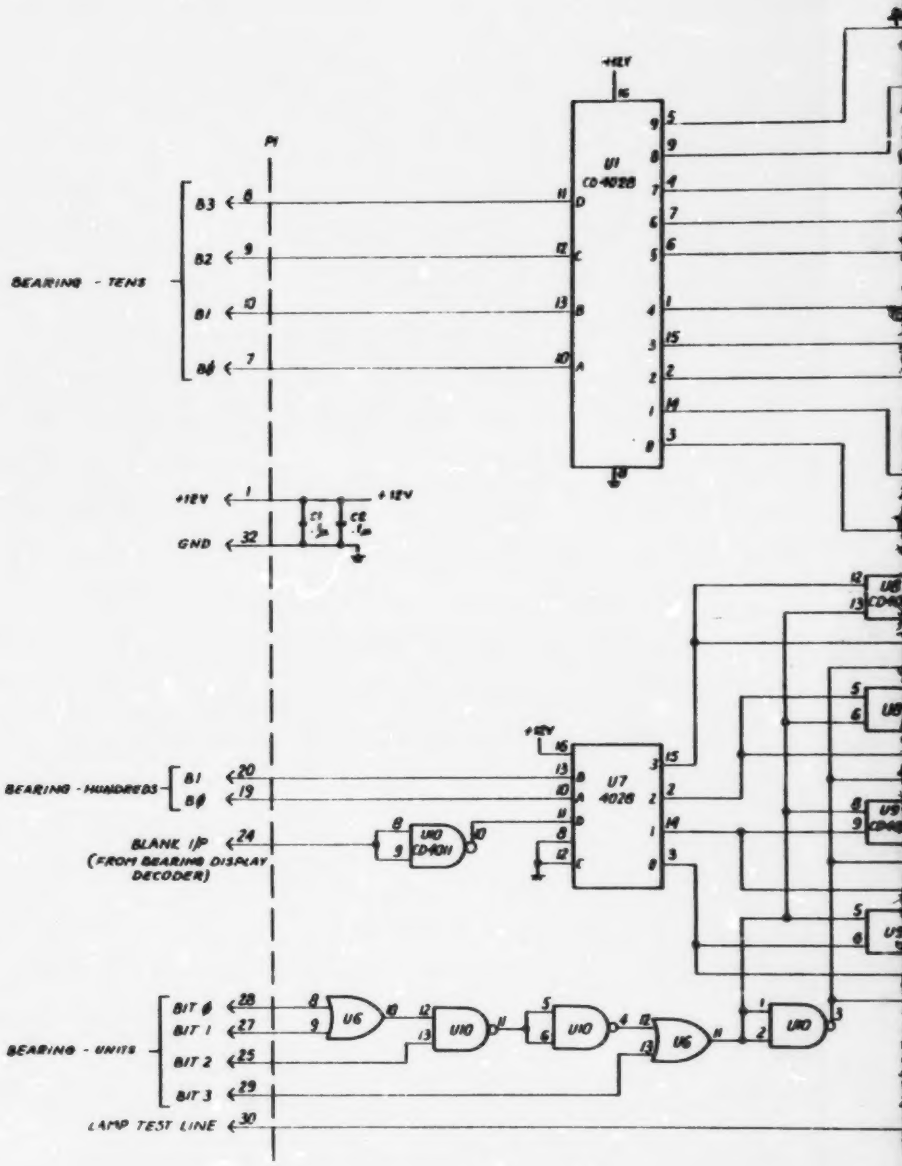
## 2.6.3 Circular Bearing Display Decoder

The 'Circular Bearing Display Decoder' is located in the Operator's Control/Display Unit of the Doppler Radio Direction Finder and is used as the driver for the 'Circular Bearing Display'.

It consists of two BCD to decimal decoders, a combination of gates, and eighteen driver transistors.

Two BCD to decimal decoders (U1 and U7) are used to decode the tens and hundreds digits, while a combination of gates are used to decode the units digit. Ten driver transistors (Q1 to Q10) apply a positive voltage to all LED's which have the same tens digit (e.g. 10, 110, 210 and 310). The 'hundreds' decoder outputs are further split using AND gates and the proper transistor (Q11 to Q18) is selected on the basis of the hundreds output (U6) and the output of the units decoder. This will apply a ground to the cathode of the appropriate LED.

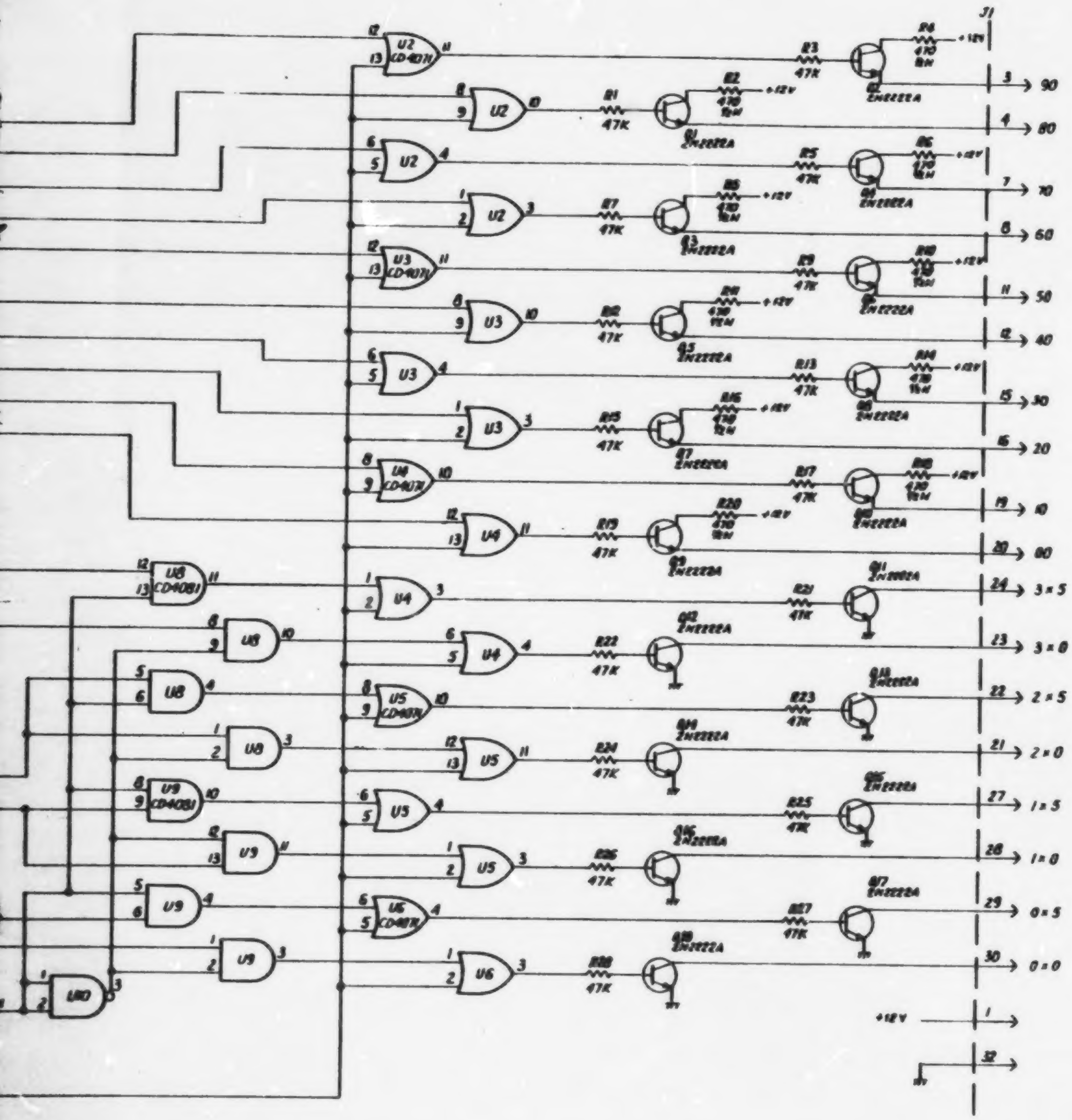
Intensity modulation is achieved by inverting the system intensity control line and using this signal to modulate the 'D' input of the hundreds BCD decoder. This will cause the selected LED cathode to be turned on and off with a duty cycle set by the intensity control.


P1
BEARING - TENS
B3 8
B2 9
B1 10
B0 7
+12V
16
U1
CD4028
11 D
12 C
13 B
10 A
9 5
8 9
7 4
6 7
5 6
4 1
3 15
2 2
1 14
0 3
8
+12V 1
GND 32
C1 .1µ
C2 .1µ
+12V
U8
CD40
12
13
5
6
U8
U9
CD40
8
9
5
6
U9
+12V
16
BEARING - HUNDREDS
B1 20
B0 19
BLANK I/P (FROM BEARING DISPLAY DECODER) 24
U10 CD4011
8
9
10
U7 4028
13 B
10 A
11 D
8
12 C
3 15
2 2
1 14
0 3
BEARING - UNITS
BIT 0 28
BIT 1 27
BIT 2 25
BIT 3 29
LAMP TEST LINE 30
U6
8
9
10
U10
12
13
11
U10
5
6
4
U6
12
13
11
U10
1
2
3

NOTES: 1 UNLESS OTHER

a) ALL RESISTOR

b) ALL CAPACITO


J1
U2 CD4071
U3 CD4071
U4 CD4071
U5 CD4071
U6 CD4071
U8 CD4081
U9 CD4081
U10
R1 47K
R3 47K
R2 470 ½W
R4 470 ½W
Q1 2N2222A
Q2 2N2222A
+12V
3 → 90
4 → 80
7 → 70
8 → 60
11 → 50
12 → 40
15 → 30
16 → 20
19 → 10
20 → 00
24 → 3×5
23 → 3×0
22 → 2×5
21 → 2×0
27 → 1×5
28 → 1×0
29 → 0×5
30 → 0×0
+12V → 1
32

: 1 UNLESS OTHERWISE SPECIFIED
a) ALL RESISTOR VALUES ARE IN OHMS
b) ALL CAPACITOR VALUES ARE IN FARADS

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV NO | REVISION | DATE | APPD BY |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 23-06-80 | |

DRAWN A SMITH DATE DEC 10.80 CHECKED

BAYLY ENGINEERING LTD a member of

TITLE SCHEMATIC DIAGRAM
CIRCULAR DISPLAY DECODER

DWG NO 67-0643.027 236.CD-C 01

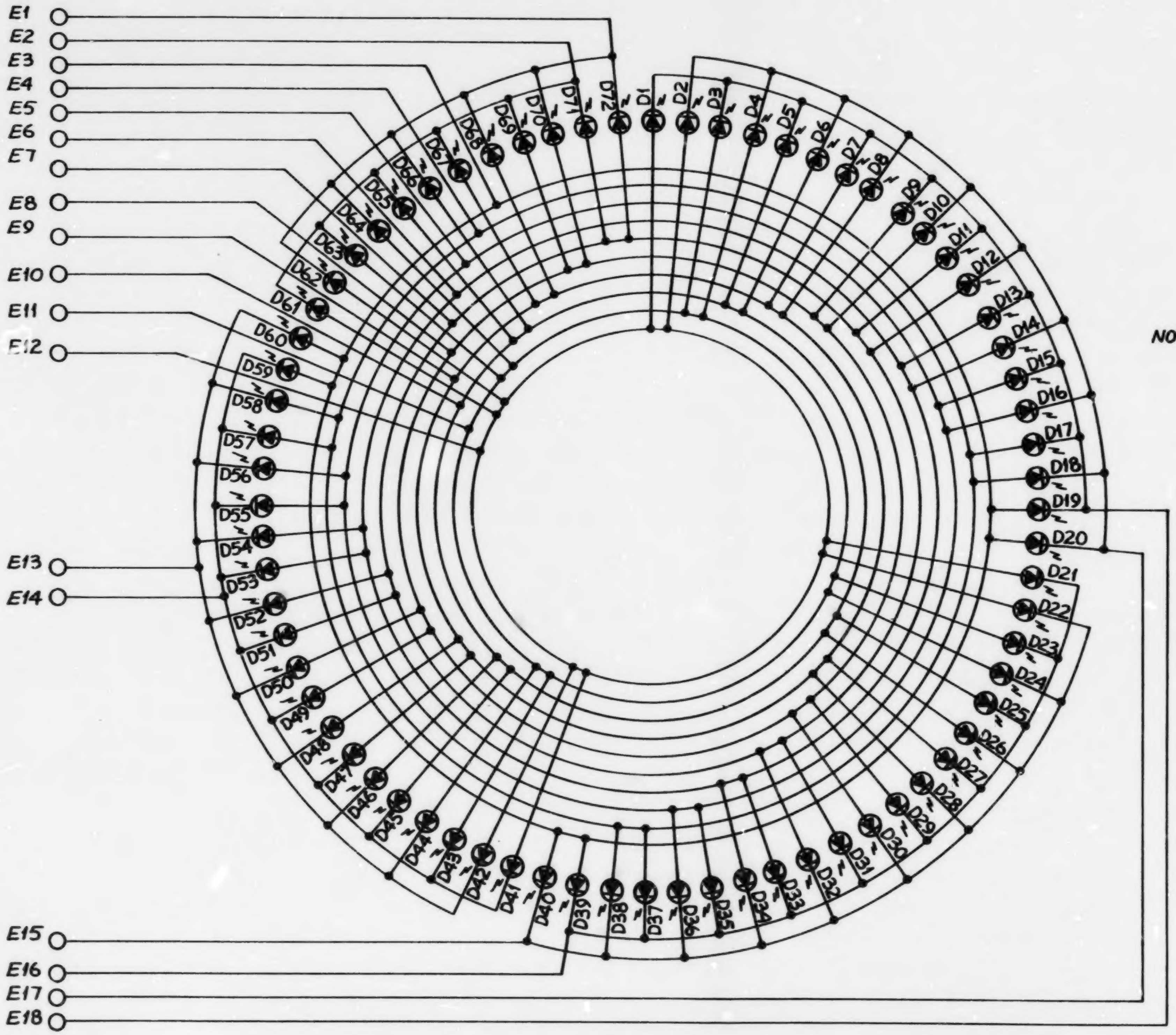
### 2.6.4 Circular Bearing Display

The 'Circular Bearing Display' (CBD) is located in the Operator's CDU of the Doppler Radio Direction Finder, and provides an indication of the relative position of the plane.

The 'CBD' uses 72 individual LED's with the associated decoding circuitry (Circular Bearing Display Decoder). To keep decoding circuitry simple, '0' LED means an actual value between 0° and 4°, while a '5' LED lights when the reading is between 5° and 9°. This would be repeated for every decade (i.e. 0, 5, 10, 15, etc. to 355).

The matrix approach is adopted with common lines for the 'tens' and 'hundreds'. The line for the units is decoded to decide if the units digit is less than or equal to 5, or more than 5.

66-0643.028 230. CD-B


E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
D42
D43
D44
D45
D46
D47
D48
D49
D50
D51
D52
D53
D54
D55
D56
D57
D58
D59
D60
D61
D62
D63
D64
D65
D66
D67
D68
D69
D70
D71
D72

NOTE: UNLESS OTHERWISE SPECIFIED:

1. ALL DIODES ARE HLMP-1301.

This drawing is the property of BAYLY ENGINEERING LIMITED and may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others without written permission.

| REV NO. | REVISION | DATE | APPR. BY |
|---|---|---|---|
| 01 | RELEASED | JAN.11/82 | |

DRAWN BY KP
DATE APR.1/81
CHECKED BY RG

BAYLY ENGINEERING LTD
a member of

TITLE SCHEMATIC
CIRCULAR DISPLAY

DWG NO. 66-0643.028 230.CD-B
01

## 2.6.5 Frequency Decoder

The function of the frequency decoder board is to decode and store the six digits sent to set the receiver frequency. The main inputs are the four binary lines which carry the code for the digit currently being received (pin #7b, 7a, 6a, and 6b for bits 0 to 3 respectively) and the KEY PRESSED line (pin #21b).

This circuit is designed to work either by itself, or in conjunction with the channel decoder board. The main difference in operation is the input marked 'A', (pin #20a). In the stand-alone operation, this pin would be held high by R5 and the Flip-Flop (one section of U13) would react to the first digit received. With the channel decoder board installed, this input would be kept low until the channel decoder receives the 'frequency selection' code, at which time input 'A' is taken high and remains there until all six digits have been entered.

The flip-flop has two functions:

(a) the Q output provides the strobe which loads the digit code into the proper latch (U1 to U6), and

(b) the $\overline{Q}$ output goes to a second Flip-Flop (the other section of U13) which provides the pulse to advance digit counter U19 after the previous digit has been stored in the appropriate latch.

The BCD value of the received digit is applied to the inputs of all six latches. However, the latching input is controlled by the output of the digit counter (U19) and the KEY PRESSED signal as shaped by the initial Flip-Flop (½ of U13). Six AND Gates (U18 and two sections of U17) combine these signals to select the proper latch. Once the BCD code is stored in the latch, it appears at its output terminals.

After all six required digits have been entered, the digit counter U19 advances to its #7 output (pin #6) which initiates two functions:

(a) it sends a signal out on connector pin #21a which is used to tell the SYNTHESIZER PROGRAM card that the frequency selection is complete, and

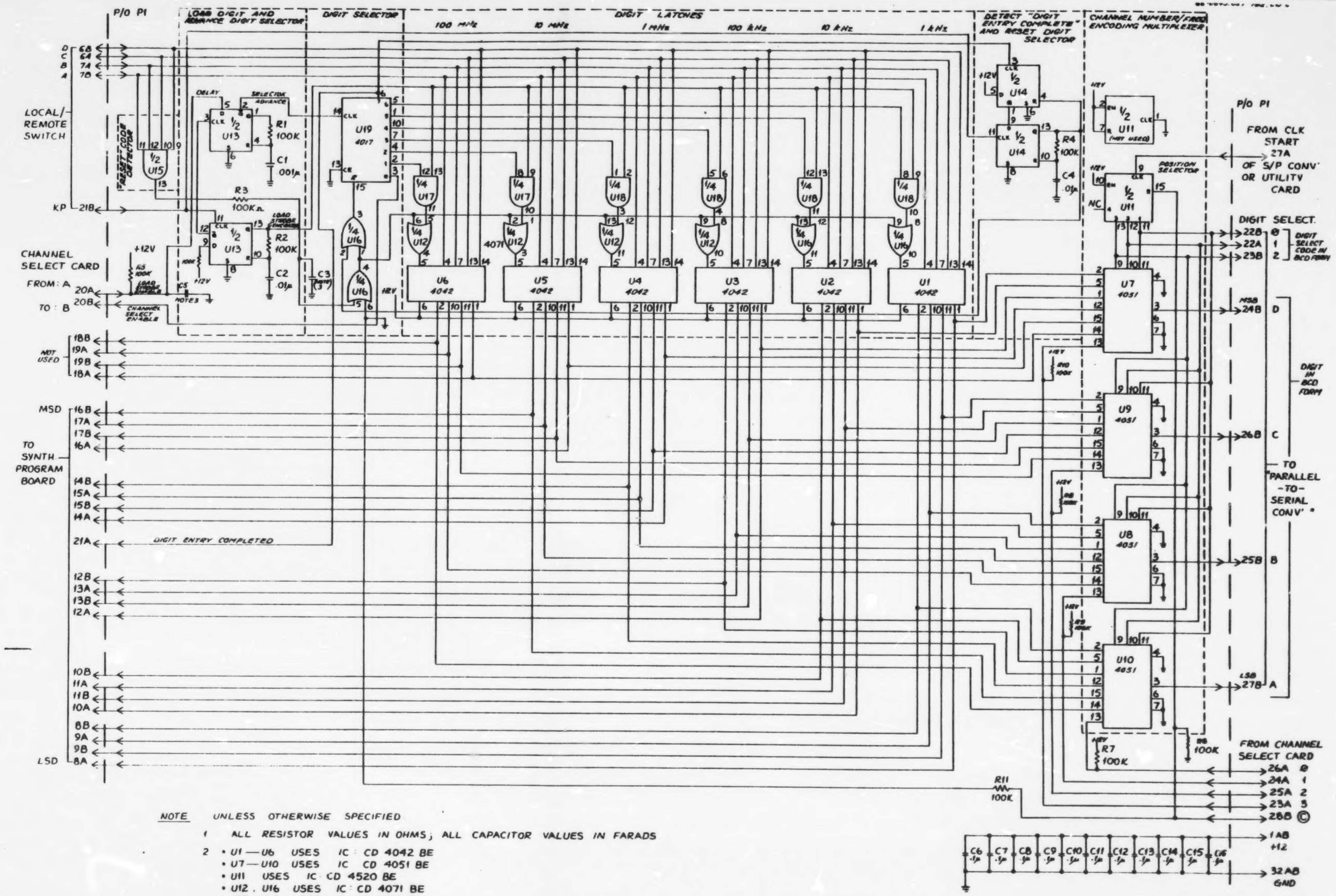
(b) it acts as a clock pulse to set the first Flip-Flop in U14, so that the next positive-going KEY PRESSED strobe will initialize the decoder.

This provides the DATA input for the second Flip-Flop in U14, so that the next positive-going KEY PRESSED strobe will initialize the decoder. The pulse generated in the second section of U14 is fed back to the reset input of digit counter U19 via an OR gate (one section of U16) and returns the counter to the 0 position. If the channel decoder card is in the system, it will now be enabled again and the frequency decoder would be disabled until the next 'frequency select' code is received.

A 4-input AND gate (½ of U15) monitors the BCD input lines to check for a 'reset' code (1111). An output from this gate will reset the digit counter U19 and store this code in the six latches. Since the code has no meaning, it will be ignored by the synthesizer program card and will also cause all frequency displays to blank.

The remaining circuitry (U7 to U11) has nothing to do with the frequency selection itself, but is used instead for the acknowledgement of the digits already entered. U7 to U10 are multiplexers which perform the scanning of the channel number and the six frequency digits. One multiplexer is used for each of the four bits in the BCD code. A binary counter, U11, controls the scanning and is, in turn, controlled by the same clock pulses which start the serial data transmission. Thus each 32 bit transmission package contains either the BCD code for the channel number, or for one of the six frequency digits. Input 'C' (connector pin #28b), coming from the channel decoder, can reset and inhibit the counter and multiplexer scanning so that in the 'channel select' mode, no scanning takes place, and the channel number is sent out in every transmitted data stream. If the CHANNEL DECODER card is not used, R6 will keep the reset input low and scanning would always occur. The same line is also used to reset the digit counter U13, to ensure that it always starts from its initial position and the latches are also cleared by a high signal on this input.

Resistors R7 to R10 keep the '0' position inputs of the multiplexers high if no channel decoder card is in the system, so that a meaningless code is sent and no channel light is activated.


P/O P1
LOAD DIGIT AND ADVANCE DIGIT SELECTOR
DIGIT SELECTOR
DIGIT LATCHES
100 MHz
10 MHz
1 MHz
100 kHz
10 kHz
1 kHz
DETECT "DIGIT ENTRY COMPLETE" AND RESET DIGIT SELECTOR
CHANNEL NUMBER/FREQ ENCODING MULTIPLEXER
D 6B
C 6A
B 7A
A 7B
LOCAL/-REMOTE SWITCH
"RESET CODE" DETECTOR
1/2 U15
DELAY
SELECTOR ADVANCE
1/2 U13
R1 100K
C1 .001µ
R3 100KΩ
LOAD STROBE GENERATOR
R2 100K
C2 .01µ
C3 (3)
U19 4017
1/4 U16
1/4 U17
1/4 U18
1/4 U12
U6 4042
U5 4042
U4 4042
U3 4042
U2 4042
U1 4042
1/2 U14
R4 100K
C4 .01µ
1/2 U11 (NOT USED)
POSITION SELECTOR
U7 4051
U9 4051
U8 4051
U10 4051
KP 21B
CHANNEL SELECT CARD
FROM: A 20A
TO: B 20B
LOAD STROBE ENABLE
CHANNEL SELECT ENABLE
NOT USED 18B 19A 19B 18A
MSD 16B 17A 17B 16A
TO SYNTH PROGRAM BOARD
14B 15A 15B 14A
21A DIGIT ENTRY COMPLETED
12B 13A 13B 12A
10B 11A 11B 10A
8B 9A 9B
LSD 8A
P/O P1
FROM CLK START 27A OF S/P CONV' OR UTILITY CARD
DIGIT SELECT.
22B 0
22A 1
23B 2
DIGIT SELECT CODE IN BCD FORM
MSB 24B D
26B C
25B B
LSB 27B A
DIGIT IN BCD FORM
TO "PARALLEL -TO- SERIAL CONV'"
R7 100K
R8 100K
R11 100K
FROM CHANNEL SELECT CARD
26A 0
24A 1
25A 2
23A 3
28B ©
1AB +12
32AB GND
C6 .1µ
C7 .1µ
C8 .1µ
C9 .1µ
C10 .1µ
C11 .1µ
C12 .1µ
C13 .1µ
C14 .1µ
C15 .1µ
C16 .1µ
+12V

NOTE UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES IN OHMS; ALL CAPACITOR VALUES IN FARADS
2. 
   - U1 — U6 USES IC: CD 4042 BE
   - U7 — U10 USES IC: CD 4051 BE
   - U11 USES IC: CD 4520 BE
   - U12, U16 USES IC: CD 4071 BE
   - U13, U14 USES IC: CD 4013 BE
   - U15 USES IC: CD 4082 BE
   - U17, U18 USES IC: CD 4081 BE
   - U19 USES IC: CD 4017 BE
3. VALUE TO BE DETERMINED ON TEST.

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV NO | REVISION | DATE | APPD BY |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 83·02·03 | |
| — | RELEASED | 88·01·13 | I.C. |

DRAWN BY KP DATE MAY 5/81 CHECKED BY

BAYLY ENGINEERING LTD a member of

TITLE SCHEMATIC FREQUENCY DECODER

DWG NO. 66-0643 027 782 CD-C 01

### 2.6.6 Channel Decoder

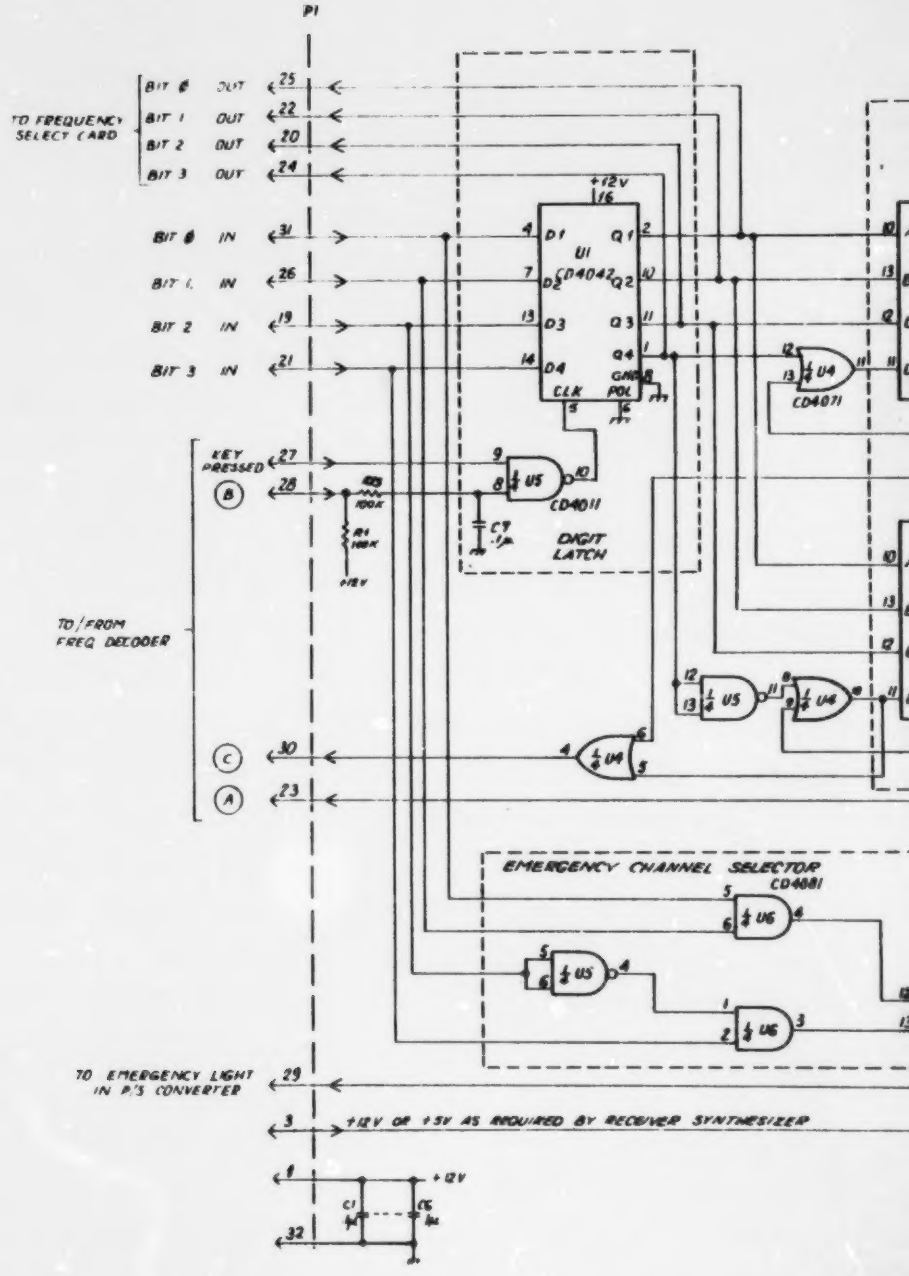
The channel decoder card will decode a channel number, originating either from a remote control, or from a local keyboard encoder and turn the single digit channel number into the 10-bit code required by the synthesizer.

The circuit requires the 4-bit binary code which signifies the channel number. This code enters the board on pin #31, 26, 19 and 21 for bits 0 to 3 respectively. In addition, the 'key pressed' signal is brought in on pin #27. These five signals are fed to U1, a Quad Latch, where the 4 bits are stored when the key is released. The stored code is brought out again on pin #25, 22, 20 and 24 respectively, for transmission back to the channel display. The stored codes are also fed to the inputs of U2 and U3, two BCD-to-Decimal decoders where the proper channel is selected. Bit 3 determines which of the two is enabled. U2 decodes channels 0 to 7 and U3 decodes channels 8 and 9. In addition, U3 also decodes the binary code for 'frequency' selection which initiates the operation of the FREQUENCY DECODER board.

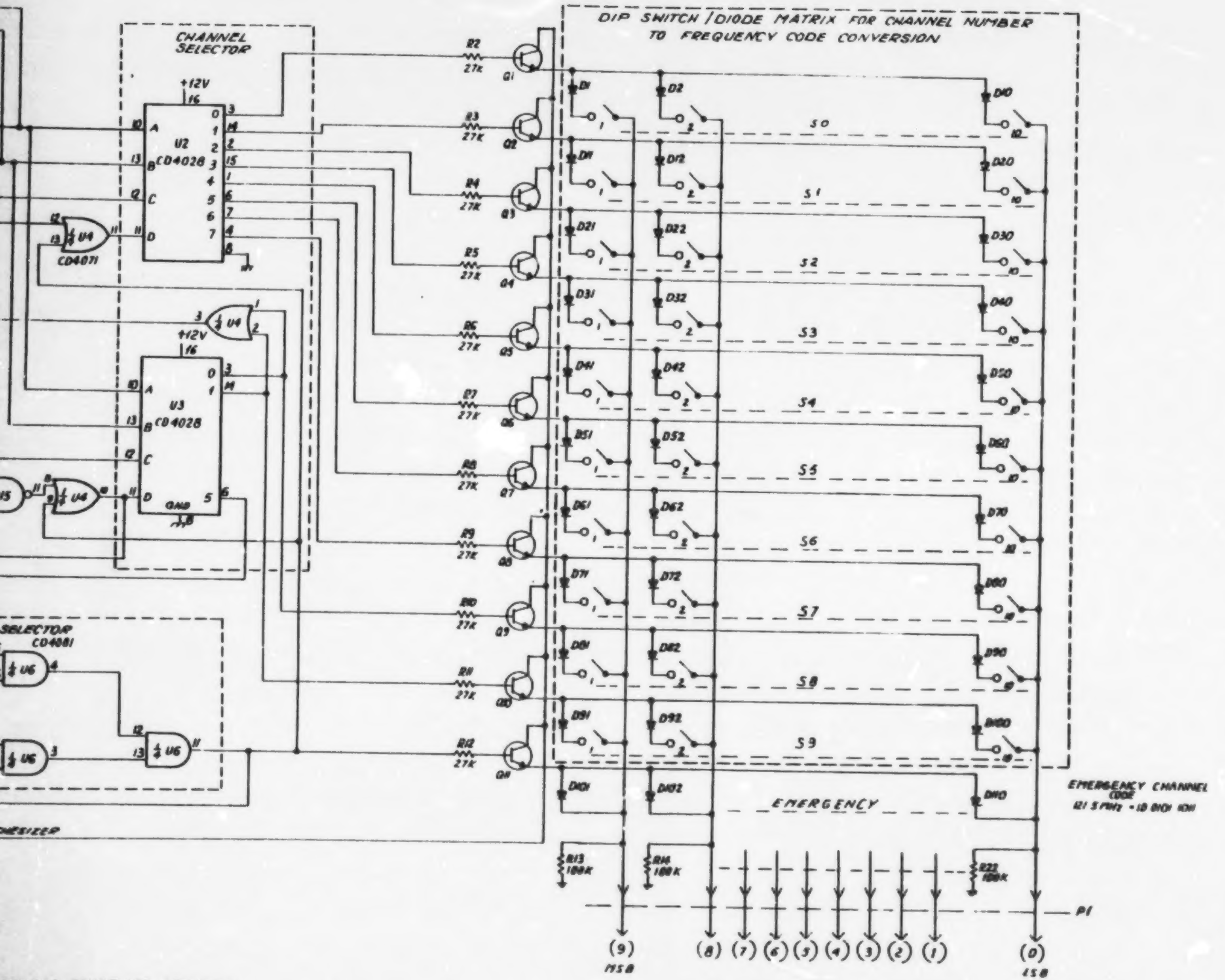
A separate decoder, consisting of one section of U5 and three sections of U6, detects the reception of the special Emergency Channel Select code which immediately tunes the receiver to the emergency channel (121.500 MHz). No KEY PRESSED input is required for this decoder, and it will override any other frequency or channel which may be selected as long as the Emergency Select Code is present.

The code generation for the 10 pre-selected channels is done by 10 ten-pole DIP switches which, together with diodes, are wired into a matrix to produce the code required by the receiver synthesizer (see Table 2.6.5). The code for the emergency frequency is also generated by this matrix. However, no DIP switch is used since this frequency is always the same and, thus, the code is hard-wired into the matrix.

The circuit was originally designed for stand-alone operation since the initial specifications did not require a 'frequency mode'. However, later the 'frequency selection' option was added and the circuit was re-designed to operate by itself, or in conjunction with the FREQUENCY DECODER board. Input 'B' (pin #28) is designed to disable the input latch (U1) when the system is in the 'frequency mode'. Output 'A' (pin #23) selects the 'frequency mode' by enabling the FREQUENCY DECODER card, while output 'C' (pin #30) disables the FREQUENCY DECODER when the system is in the 'channel select' mode.


P1
TO FREQUENCY SELECT CARD
BIT 0 OUT 25
BIT 1 OUT 22
BIT 2 OUT 20
BIT 3 OUT 24
BIT 0 IN 31
BIT 1 IN 26
BIT 2 IN 19
BIT 3 IN 21
+12V
16
U1
CD4042
D1 D2 D3 D4
Q1 Q2 Q3 Q4
CLK
GND
POL
KEY PRESSED 27
B 28
R3 100K
R4 100K
+12V
C7 .1µ
1/4 U5
CD4011
DIGIT LATCH
1/4 U4
CD4071
TO/FROM FREQ DECODER
C 30
A 23
1/4 U5
1/4 U4
1/4 U4
EMERGENCY CHANNEL SELECTOR
CD4081
1/4 U6
1/4 U5
1/4 U6
TO EMERGENCY LIGHT IN P/S CONVERTER 29
3 +12V OR +5V AS REQUIRED BY RECEIVER SYNTHESIZER
1
+12V
C1 1µ
C6 1µ
32

NOTES · UNLESS OTHERWIS
1. ALL RESISTOR V
2. ALL CAPACITOR
3. ALL DIODES ARE
4. ALL TRANSISTO


DIP SWITCH / DIODE MATRIX FOR CHANNEL NUMBER TO FREQUENCY CODE CONVERSION
CHANNEL SELECTOR
+12V
U2
CD4028
U3
CD4028
1/4 U4
CD4071
GND
SELECTOR
CD4081
1/4 U6
U5
HESIZER
R2 27K
R3 27K
R4 27K
R5 27K
R6 27K
R7 27K
R8 27K
R9 27K
R10 27K
R11 27K
R12 27K
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
D1
D2
D10
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
EMERGENCY
D101
D102
D110
R13 100K
R14 100K
R22 100K
P1
(9)
MSB
(8)
(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
LSB
EMERGENCY CHANNEL CODE
121.5 MHz = 10 0101 1011

BINARY CODES USED BY SYNTHESIZER
FOR FREQUENCY SELECTION

UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS ¼W ±5%
2 ALL CAPACITOR VALUES ARE IN FARADS
3. ALL DIODES ARE IN914
4. ALL TRANSISTORS ARE 2N2222A

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| | | | |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 23 02 83 | |
| 02 | REVISED | 16-11-81 | |
| NO. | REVISION | DATE | APPD BY |

DRAWN BY A SMITH DATE FEB 9.81

BAYLY ENGINEERING LTD a member of

SCHEMATIC DIAGRAM
CHANNEL DECODER

DWG NO 66-0643.027 864.CD-C 01

## TABLE 2.6.5

## FREQUENCY CORRESPONDING TO DIP SWITCH SETTING

**1 = Switch Closed**
**0 = Switch Open**

| FREQUENCY (MHz) | DIP SWITCH CODES 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| 117.400 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 117.425 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 117.450 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 117.475 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 117.500 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 117.525 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 117.550 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 117.575 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 117.600 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 117.625 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 117.650 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 117.675 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 117.700 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 117.725 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 117.750 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 117.775 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 117.800 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 117.825 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 117.850 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 117.875 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 117.900 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 117.925 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 117.950 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 117.975 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 118.000 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 118.025 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 118.050 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 118.075 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 118.100 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 118.125 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 118.150 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 118.175 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 118.200 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 118.225 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 118.250 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 118.275 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 118.300 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 118.325 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 118.350 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 118.375 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 118.400 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 118.425 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 118.450 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

```
118.475          1   0   1   1   0   1   0   1   0   0
118.500          1   0   1   1   0   1   0   0   1   1
118.525          1   0   1   1   0   1   0   0   1   0
118.550          1   0   1   1   0   1   0   0   0   1
118.575          1   0   1   1   0   1   0   0   0   0
118.600          1   0   1   1   0   0   1   1   1   1
118.625          1   0   1   1   0   0   1   1   1   0
118.650          1   0   1   1   0   0   1   1   0   1
118.675          1   0   1   1   0   0   1   1   0   0
118.700          1   0   1   1   0   0   1   0   1   1
118.725          1   0   1   1   0   0   1   0   1   0
118.750          1   0   1   1   0   0   1   0   0   1
118.775          1   0   1   1   0   0   1   0   0   0
118.800          1   0   1   1   0   0   0   1   1   1
118.825          1   0   1   1   0   0   0   1   1   0
118.850          1   0   1   1   0   0   0   1   0   1
118.875          1   0   1   1   0   0   0   1   0   0
118.900          1   0   1   1   0   0   0   0   1   1
118.925          1   0   1   1   0   0   0   0   1   0
118.950          1   0   1   1   0   0   0   0   0   1
118.975          1   0   1   1   0   0   0   0   0   0
119.000          1   0   1   0   1   1   1   1   1   1
119.025          1   0   1   0   1   1   1   1   1   0
119.050          1   0   1   0   1   1   1   1   0   1
119.075          1   0   1   0   1   1   1   1   0   0
119.100          1   0   1   0   1   1   1   0   1   1
119.125          1   0   1   0   1   1   1   0   1   0
119.150          1   0   1   0   1   1   1   0   0   1
119.175          1   0   1   0   1   1   1   0   0   0
119.200          1   0   1   0   1   1   0   1   1   1
119.225          1   0   1   0   1   1   0   1   1   0
119.250          1   0   1   0   1   1   0   1   0   1
119.275          1   0   1   0   1   1   0   1   0   0
119.300          1   0   1   0   1   1   0   0   1   1
119.325          1   0   1   0   1   1   0   0   1   0
119.350          1   0   1   0   1   1   0   0   0   1
119.375          1   0   1   0   1   1   0   0   0   0
119.400          1   0   1   0   1   0   1   1   1   1
119.425          1   0   1   0   1   0   1   1   1   0
119.450          1   0   1   0   1   0   1   1   0   1
119.475          1   0   1   0   1   0   1   1   0   0
119.500          1   0   1   0   1   0   1   0   1   1
119.525          1   0   1   0   1   0   1   0   1   0
119.550          1   0   1   0   1   0   1   0   0   1
119.575          1   0   1   0   1   0   1   0   0   0
119.600          1   0   1   0   1   0   0   1   1   1
119.625          1   0   1   0   1   0   0   1   1   0
119.650          1   0   1   0   1   0   0   1   0   1
119.675          1   0   1   0   1   0   0   1   0   0
119.700          1   0   1   0   1   0   0   0   1   1
119.725          1   0   1   0   1   0   0   0   1   0
119.750          1   0   1   0   1   0   0   0   0   1
119.775          1   0   1   0   1   0   0   0   0   0
119.800          1   0   1   0   0   1   1   1   1   1
119.825          1   0   1   0   0   1   1   1   1   0
119.850          1   0   1   0   0   1   1   1   0   1
119.875          1   0   1   0   0   1   1   1   0   0
119.900          1   0   1   0   0   1   1   0   1   1
```

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 119.925 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 119.950 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 119.975 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 120.000 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 120.025 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 120.050 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 120.075 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 120.100 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 120.125 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 120.150 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 120.175 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 120.200 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 120.225 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 120.250 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 120.275 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 120.300 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 120.325 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 120.350 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | 1 |
| 120.375 | 1 | | 1 | 0 | 0 | 0 | 1 | | | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 120.425 | 1 | 0 | 1 | | 0 | 0 | 0 | 1 | 1 | 0 |
| 120.450 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 120.475 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 120.500 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 120.525 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 120.550 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 120.575 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 120.600 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 120.625 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 120.650 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 120.675 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 120.700 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 120.725 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 120.750 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 120.775 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 120.800 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 120.825 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 120.850 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 120.875 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 120.900 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 120.925 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 120.950 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 120.975 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 121.000 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 121.025 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 121.050 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 121.075 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 121.100 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 121.125 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 121.150 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 121.175 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 121.200 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 121.225 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 121.250 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 121.275 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 121.300 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 121.325 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 121.350 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 121.375 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 121.400 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 121.425 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 121.450 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 121.475 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 121.500 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 121.525 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 121.550 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 121.575 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 121.600 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 121.625 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 121.650 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 121.675 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 121.700 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 121.725 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 121.750 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 121.775 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 121.800 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 121.825 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 121.850 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 121.875 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 121.900 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 121.925 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 121.950 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 121.975 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 122.000 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 122.025 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 122.050 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 122.075 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 122.100 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 122.125 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 122.150 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 122.175 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 122.200 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 122.225 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 122.250 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 122.275 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 122.300 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 122.325 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 122.350 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 122.375 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 122.400 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 122.425 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 122.450 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 122.475 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 122.500 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 122.525 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 122.550 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 122.575 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 122.600 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 122.625 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 122.650 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 122.675 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 122.700 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 122.725 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 122.750 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 122.775 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 122.800 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |

```
122.825         1  0  0  0  1  0  0  1  1  0
122.850         1  0  0  0  1  0  0  1  0  1
122.875         1  0  0  0  1  0  0  1  0  0
122.900         1  0  0  0  1  0  0  0  1  1
122.925         1  0  0  0  1  0  0  0  1  0
122.950         1  0  0  0  1  0  0  0  0  1
122.975         1  0  0  0  1  0  0  0  0  0
123.000         1  0  0  0  0  1  1  1  1  1
123.025         1  0  0  0  0  1  1  1  1  0
123.050         1  0  0  0  0  1  1  1  0  1
123.075         1  0  0  0  0  1  1  1  0  0
123.100         1  0  0  0  0  1  1  0  1  1
123.125         1  0  0  0     1  1     1  0
123.150         1  0  0  0  0  1  1  0  0  1
123.175         1  0  0  0  0  1  1  0  0  0
123.200         1  0  0  0  0  1  0  1  1  1
123.225         1  0  0  0  0  1  0  1  1  0
123.250         1  0  0  0  0  1  0  1  0  1
123.275         1  0  0  0  0  1  0  1  0  0
123.300         1  0  0  0  0  1  0  0  1  1
123.325         1  0  0  0  0  1  0  0  1  0
123.350         1  0  0  0  0  1  0  0  0  1
123.375         1  0  0  0  0  1  0  0  0  0
123.400         1  0  0  0  0  0  1  1  1  1
123.425         1  0  0  0  0  0  1  1  1  0
123.450         1  0  0  0  0  0  1  1  0  1
123.475         1  0  0  0  0  0  1  1  0  0
123.500         1  0  0  0  0  0  1  0  1  1
123.525         1  0  0  0  0  0  1  0  1  0
123.550         1  0  0  0  0  0  1  0  0  1
123.575         1  0  0  0  0  0  1  0  0  0
123.600         1  0  0  0  0  0  0  1  1  1
123.625         1  0  0  0  0  0  0  1  1  0
123.650         1  0  0  0  0  0  0  1  0  1
123.675         1  0  0  0  0  0  0  1  0  0
123.700         1  0  0  0  0  0  0  0  1  1
123.725         1  0  0  0  0  0  0  0  1  0
123.750         1  0  0  0  0  0  0  0  0  1
123.775         1  0  0  0  0  0  0  0  0  0
123.800         0  1  1  1  1  1  1  1  1  1
123.825         0  1  1  1  1  1  1  1  1  0
123.850         0  1  1  1  1  1  1  1  0  1
123.875         0  1  1  1  1  1  1  1  0  0
123.900         0  1  1  1  1  1  1  0  1  1
123.925         0  1  1  1  1  1  1  0  1  0
123.950         0  1  1  1  1  1  1  0  0  1
123.975         0  1  1  1  1  1  1  0  0  0
124.000         0  1  1  1  1  1  0  1  1  1
124.025         0  1  1  1  1  1  0  1  1  0
124.050         0  1  1  1  1  1  0  1  0  1
124.075         0  1  1  1  1  1  0  1  0  0
124.100         0  1  1  1  1  1  0  0  1  1
124.125         0  1  1  1  1  1  0  0  1  0
124.150         0  1  1  1  1  1  0  0  0  1
124.175         0  1  1  1  1  1  0  0  0  0
124.200         0  1  1  1  1  0  1  1  1  1
124.225         0  1  1  1  1  0  1  1  1  0
124.250         0  1  1  1  1  0  1  1  0  1
```

|  |  |  |  |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|---|---|
| 124.275 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 124.300 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 124.325 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 124.350 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 124.375 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 124.400 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 124.425 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 124.450 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 124.475 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 124.500 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 124.525 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 124.550 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 124.575 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 124.600 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 124.625 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 124.650 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 124.675 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 124.700 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 124.725 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 124.750 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 124.775 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 124.800 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 124.825 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 124.850 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 124.875 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 124.900 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 124.925 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 124.950 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 124.975 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 125.000 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 125.025 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 125.050 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 125.075 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 125.100 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 125.125 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 125.150 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 125.175 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 125.200 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 125.225 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 125.250 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 125.275 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 125.300 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 125.325 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 125.350 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 125.375 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 125.400 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 125.425 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 125.450 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 125.475 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 125.500 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 125.525 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 125.550 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 125.575 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 125.600 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 125.625 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 125.650 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 125.675 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 125.700 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 125.725 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 125.750 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 125.775 | [illegible] | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 125.800 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 125.825 | 0 | 1 | 1 | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | 1 | [illegible] |
| 125.850 | 0 | 1 | 1 | 0 | 1 | [illegible] | 1 | 1 | 0 | 1 |
| 125.875 | [illegible] | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 125.900 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | [illegible] | 1 | 1 |
| 125.925 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 125.950 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 125.975 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 126.000 | [illegible] | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 126.025 | 0 | 1 | 1 | 0 | 1 | 0 | [illegible] | 1 | 1 | 0 |
| 126.050 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 126.075 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 126.100 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 126.125 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 126.150 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 126.175 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 126.200 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 126.225 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 126.250 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 126.275 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 126.300 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 126.325 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 126.350 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 126.375 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 126.400 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 126.425 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 126.450 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 126.475 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 126.500 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 126.525 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 126.550 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 126.575 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 126.600 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 126.625 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 126.650 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 126.675 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 126.700 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 126.725 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 126.750 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 126.775 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 126.800 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 126.825 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 126.850 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 126.875 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 126.900 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 126.925 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 126.950 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 126.975 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 127.000 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 127.025 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 127.050 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 127.075 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 127.100 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 127.125 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 127.150 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

|  |  |  |  |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|---|---|
| 127.175 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 127.200 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 127.225 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 127.250 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 127.275 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 127.300 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 127.325 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 127.350 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 127.375 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 127.400 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 127.425 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 127.450 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 127.475 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 127.500 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 127.525 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 127.550 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 127.575 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 127.600 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 127.625 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 127.650 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 127.675 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 127.700 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 127.725 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 127.750 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 127.775 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 127.800 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 127.825 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 127.850 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 127.875 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 127.900 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 127.925 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 127.950 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 127.975 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 128.000 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 128.025 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 128.050 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 128.075 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 128.100 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 128.125 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 128.150 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 128.175 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 128.200 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 128.225 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 128.250 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 128.275 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 128.300 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 128.325 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 128.350 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 128.375 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 128.400 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 128.425 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 128.450 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 128.475 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 128.500 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 128.525 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 128.550 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 128.575 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | [illegible] | 0 |
| 128.600 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 128.625 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 128.650 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 128.675 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 128.700 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 128.725 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 128.750 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 128.775 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 128.800 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 128.825 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 128.850 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 128.875 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 128.900 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 128.925 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 128.950 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 128.975 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 129.000 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 129.025 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 129.050 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 129.075 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 129.100 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 129.125 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 129.150 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 129.175 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 129.200 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 129.225 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 129.250 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 129.275 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 129.300 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 129.325 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 129.350 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 129.375 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 129.400 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 129.425 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 129.450 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 129.475 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 129.500 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 129.525 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 129.550 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 129.575 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 129.600 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 129.625 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 129.650 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 129.675 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 129.700 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 129.725 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 129.750 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 129.775 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 129.800 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 129.825 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 129.850 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 129.875 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 129.900 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 129.925 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 129.950 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 129.975 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 130.000 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 130.025 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 130.050 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 130.075 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 130.100 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 130.125 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 130.150 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 130.175 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 130.200 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 130.225 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 130.250 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 130.275 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 130.300 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 130.325 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 130.350 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 130.375 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 130.400 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 130.425 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 130.450 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 130.475 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 130.500 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 130.525 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 130.550 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 130.575 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 130.600 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 130.625 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 130.650 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 130.675 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 130.700 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 130.725 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 130.750 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 130.775 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 130.800 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 130.825 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 130.850 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 130.875 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 130.900 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 130.925 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 130.950 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 130.975 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 131.000 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 131.025 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 131.050 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 131.075 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 131.100 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 131.125 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 131.150 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 131.175 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 131.200 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 131.225 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | [illegible] |
| 131.250 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 131.275 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | [illegible] | [illegible] |
| 131.300 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 131.325 | 0 | 0 | 1 | 1 | [illegible] | 1 | 0 | 0 | 1 | 0 |
| 131.350 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 131.375 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 131.400 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 131.425 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 131.450 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 131.475 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 131.500 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 131.525 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 131.550 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 131.575 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 131.600 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 131.625 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 131.650 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 131.675 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 131.700 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 131.725 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 131.750 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 131.775 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 131.800 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 131.825 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 131.850 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 131.875 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 131.900 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 131.925 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 131.950 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 131.975 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 132.000 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 132.025 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 132.050 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 132.075 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 132.100 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 132.125 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 132.150 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 132.175 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 132.200 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 132.225 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 132.250 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 132.275 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 132.300 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 132.325 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 132.350 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 132.375 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 132.400 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 132.425 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 132.450 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 132.475 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 132.500 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 132.525 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 132.550 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 132.575 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 132.600 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 132.625 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 132.650 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 132.675 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 132.700 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 132.725 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 132.750 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 132.775 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 132.800 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 132.825 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 132.850 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 132.875 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 132.900 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 132.925 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 132.950 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 132.975 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 133.000 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 133.025 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 133.050 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 133.075 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 133.100 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 133.125 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 133.150 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 133.175 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 133.200 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 133.225 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 133.250 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 133.275 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 133.300 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 133.325 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 133.350 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 133.375 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 133.400 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 133.425 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 133.450 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 133.475 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 133.500 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 133.525 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 133.550 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 133.575 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 133.600 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 133.625 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 133.650 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 133.675 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 133.700 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 133.725 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 133.750 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 133.775 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 133.800 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 133.825 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 133.850 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 133.875 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 133.900 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 133.925 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 133.950 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 133.975 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 134.000 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 134.025 | 0 | 0 | 0 | 1 | 1 | 0 | [illegible] | 1 | 1 | 0 |
| 134.050 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 134.075 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 134.100 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 134.125 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 134.150 | 0 | 0 | 0 | 1 | 1 | [illegible] | 0 | 0 | 0 | 1 |
| 134.175 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 134.200 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 134.225 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 134.250 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 134.275 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 134.300 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 134.325 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 134.350 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 134.375 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 134.400 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 134.425 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 134.450 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 134.475 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 134.500 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 134.525 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 134.550 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 134.575 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 134.600 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 134.625 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 134.650 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 134.675 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 134.700 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 134.725 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 134.750 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 134.775 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 134.800 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 134.825 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 134.850 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 134.875 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 134.900 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 134.925 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 134.950 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 134.975 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 135.000 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 135.025 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 135.050 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 135.075 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 135.100 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 135.125 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 135.150 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 135.175 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 135.200 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 135.225 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 135.250 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 135.275 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 135.300 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 135.325 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 135.350 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 135.375 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 135.400 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 135.425 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 135.450 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 135.475 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 135.500 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 135.525 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 135.550 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 135.575 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 135.600 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 135.625 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 135.650 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 135.675 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 135.700 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 135.725 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 135.750 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 135.775 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 135.800 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 135.825 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 135.850 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

```
135.875            0   0   0   0   0   1   1   1   0   0
135.900            0   0   0   0   0   1   1   0   1   1
135.925            0   0   0   0   0   1   1   0   1   0
135.950            0   0   0   0   0   1   1   0   0   1
135.975            0   0   0   0   0   1   1   0   0   0
136.000            0   0   0   0   0   1   0   1   1   1
136.025            0   0   0   0   0   1   0   1   1   0
136.050            0   0   0   0   0   1   0   1   0   1
136.075            0   0   0   0   0   1   0   1   0   0
136.100            0   0   0   0   0   1   0   0   1   1
136.125            0   0   0   0   0   1   0   0   1   0
136.150            0   0   0   0   0   1   0   0   0   1
136.175            0   0   0   0   0   1   0   0   0   0
136.200            0   0   0   0   0   0   1   1   1   1
136.225            0   0   0   0   0   0   1   1   1   0
136.250            0   0   0   0   0   0   1   1   0   1
136.275            0   0   0   0   0   0   1   1   0   0
136.300            0   0   0   0   0   0   1   0   1   1
136.325            0   0   0   0   0   0   1   0   1   0
136.350            0   0   0   0   0   0   1   0   0   1
136.375            0   0   0   0   0   0   1   0   0   0
136.400            0   0   0   0   0   0   0   1   1   1
136.425            0   0   0   0   0   0   0   1   1   0
136.450            0   0   0   0   0   0   0   1   0   1
136.475            0   0   0   0   0   0   0   1   0   0
136.500            0   0   0   0   0   0   0   0   1   1
136.525            0   0   0   0   0   0   0   0   1   0
136.550            0   0   0   0   0   0   0   0   0   1
136.575            0   0   0   0   0   0   0   0   0   0
```

## 2.6.7 Synthesizer Program

The SYNTHESIZER PROGRAM card converts the multi-digit BCD code, stored in the FREQUENCY DECODER card, to a 10-bit binary code suitable for use by the receiver synthesizer.

Since the first digit in the frequency is always a '1', it is ignored by the SYNTHESIZER PROGRAM card. The next five digits are used to program five pre-settable counters U1 to U5. These counters are set to the 'decimal' and 'count-down' modes. The clock pulses for the counters are derived from the 1.76 MHz system clock through a divide-by-two Flip-Flop (½ of U7), which results in an actual clock frequency of 880 kHz. The divide-by-two circuit is enabled by the 'information complete' strobe which is the signal from the FREQUENCY DECODER card that the storage of the frequency doe has been completed. When this strobe is received by pin #3 the Flip-Flop U6 it generates a brief pulse which causes counters U1 to U5 to be preset to the BCD codes received from the FREQUENCY DECODER card. At the end of the preset pulse, the second half of U6 is triggered, which removes the RESET signal from pin #10 of U7 and allows the clock pulses to be applied to the counters.

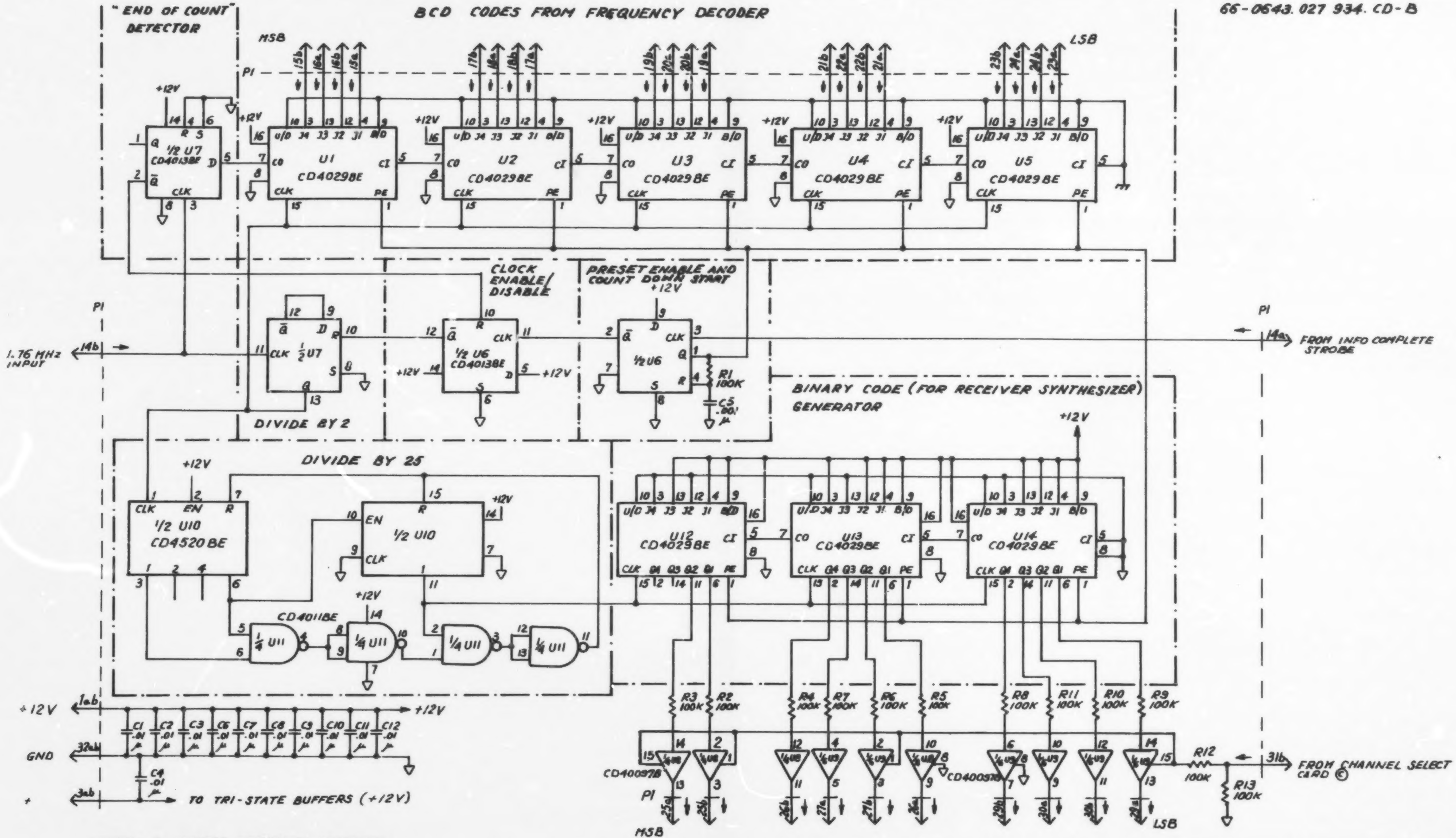
The same clock pulses are also applied to U10 which, together with U11, forms a divide-by-25 circuit. This division eliminates all the possible meaningless codes which could be generated by trying to retune the receiver to any frequency not used in the 25 kHz channel spacing.

A second set of counters, U12 to U14, are preset to the binary equivalent of the decimal number 1463. These counters are set to the 'binary' and 'count-down' modes. The outputs of these counters are applied to the inputs of tri-state buffers and represent the actual code needed by the synthesizer.

The basic operation is as follows: The BCD equivalents of the last five digits of the frequency selected are latched into the first set of counters (U1 to U5). A series of clock pulses is then used to decrement the counters until they reach zero. The same series of pulses is divided by 25 and used to decrement the second set of counters (U12 to U14). When the first set reaches the zero count, it stops the clock and whatever remains in the second set is the code for the synthesizer.

The tri-state buffers are used to disable the output when the 'channel select' mode is used, rather than the 'frequency select' mode.

66-0643.027 934. CD-B


"END OF COUNT" DETECTOR
BCD CODES FROM FREQUENCY DECODER
MSB
LSB
P1
15b
16a
16b
15a
17b
18a
18b
17a
19b
20a
20b
19a
21b
22a
22b
21a
23b
24a
24b
23a
+12V
1/2 U7 CD4013BE
U1 CD4029BE
U2 CD4029BE
U3 CD4029BE
U4 CD4029BE
U5 CD4029BE
CLOCK ENABLE/ DISABLE
PRESET ENABLE AND COUNT DOWN START
1.76 MHz INPUT
14b
1/2 U7
1/2 U6 CD4013BE
1/2 U6
R1 100K
C5 .001 µ
14a
FROM INFO COMPLETE STROBE
DIVIDE BY 2
BINARY CODE (FOR RECEIVER SYNTHESIZER) GENERATOR
DIVIDE BY 25
1/2 U10 CD4520BE
1/2 U10
CD4011BE
1/4 U11
U12 CD4029BE
U13 CD4029BE
U14 CD4029BE
R3 100K
R2 100K
R4 100K
R7 100K
R6 100K
R5 100K
R8 100K
R11 100K
R10 100K
R9 100K
CD40097B
1/6 U8
1/6 U9
R12 100K
R13 100K
31b
FROM CHANNEL SELECT CARD ©
25a
25b
26b
27a
27b
28a
29b
30a
30b
28a
MSB
LSB
+12V
1ab
C1 .01 µ
C2 .01 µ
C3 .01 µ
C6 .01 µ
C7 .01 µ
C8 .01 µ
C9 .01 µ
C10 .01 µ
C11 .01 µ
C12 .01 µ
C4 .01 µ
GND
32ab
3ab
TO TRI-STATE BUFFERS (+12V)

NOTES: 1. UNLESS OTHERWISE SPECIFIED

a) ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W

b) ALL CAPACITOR VALUES ARE IN FARADS.

2-213

This drawing is the property of BAYLY ENGINEERING LIMITED and may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others without written permission.

| REV NO | REVISION | DATE | APPR. BY |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 24.02.83 | |
| 01 | RELEASED | JAN. 14 82 | |

DRAWN BY I CLARK | DATE NOV 11.81 | CHECKED BY

BAYLY ENGINEERING LTD a member of

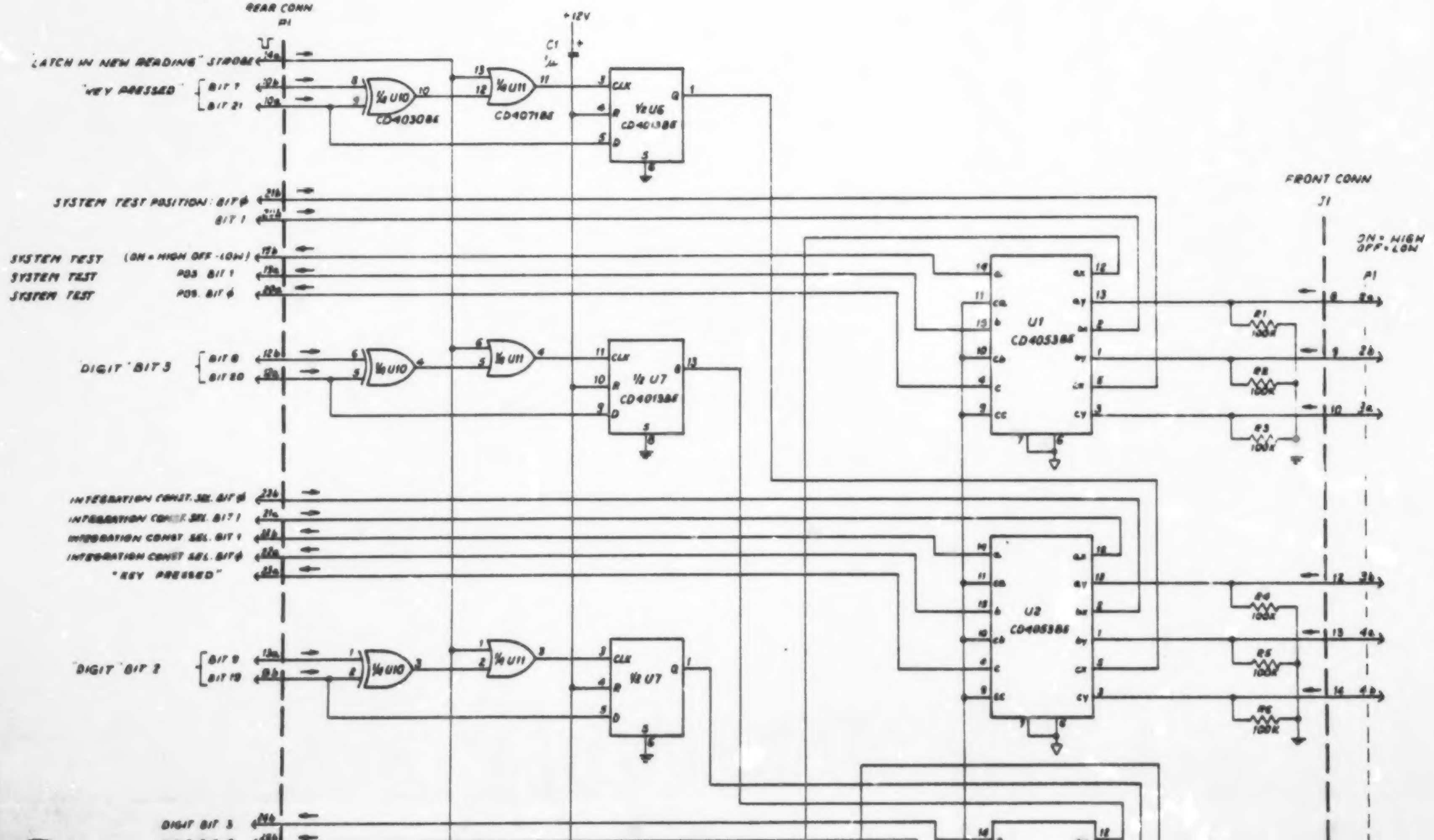
TITLE SCHEMATIC DIAGRAM SYNTHESIZER PROGRAM CARD

DWG NO. 66-0643.027 934. CD-B 01

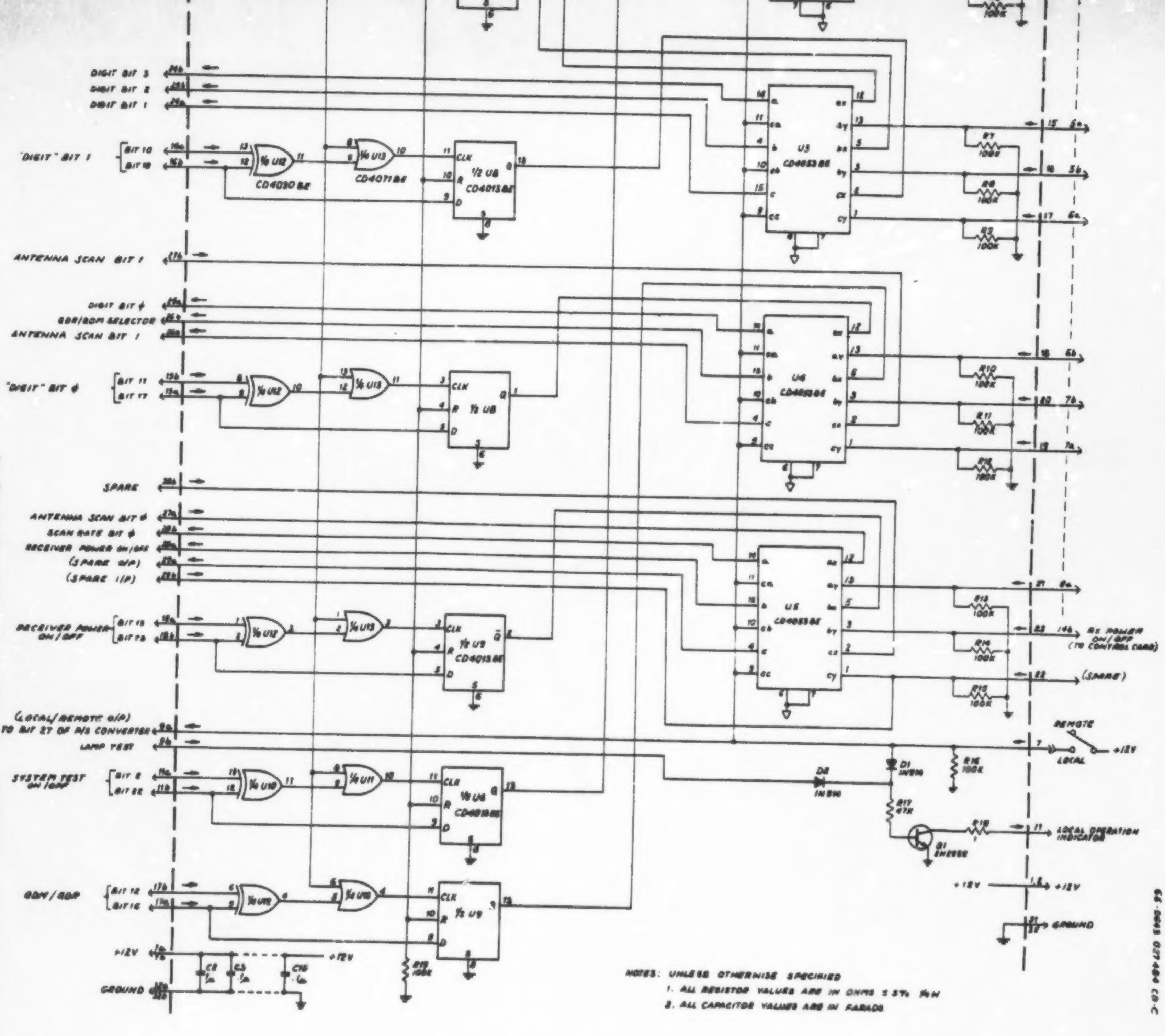
### 2.6.8 Local/Remote Switch

The LOCAL/REMOTE SWITCH card is used in the receiver control panel to select whether the receiver is controlled from the local front panel or a remotely located operator's control panel. Five Triple 2-channel multiplexers (U1 to U5) select the source for the control signals. The selection itself is controlled by a toggle switch on the front panel (connected to front connector pin #7). The mode of the card is indicated by the white front panel lamp ('PANEL ACTIVE') which is driven by Q1 in this unit.

The second function of this card is the error checking and confirmation of any critical signals sent by the remote control unit(s). All critical data is duplicated at different points in the data stream. The EXCLUSIVE OR gates (U10 and U12) compare these separate signals and pass any changes on to the receiver only if they are identical. A negative going strobe from the SERIAL-TO-PARALLEL CONVERTER signifies that conversion is complete and the applied data may be read. However, positive outputs from the EXCLUSIVE OR gates (signifying that their two inputs are not the same) will override this strobe and leave the Flip-Flops (U6 to U9) in the state they assumed when the last valid signals were received.



REAR CONN
P1
"LATCH IN NEW READING" STROBE
"KEY PRESSED"
BIT 7
BIT 21
SYSTEM TEST POSITION: BIT Ø
BIT 1
SYSTEM TEST (ON = HIGH OFF - LOW)
SYSTEM TEST POS. BIT 1
SYSTEM TEST POS. BIT Ø
"DIGIT" BIT 3
BIT 8
BIT 20
INTEGRATION CONST. SEL. BIT Ø
INTEGRATION CONST. SEL. BIT 1
INTEGRATION CONST. SEL. BIT 1
INTEGRATION CONST. SEL. BIT Ø
"KEY PRESSED"
"DIGIT" BIT 2
BIT 9
BIT 19
DIGIT BIT 3
¼ U10
CD4030BE
¼ U11
CD4071BE
+12V
C1
½ U6
CD4013BE
½ U7
CD4013BE
½ U7
U1
CD4053BE
U2
CD4053BE
R1 100K
R2 100K
R3 100K
R4 100K
R5 100K
R6 100K
FRONT CONN
J1
ON = HIGH
OFF = LOW
P1
2a
2b
3a
3b
4a
4b


DIGIT BIT 3
DIGIT BIT 2
DIGIT BIT 1
"DIGIT" BIT 1
BIT 10
BIT 18
CD4030BE
CD4071BE
1/2 U8 CD4013BE
U3 CD4053BE
R7 100K
R8 100K
R9 100K
ANTENNA SCAN BIT 1
DIGIT BIT 4
BDR/BDM SELECTOR
ANTENNA SCAN BIT 1
"DIGIT" BIT 4
BIT 11
BIT 17
U4 CD4053BE
R10 100K
R11 100K
R12 100K
SPARE
ANTENNA SCAN BIT 4
SCAN RATE BIT 4
RECEIVER POWER ON/OFF
(SPARE O/P)
(SPARE I/P)
RECEIVER POWER ON/OFF
BIT 19
BIT 23
1/2 U9 CD4013BE
U5 CD4053BE
R13 100K
R14 100K
R15 100K
RX POWER ON/OFF (TO CONTROL CARD)
(SPARE)
(LOCAL/REMOTE O/P) TO BIT 27 OF P/S CONVERTER
LAMP TEST
REMOTE
LOCAL
+12V
R16 100K
D1 1N914
D2 1N914
R17 47K
R18
Q1 2N2222
LOCAL OPERATION INDICATOR
SYSTEM TEST ON/OFF
BIT 8
BIT 22
1/2 U8 CD4013BE
BDM/BDP
BIT 12
BIT 16
1/2 U9
R19 100K
+12V
GROUND
C8
C9
C10
+12V
GROUND

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS ± 5% ¼W
2. ALL CAPACITOR VALUES ARE IN FARADS

66-0645 027484 CD-C

2-215

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others.

| | | | |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 25 08 80 | K |
| — | RELEASED | DEC. 17 81 | VS |
| REV. | REVISION | DATE | APP'D |

DRAWN VS DATE FEB 16 81

**BAYLY** ENGINEERING LTD a member of

TITLE SCHEMATIC DIAGRAM LOCAL REMOTE SW.

DWG NO. 66-0645.027 484. CD-C 01

### 2.6.9 Stored Display Decoder

The operation of the STORED DISPLAY DECODER is basically identical to that of the MAIN DISPLAY DECODER. The difference is in the strobe used to latch the bearing into the display decoder/drivers. After the serial-to-parallel conversion is complete, the SERIAL-TO-PARALLEL converter sends out the 'latch-in-previous reading' strobe, which causes the STORED DISPLAY DECODER to be updated to the previous valid reading. Should the previous reading be invalid (i.e. no DATA VALID signal), then updating is suppressed.

The display will be activated under one of the following conditions:

#### (a) No Signal Received

The last valid reading will appear on the display. However, the reading is not locked and will disappear when the next valid signal is received.

#### (b) Overhead Pass

The last reading before the overhead pass condition occurred will be seen on the stored display. This reading is not locked and will disappear when the transmitting aircraft leaves the overhead pass zone.

#### (c) System Alarm

Triggering of the system alarm will cause the last valid reading to appear on the stored display. The reading is not locked and will disappear when the next valid reading is received after the alarm condition has been cleared.

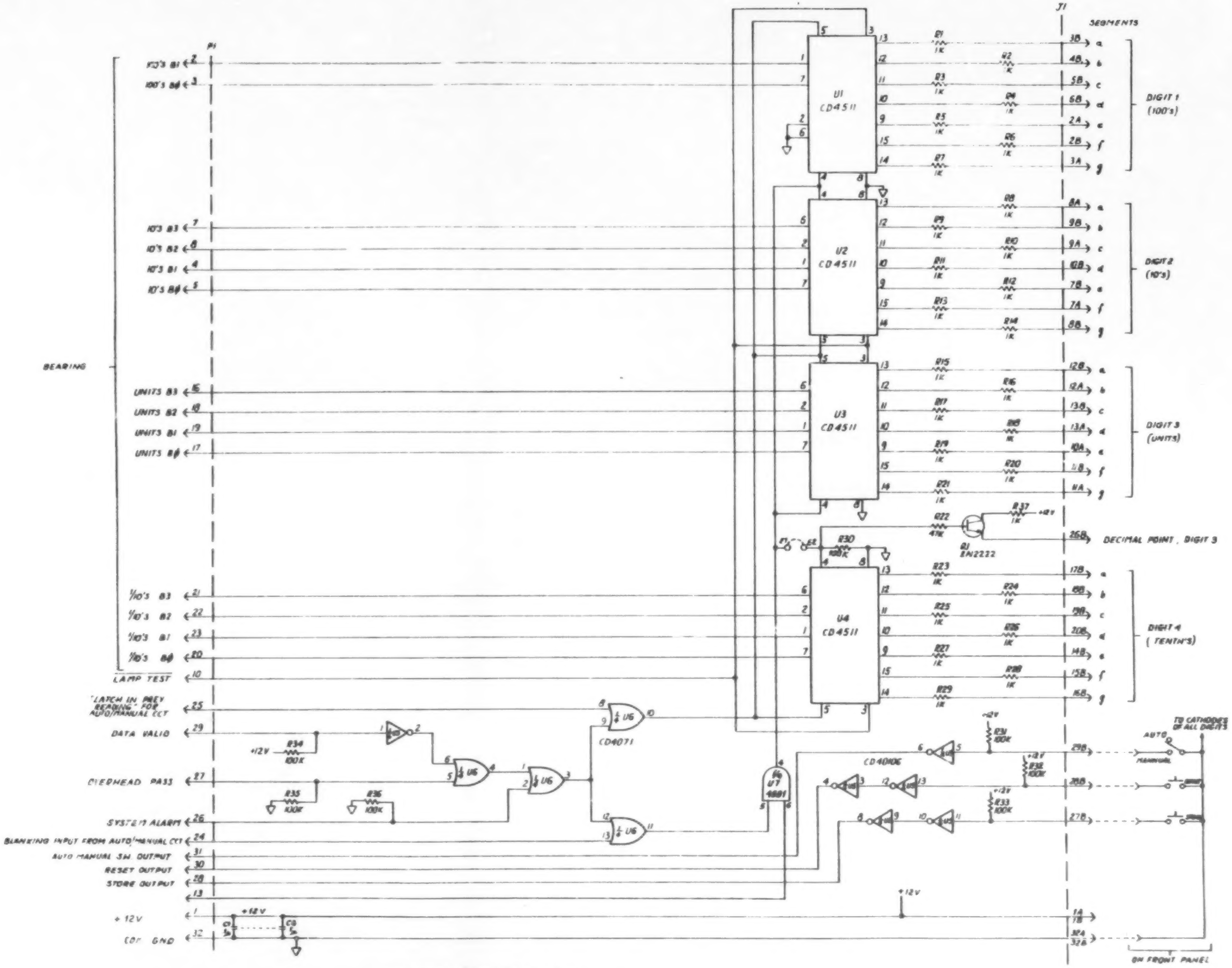
Note: Since, under the above conditions, the reading is not actually locked in the storage, pressing the store RESET button will have no affect.

#### (d) Manual Storage

When the STORE button on the front panel is pressed, the reading currently on the main display will be locked into the stored display. The reading will stay on the display until it is cancelled with the storage RESET button.

#### (e) Auto Emergency Switchover

If an automatic selection of the emergency channel has occurred, the bearing obtained from the first valid transmission of the emergency transmitter will be locked into the stored display. It can only be cancelled by pressing the storage RESET button.


P1
100'S B1
100'S BØ
10'S B3
10'S B2
10'S B1
10'S BØ
BEARING
UNITS B3
UNITS B2
UNITS B1
UNITS BØ
1/10'S B3
1/10'S B2
1/10'S B1
1/10'S BØ
LAMP TEST
"LATCH IN PREV BEARING" FOR AUTO/MANUAL CCT
DATA VALID
OVERHEAD PASS
SYSTEM ALARM
BLANKING INPUT FROM AUTO/MANUAL CCT
AUTO MANUAL SW OUTPUT
RESET OUTPUT
STORE OUTPUT
+ 12V
COM GND
U1 CD4511
U2 CD4511
U3 CD4511
U4 CD4511
CD4071
CD40106
U7 4081
Q1 2N2222
R22 47K
R30 100K
R34 100K
R35 100K
R36 100K
R37 1K
C1
C8
J1
SEGMENTS
DIGIT 1 (100's)
DIGIT 2 (10's)
DIGIT 3 (UNITS)
DECIMAL POINT, DIGIT 3
DIGIT 4 (TENTH'S)
TO CATHODES OF ALL DIGITS
AUTO
MANUAL
ON FRONT PANEL

NOTES UNLESS OTHERWISE SPECIFIED
1 ALL RESISTOR VALUES ARE IN OHMS ±5%, ¼W
2 ALL CAPACITOR VALUES ARE IN FARADS

2-217

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others.

| REV. | REVISION | DATE | APP. |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 80 02 03 | |
| — | RELEASED | | |

DRAWN A SMITH DATE FEB 9.81

BAYLY ENGINEERING LTD

SCHEMATIC DIAGRAM
STORED DISPLAY

DWG NO 66-0643 027 775 CD-C 01

### 2.6.10 Main Display Decoder

The MAIN DISPLAY DECODER (sometimes called the BEARING DISPLAY DECODER) takes the 4-digit BCD encoded bearing value and decodes it for the 7-segment display. The decoding itself is done in the four BCD-to-7 segment decoders U1 to U4. The latching in these decoders is done by applying the 'new date strobe' to the latching inputs of the decoders (pin #5). The 'new data strobe' is a negative going pulse sent out by the SERIAL-TO-PARALLEL CONVERTER to signify that conversion is complete and the codes are valid.

Pin #4 on the decoders is the blanking input (0=display blanked) and this input is controlled by three different signals:

(a) The INTENSITY is a pulse train with a variable duty cycle coming from the control board to control the intensity of the displays.

(b) The DATA VALID signal comes from the DF Receiver to indicate that the bearing displayed is indeed a valid reading. The display will be blanked if the data presented to the inputs of the decoders are not valid.

Note: In later versions, including the marine version, an oscillator is added to this line so that the display will flash, rather than blank, when the reading is invalid. This would allow the operator to still be able to get a reading on a transmitter which would be too weak for an accurate bearing value.

(c) OVERHEAD PASS is a signal taken either from the steady output of the SERIAL-TO-PARALLEL CONVERTER, or from the output of a low frequency oscillator located on the SYSTEM CONTROL board, depending on whether the display should be blanked or flashed when an overhead pass occurs.

Pin #4 of U4 is connected to the rest of the blanking inputs by a jumper marked 'A----B' on the diagram. If the jumper is installed, the display will have four digits and a decimal point between the third and fourth digits. If the jumper is left out, or removed, the fourth digit and the decimal point are permanently blanked and the bearing will be shown to the nearest degree only.

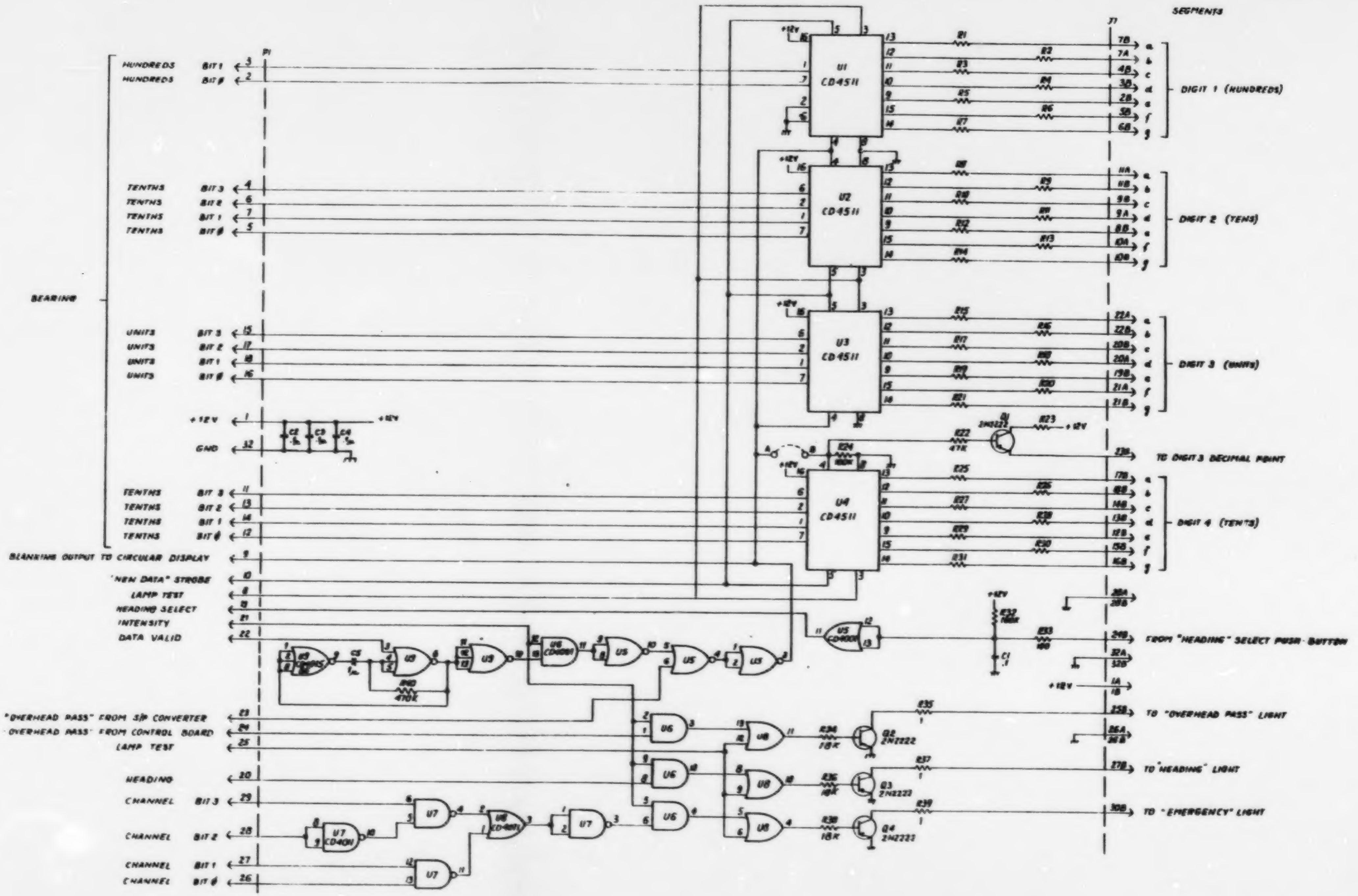
The LAMP TEST and $\overline{\text{LAMP TEST}}$ lines come from the SYSTEM CONTROL board and will activate all displays with full brightness when the LAMP TEST pushbutton on the front panel is pressed.

The HEADING signal activates a light on the front panel which shows that the reading on the 7-segment display represents a 'heading' (QDR) rather than a 'bearing' (QDM).

The four bits of the BCD code representing the channel number are also decoded and a transistor driver (Q4) will activate the EMERGENCY light on the front panel to show that the receiver is now tuned to the emergency channel (121.500 MHz).

The 'heading' mode is selected by pressing the HEADING pushbutton on the front panel. This pushbutton switch is connected to pin #24b on the front connector of the main display decoder and goes low whenever the button is pressed. This is turned to a high signal in the inverter (one section of U5) and sent to pin #20 (pin #19 on later versions) to send the appropriate control signal to the receiver.

67-0643 027 235 CD-C


SEGMENTS
HUNDREDS BIT 1
HUNDREDS BIT Ø
TENTHS BIT 3
TENTHS BIT 2
TENTHS BIT 1
TENTHS BIT Ø
BEARING
UNITS BIT 3
UNITS BIT 2
UNITS BIT 1
UNITS BIT Ø
+12V
GND
TENTHS BIT 3
TENTHS BIT 2
TENTHS BIT 1
TENTHS BIT Ø
BLANKING OUTPUT TO CIRCULAR DISPLAY
"NEW DATA" STROBE
LAMP TEST
HEADING SELECT
INTENSITY
DATA VALID
"OVERHEAD PASS" FROM S/P CONVERTER
"OVERHEAD PASS" FROM CONTROL BOARD
LAMP TEST
HEADING
CHANNEL BIT 3
CHANNEL BIT 2
CHANNEL BIT 1
CHANNEL BIT Ø
P1
J1
U1 CD4511
U2 CD4511
U3 CD4511
U4 CD4511
U5 CD4001
U6 CD4081
U7 CD4011
U8 CD4071
Q1 2N2222
Q2 2N2222
Q3 2N2222
Q4 2N2222
R22 47K
R23
R24
R32 100K
R33 100
R34 18K
R36 18K
R38 18K
R40 470K
C1
C2
C3
C4
DIGIT 1 (HUNDREDS)
DIGIT 2 (TENS)
DIGIT 3 (UNITS)
TO DIGIT 3 DECIMAL POINT
DIGIT 4 (TENTHS)
FROM "HEADING" SELECT PUSH-BUTTON
TO "OVERHEAD PASS" LIGHT
TO "HEADING" LIGHT
TO "EMERGENCY" LIGHT

NOTES: UNLESS OTHERWISE SPECIFIED

1 R1 TO R21, R33 AND R35 TO R31 ARE ALL 1kΩ, 5%, ¼W

2 ALL CAPACITOR VALUES ARE IN FARADS

2-220

| REV NO | REVISION | DATE | APPD BY |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 25.02.83 | I.C. |
| a | U8, C5 & R40 ADDED | MARCH 1 82 | WS |

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

DRAWN BY A SMITH | DATE MAY 7, 81 | CHECKED BY | APPD BY | STOCK

**BAYLY** ENGINEERING LTD a member of

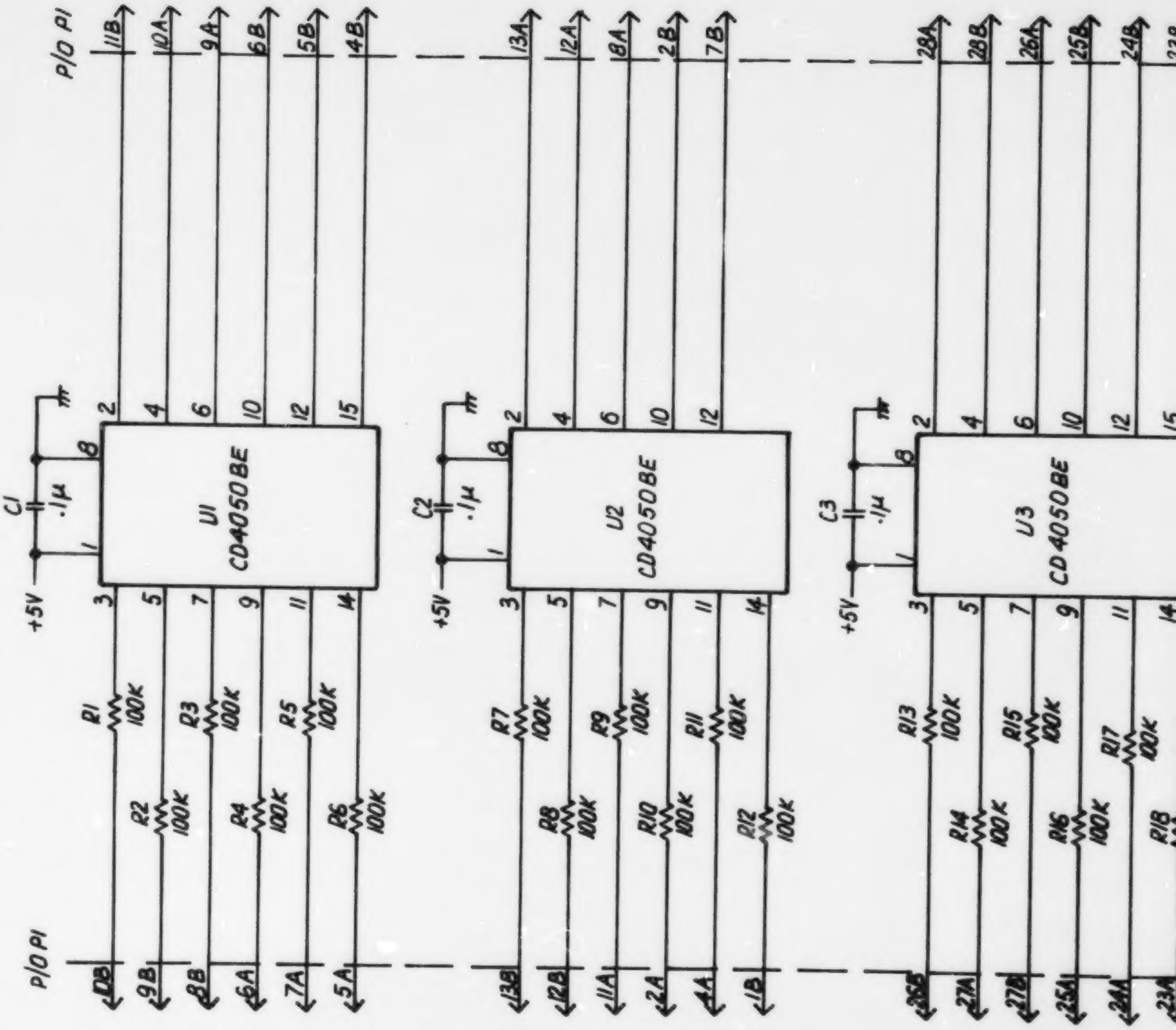
TITLE SCHEMATIC DIAGRAM
MAIN DISPLAY DECODER

DWG NO 67-0643.027 235.CD-C 01

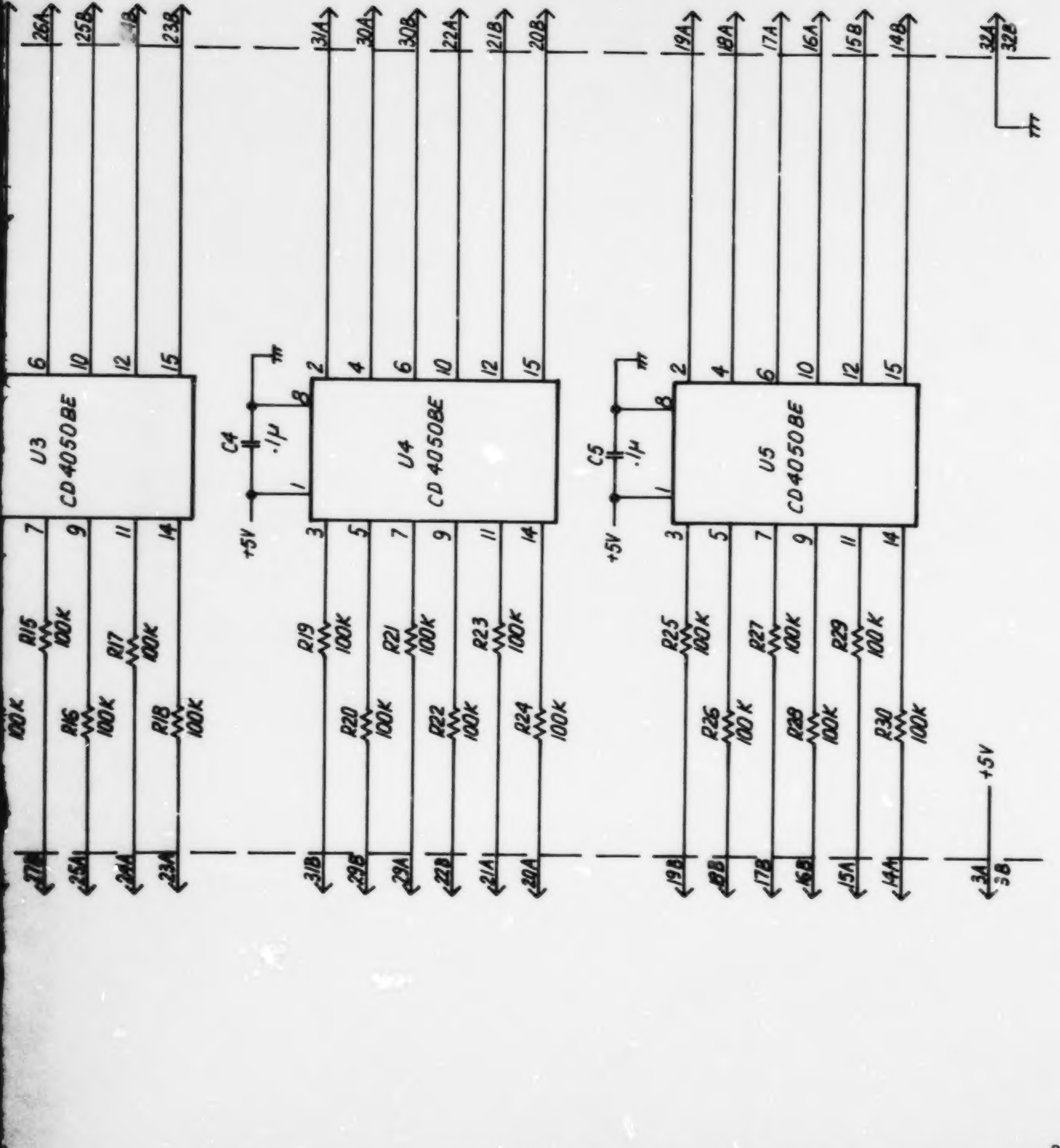
## 2.6.11 Peripheral Interface

The PERIPHERAL INTERFACE card is used in the Operator's Console to provide buffered, TTL-level outputs for 29 of the 30 data lines from the Serial-to-Parallel Converter. This will allow the connection of peripheral equipment, such as data logging equipment to the Operator's Console.

Five Hex CMOS buffers, U1 to U5, are used for the buffering and level translation. A type 4050 CMOS buffer is used which was especially designed for level translation and can drive two TTL inputs or 9 LSTTL inputs. The buffers are powered from the unit's 5V supply, rather than the 12V supply used for the rest of the logic system to provide the level translation. Resistors R1 to R30 augment the input protection already included in the 4050's, so that the circuits can be safely driven with the +12V levels from the rest of the system.


P/O P1
11B
10A
9A
6B
5B
4B
13A
12A
8A
2B
7B
28A
28B
26A
25B
24B
C1 .1μ
+5V
U1 CD4050BE
C2 .1μ
U2 CD4050BE
C3 .1μ
U3 CD4050BE
1
8
2
4
6
10
12
15
3
5
7
9
11
14
R1 100K
R2 100K
R3 100K
R4 100K
R5 100K
R6 100K
R7 100K
R8 100K
R9 100K
R10 100K
R11 100K
R12 100K
R13 100K
R14 100K
R15 100K
R16 100K
R17 100K
R18
10B
9B
8B
6A
7A
5A
13B
12B
11A
2A
4A
1B
26B
27A
27B
25A
24A
23A

This drawing is the property of BAYLY
LIMITED and may be neither used, copied,
or otherwise dealt with nor its contents communicated
others without written permission.


26A
25B
23B
31A
30A
30B
22A
21B
20B
19A
18A
17A
16A
15B
14B
32A
32B
U3
CD4050BE
U4
CD4050BE
U5
CD4050BE
C4
.1μ
C5
.1μ
+5V
+5V
+5V
6
10
12
15
7
9
11
14
2
4
6
10
12
15
8
1
3
5
7
9
11
14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
100K
27B
25A
24A
23A
31B
29B
29A
22B
21A
20A
19B
18B
17B
16B
15A
14A
3A
3B

| | | | |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| 01 | RELEASED | 11.01.82 | M.P. |
| REV NO. | REVISION | DATE | APPR. BY |

DRAWN BY A. SMITH | DATE FEB. 5, 81 | CHECKED BY | APPR. BY

BAYLY ENGINEERING LTD
a member of

TITLE SCHEMATIC DIAGRAM
PERIPHERAL INTERFACE

DWG NO. 066-0643.027 505. CD-B | 01

## 2.6.12 Receiver Interface

The RECEIVER INTERFACE Card is used in the Receiver Console to provide the buffering and level translation required between the control system and the receiver itself.

There are two sections on this card:

(a) Signals coming from the receiver and going to the control system. These include:

Bearing or Heading Mode Indication

Digital Bearing Readout

Data Ready Strobe

Data Valid

Overhead Pass

These signals are handled by U1 to U3 which are Hex TTL buffers with open-collector outputs and 10 K Ohm pull-up resistors (R1 to R18) connected to +12V. This translates the TTL level signals from the receiver to the levels required by the control system (0V to +12V).

(b) Signals coming from the control system and going to the receiver. These include:

QDM/QDR mode selection

Antenna Scan Frequency Selection

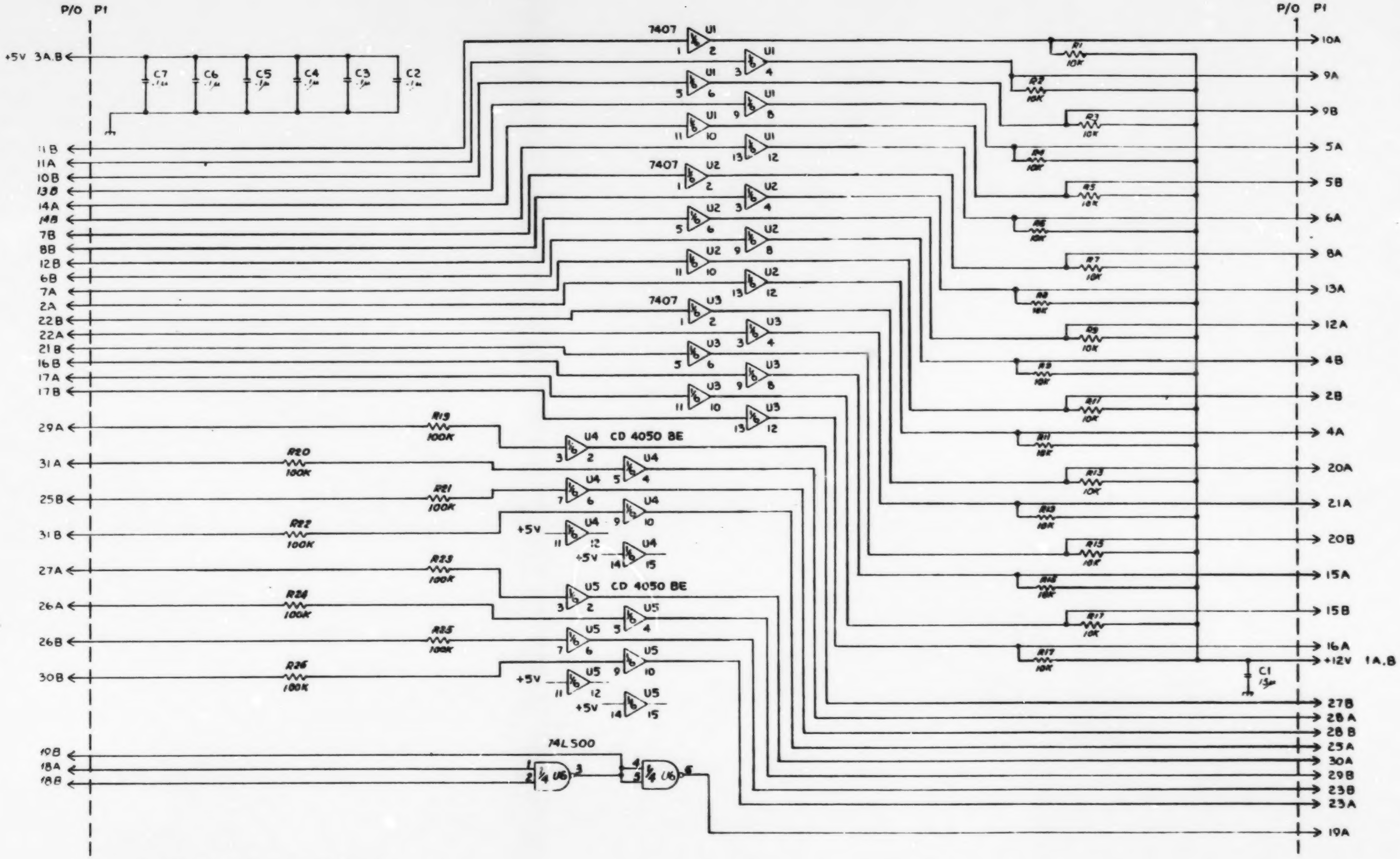
System Test

Integration Constant Selection

These signals are handled by U4 and U5, two type 4050 CMOS buffers which are powered from the 5V supply to provide TTL level outputs. Resistors R19 to R26 augment the input protection inherent in the 4050's so that they can be fed with the +12V level from the rest of the control system.

(The signals required by the local oscillator synthesizer to select the proper operating frequency can be provided by the CHANNEL SELECTOR and SYNTHESIZER PROGRAM cards at the required levels and need no interfacing).

66-0643 027 674 CD-C


P/O P1
+5V 3A,B
C7 .1μ
C6 .1μ
C5 .1μ
C4 .1μ
C3 .1μ
C2 .1μ
11B
11A
10B
13B
14A
14B
7B
8B
12B
6B
7A
2A
22B
22A
21B
16B
17A
17B
29A
31A
25B
31B
27A
26A
26B
30B
19B
18A
18B
7407
U1
U2
U3
1/6
R19 100K
R20 100K
R21 100K
R22 100K
R23 100K
R24 100K
R25 100K
R26 100K
U4 CD 4050 BE
U5 CD 4050 BE
+5V
74LS00
1/4 U6
R1 10K
R2 10K
R3 10K
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
R11 10K
R13 10K
R15 10K
R16 10K
R17 10K
C1 1.5μ
P/O P1
10A
9A
9B
5A
5B
6A
8A
13A
12A
4B
2B
4A
20A
21A
20B
15A
15B
16A
+12V 1A,B
27B
28A
28B
25A
30A
29B
23B
23A
19A

NOTES UNLESS OTHERWISE SPECIFIED

1 ALL RESISTORS VALUES ARE IN OHMS (1/4 W)
2 ALL CAPACITOR VALUES ARE IN FARADS.

2-224

Without prior written consent of BAYLY ENGINEERING LIMITED this document may be neither used, copied, reproduced or otherwise dealt with nor its contents communicated to others.

| | | | |
|---|---|---|---|
| 01 | RELEASED | DEC 14-81 | I.C. |
| REV. NO. | REVISION | DATE | APPR. BY |
| KP | JAN 29-81 | Q1 | |

BAYLY ENGINEERING LTD a member of

RX INTERFACE CARD
SCHEMATIC

DWG NO 66-0643 027 674 CD-C

### 2.6.13 Keyboard Encoder

The KEYBOARD ENCODER card has four functions:

(a) It decodes the channel number and drives the appropriate light on the front panel.

(b) It decodes the keypad on the front panel and generates the binary values for the numbers which are keyed in.

(c) It provides the automatic switchover to the emergency channel.

(d) It controls the storage of a bearing in the STORED DISPLAY.

Since a channel number corresponds to a 'position 0' in the position code for the digit, if any of the bits in the position code are not zero, then the digit will not be latched into the storage latch U1. Two BCD-Decimal decoders U6 and U7 are used to decode the channel number and address the corresponding lamp driver (Q1 to Q10). A four-input OR gate (¼ of U3) detects if any of the channel displays are selected and blanks the frequency display so that only a channel light or the frequency display can be enabled at any one time.

OR gates U10, U11 and three sections of U12 are used to light all lamps when the LAMP TEST button the front panel is pressed.

U17 is a special keyboard encoder IC which handles the scanning of a keyboard matrix, eliminates contact bounce and produces 4-bit binary output (with tri-state capability) and a DATA AVAILABLE output which goes high every time a key is present. This output provides the KEY PRESSED signal used on some of the other cards in the system.

The rest of the circuitry is used to provide the automatic switch to the emergency frequency. If the AUTO/MANUAL input (rear connector pin #19) is left open, the automatic switchover is enabled, but when it is connected to ground, the circuit is disabled and the emergency frequency has to be selected manually.

EMERGENCY INPUTS 1 and 2 go high if the emergency receiver picks up a call. The two inputs are compared in an Exclusive-OR gate which will suppress the registration of the call if the two inputs are not the same. The DATA VALID input (rear connector pin #26) would also be connected to one of these lines. When an emergency call is received, the inverted 'latch in new data' strobe triggers the monostable (½ of U15) which, in turn, produces a negative going pulse at its Q output (pin #12). If both EMERGENCY INPUTS are the same, the pulse passes on to the second half of U15. If the EMERGENCY INPUTS were high, this is passed on to the Q output (U15 pin #1) and the next Flip-Flop is set (½ of U13).

An EXCLUSIVE-OR gate (¼ of U4) compares the SET input and the Q output of U13 and starts the time-out for the switchover. The time required for this reset is about 1 second, as determined by R27 and C1. Thus, the emergency transmission can be intermittent without having the receiver switch back to its original frequency, unless the transmission disappears for at least 1 second.

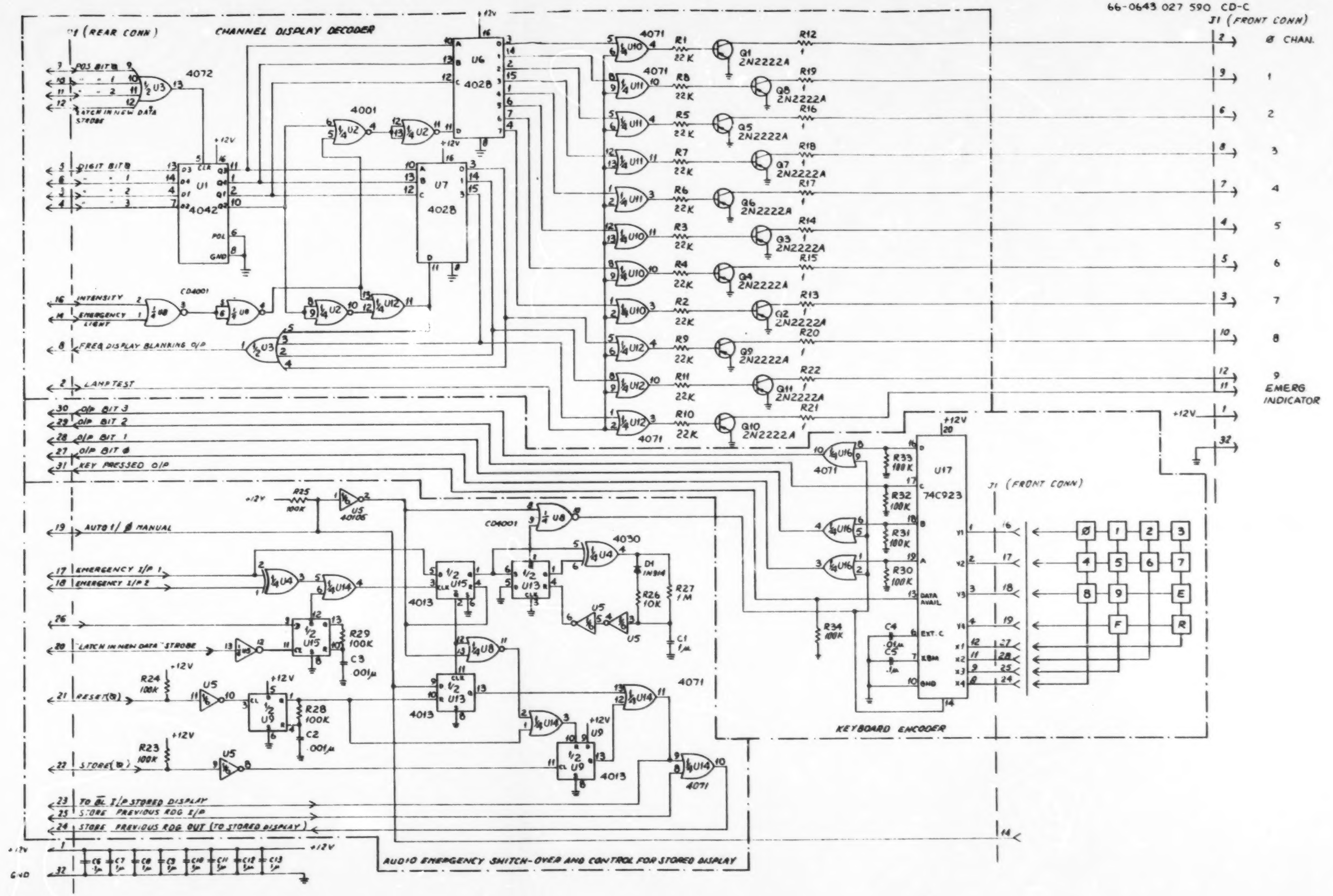
The Q output (U13 pin #1) is also taken to the keyboard encoder (U17) which now has its outputs disabled. Three OR gates (three sections of U16) substitute the binary code of the emergency channel for the disabled outputs of U17, and thus lead the CHANNEL DECODER to believe that the emergency channel has been selected. Since no KEY PRESSED strobe is sent, the original channel information in the CHANNEL DECODER is not destroyed and the receiver can go back to the original channel or frequency selection when the emergency transmission is terminated.

The STORED DISPLAY is normally blanked, but it is also constantly updated using the 'store previous reading' strobe from the SERIAL-TO-PARALLEL CONVERTER. This strobe is routed over the KEYBOARD ENCODER board so that it can be suppressed when a reading is stored. Storage can be operator actuated by use of the STORE pushbutton on the front panel. The button sets the output of a Flip-Flop (U9 pin #13) high which activates the stored display and suppresses any further updating.

The Flip-Flop can be reset by a pulse from the RESET Flip-Flop (the other half of U9) which is triggered by the RESET button on the front panel.

The second way to store a bearing is via the automatic emergency switchover. When the emergency transmission ceases, the Q output of U15 (pin #2) goes high again, providing a clock pulse on U13 pin #11 which causes the same action as the manual triggering. Thus, the last bearing of the transmitter on the emergency frequency is locked into the stored display and can only be cancelled by pressing the RESET button on the front panel.

66-0643 027 590 CD-C


J1 (REAR CONN)
CHANNEL DISPLAY DECODER
J1 (FRONT CONN)
POS BIT 0
POS BIT 1
POS BIT 2
LATCH IN NEW DATA STROBE
DIGIT BIT 0
DIGIT BIT 1
DIGIT BIT 2
DIGIT BIT 3
INTENSITY
EMERGENCY LIGHT
FREQ DISPLAY BLANKING O/P
LAMP TEST
O/P BIT 3
O/P BIT 2
O/P BIT 1
O/P BIT 0
KEY PRESSED O/P
AUTO 1/0 MANUAL
EMERGENCY I/P 1
EMERGENCY I/P 2
"LATCH IN NEW DATA" STROBE
RESET(0)
STORE(0)
TO BL I/P STORED DISPLAY
STORE PREVIOUS RDG I/P
STORE PREVIOUS RDG OUT (TO STORED DISPLAY)
+12V
GND
4072
4042
4001
4028
CD4001
4071
4013
4030
40106
74C923
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
Q1 2N2222A
Q2 2N2222A
Q3 2N2222A
Q4 2N2222A
Q5 2N2222A
Q6 2N2222A
Q7 2N2222A
Q8 2N2222A
Q9 2N2222A
Q10 2N2222A
Q11 2N2222A
R1 22K
R2 22K
R3 22K
R4 22K
R5 22K
R6 22K
R7 22K
R8 22K
R9 22K
R10 22K
R11 22K
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23 100K
R24 100K
R25 100K
R26 10K
R27 1M
R28 100K
R29 100K
R30 100K
R31 100K
R32 100K
R33 100K
R34 100K
C1 1µ
C2 .001µ
C3 .001µ
C4 .01µ
C5 .1µ
C6 1µ
C7 1µ
C8 1µ
C9 1µ
C10 1µ
C11 1µ
C12 1µ
C13 1µ
D1 IN914
0 CHAN.
1
2
3
4
5
6
7
8
9
EMERG INDICATOR
DATA AVAIL
EXT. C
KBM
GND
POL
CLK
KEYBOARD ENCODER
0
1
2
3
4
5
6
7
8
9
E
F
R
AUDIO EMERGENCY SWITCH-OVER AND CONTROL FOR STORED DISPLAY

NOTES 1 UNLESS OTHERWISE SPECIFIED
a) ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W
b) ALL CAPACITOR VALUES ARE IN FARADS

2-227

| REV. NO | REVISION | DATE | APPD BY |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 10 03 83 | |
| B | REVISED | 12 02 82 | JC/ |
| A | REVISED | 16 11 81 | MP/ |

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

DRAWN RP DATE MAY 7/81 CHECKED

BAYLY ENGINEERING LTD a member of

TITLE SCHEMATIC KEYBOARD ENCODER

DWG NO 66-0643 027 590 CD-C 01

### 2.6.14 Frequency Display Decoder

The FREQUENCY DISPLAY DECODER card is used in the Operator's and Receiver control consoles to drive the 6-digit display showing the receiver's current operating frequency (frequency selection mode only).

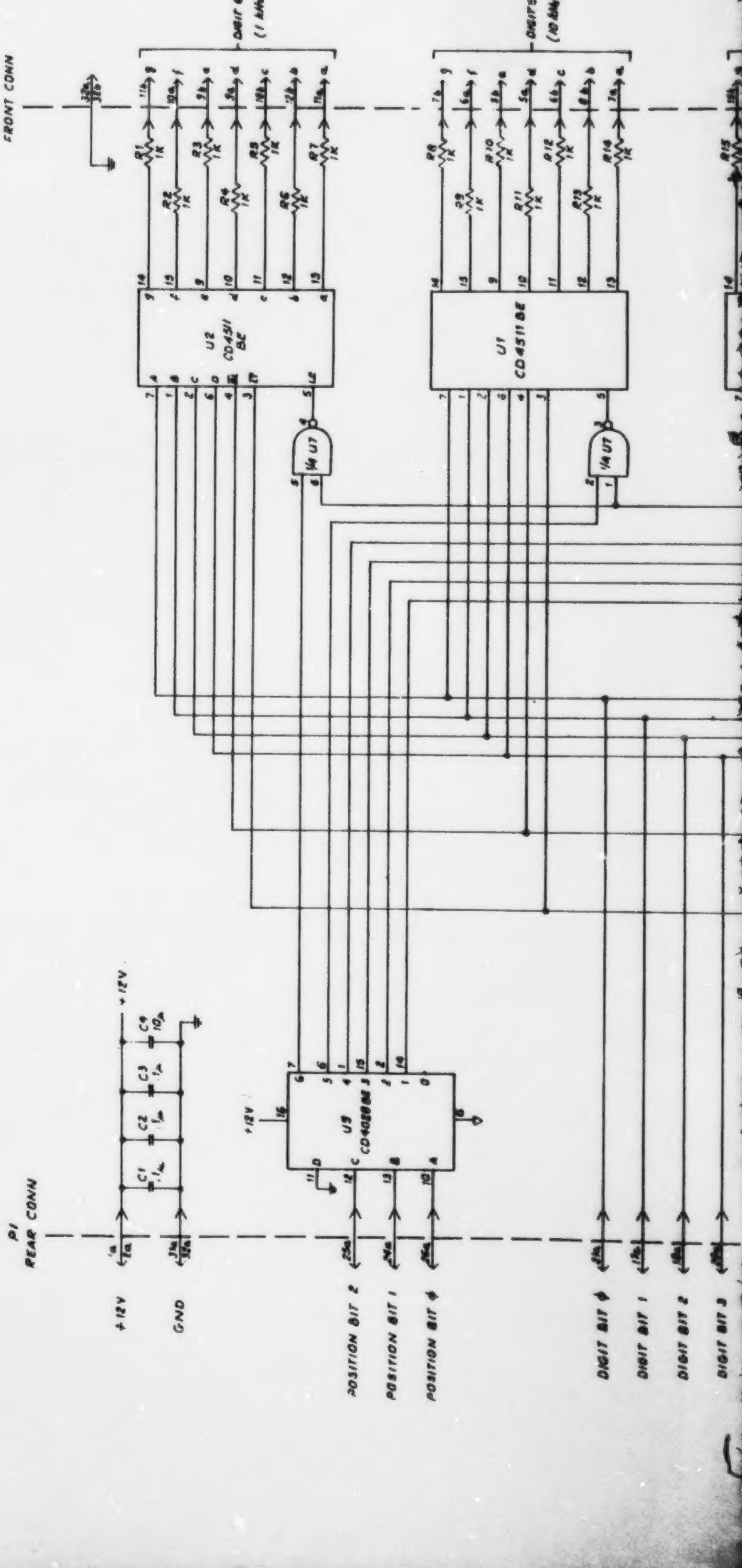
The circuit is designed to accept the signals in the form in which they are transmitted over the data link, i.e. a 4-bit digit code determines the value of the digit displayed, while a 3-bit position code determines which of the six digits is to be addressed.

The 3-bit position code is fed to U9, a 4028 BCD-to-Decimal Decoder which translates the binary code to a unique decimal digit (1 to 6; the digit 0 means that the channel display is selected and thus the digit code transmitted at the same time would have no meaning to the frequency display).

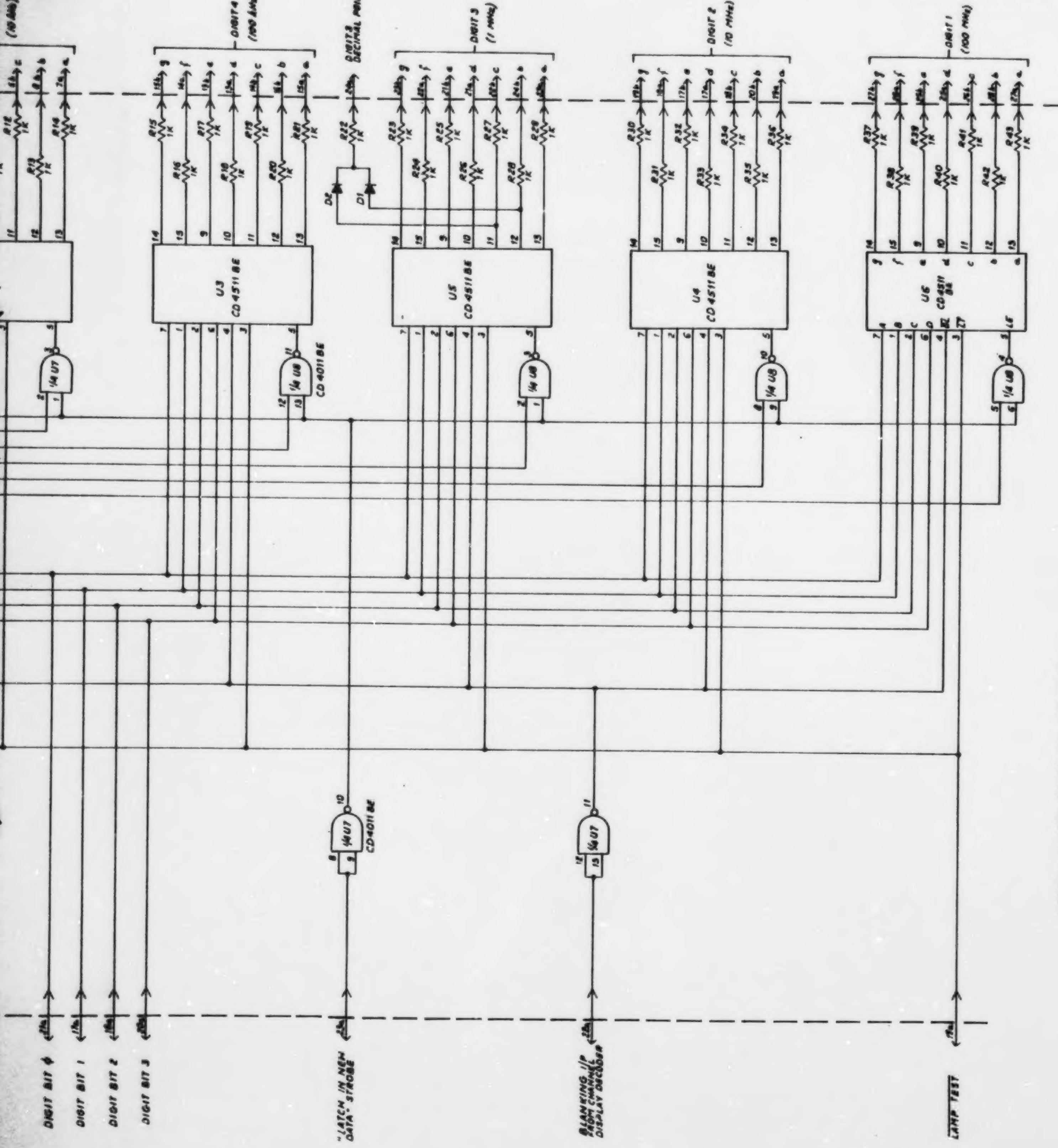
Six 4511 BCD-to-7 segment latch/decoder/drivers (U1 to U6) are used to drive the 7-segment LED displays. Inputs, A, B, C and D are the BCD inputs. The 4-bit position code is fed to all decoders simultaneously, but only the unit whose LE (= latch enable) input is low will store the information. BCD codes from 0 to 9 are acceptable, but any other code causes the display to be blanked, a feature which is used to blank the display when the frequency RESET button is pressed on the front panel. In digit #3, the decimal point is also driven by one or both of the segment 'b' or 'c' outputs (for any digit, at least one of these two is high) so that it is lit when this digit is energized.

The decoders also have a special BL (= blanking) input which is used to blank the display when the unit is in the Channel Select mode and also to vary the display intensity by applying a variable duty cycle pulse train from the intensity control. The LT (= lamp test) input causes all 7 segments to be lit with full brightness, regardless of any other input.

Two sections of U7 are used to invert the latching strobe and blanking input, while the other two sections, as well as all four sections of U8, are used to route the latching strobe to the desired decoder.


J1 FRONT CONN
DIGIT 6 (1 kHz)
DIGIT 5 (10 kHz)
U2 CD4511 BE
U1 CD4511 BE
1/4 U7
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
R6 1K
R7 1K
R8 1K
R9 1K
R10 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15
U3 CD4028BE
+12V
C1 .1
C2 .1
C3 .1
C4 10
P1 REAR CONN
+12V
GND
POSITION BIT 2
POSITION BIT 1
POSITION BIT 0
DIGIT BIT 0
DIGIT BIT 1
DIGIT BIT 2
DIGIT BIT 3

66-0643 027 480 CD-C


DIGIT 4 (100 kHz)
DIGIT 3 DECIMAL POINT
DIGIT 3 (1 MHz)
DIGIT 2 (10 MHz)
DIGIT 1 (100 MHz)
R12 1K
R13 1K
R14 1K
R15 1K
R16 1K
R17 1K
R18 1K
R19 1K
R20 1K
R21 1K
R22 1K
R23 1K
R24 1K
R25 1K
R26 1K
R27 1K
R28 1K
R30 1K
R31 1K
R32 1K
R33 1K
R34 1K
R35 1K
R36 1K
R37 1K
R38 1K
R39 1K
R40 1K
R41 1K
R42 1K
R43 1K
D1
D2
U3 CD4511BE
U5 CD4511BE
U4 CD4511BE
U6 CD4511 BE
1/4 U7
1/4 U8
CD4011BE
DIGIT BIT 0
DIGIT BIT 1
DIGIT BIT 2
DIGIT BIT 3
"LATCH IN NEW DATA" STROBE
BLANKING I/P FROM CHANNEL DISPLAY DECODER
LAMP TEST

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ¼W
2. ALL CAPACITOR VALUES ARE IN FARADS

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV. NO. | REVISION | DATE | APPD BY |
|---|---|---|---|
| | | | |
| | | | |
| 01 | PROTOTYPE RELEASE | 24 02 83 | MR/ |
| — | RELEASED | 17 DEC 81 | |

DRAWN BY: V S | DATE: FEB. 9 81 | CHECKED BY: | APPD BY: | STRS

**BAYLY** ENGINEERING LTD a member of

TITLE: SCHEMATIC DIAGRAM
FREQUENCY DISPLAY DECODER & DRIVER

DWG NO 66-0643. 027 480 CD-C | 01

## 2.7 AUDIO AND DATA TRANSMISSION

**Index**

2.7.1 DF Audio/Communications

2.7.2 High/Low Filter

2.7.3 Hybrid 2/4 Wire

2.7.4 Frequency Shift Key

2.7.5 Serial to Parallel Converter

2.7.6 Data Converter

### 2.7.1 DF Audio/Communications

The Audio/Communications board has four functions in the system:

(a) It has the Hybrid Transformer (T1) which is used to change the balanced incoming telephone line into the unbalanced configuration needed internally in the system.

(b) It has the audio amplifier (U1 and associated circuitry) to amplify the incoming voice signal for the loudspeaker and earphone jack, as well as the 600 Ohm line for remote monitoring.

(c) It has the mixer for the outgoing voice and data (U2) as well as the line driver for the outgoing 2-wire line.

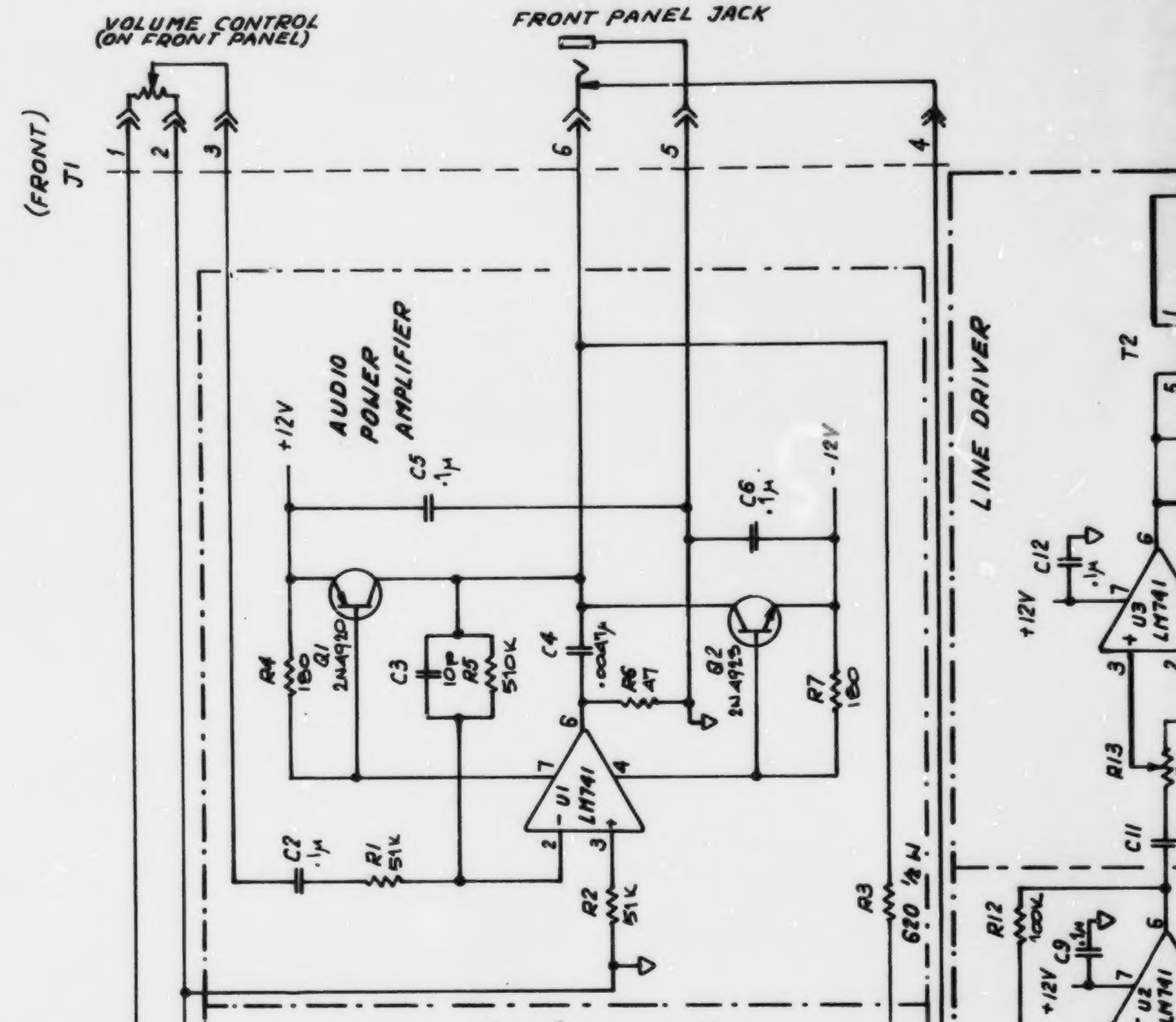
(d) It has a low-pass filter to remote the high frequency components from the outgoing voice before it reaches the mixer, so that it cannot interfere with the data transmission.

The tap on the primary of hybrid transformer T1, as well as the capacitor C1, allows DC signalling on the incoming line.

The incoming voice (separated from the data/voice signal by the Hi-Lo Filter elsewhere in the system) is brought onto the board on rear connector pin #3. It is fed straight through to the front connector pin #1 and taken to the VOLUME control on the front panel. The slider of the control returns on pin #3 and is taken to the input of the op-amp U1 (pin #2). Power transistors Q1 and Q2 boost the output of the op-amp so that it can drive a loudspeaker.

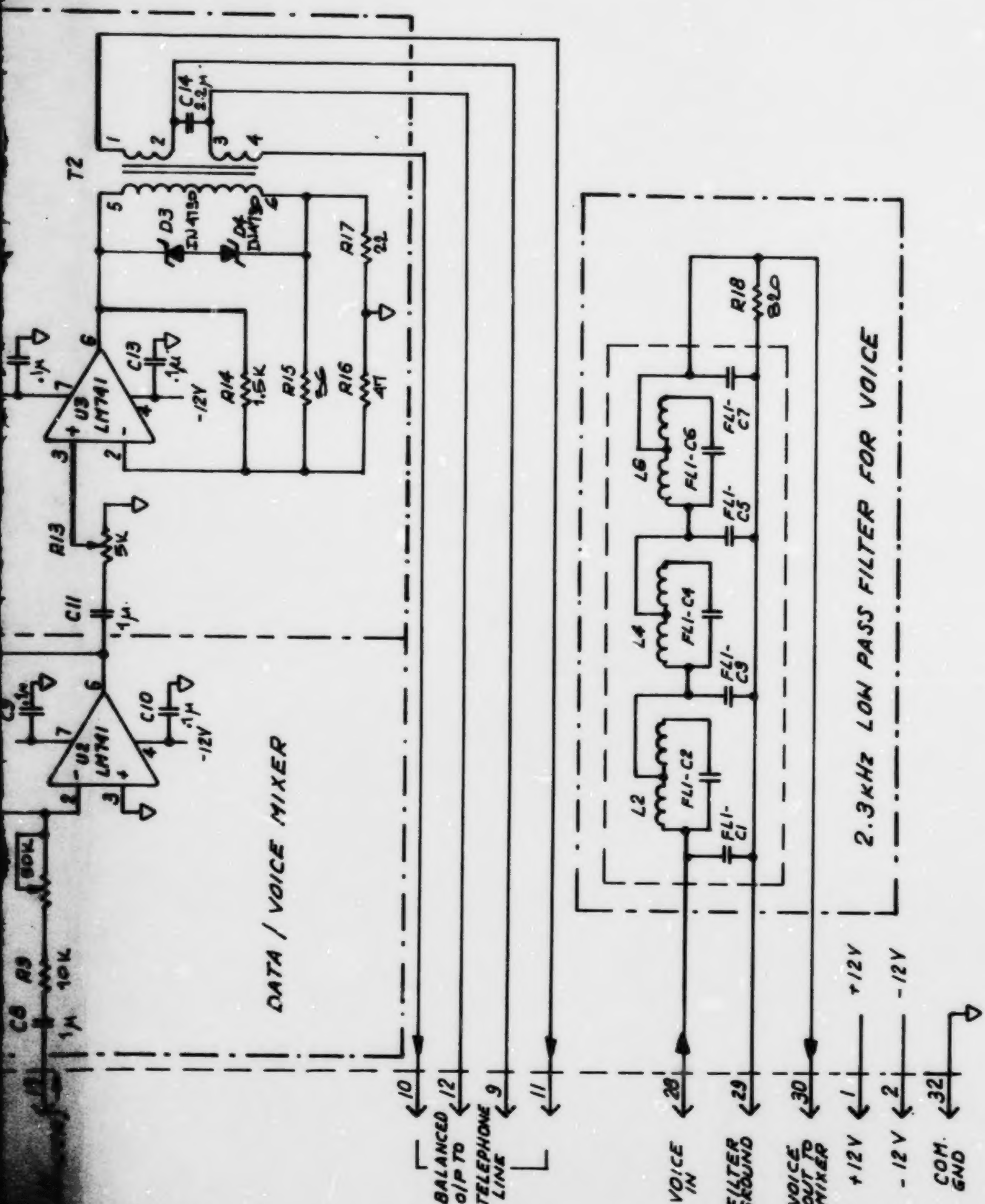
Data to be transmitted (using FSK transmission) is brought to pin #17 of the rear connector and fed to the input of the mixer op-amp U2. R10 is a level control for the data stream. Voice to be transmitted is brought to rear connector pin #28 and passed through the low-pass filter (L2, L4, L6 and associated capacitors) from where it is fed to the other input of the mixer amplifier. R1ˉ is the level control for the voice.

R13 is an overall level control for the outgoing signal and U3, with its associated components, forms the line driver. This amplifier is a somewhat unconventional design which will simulate a 600 Ohm source impedance while it still provides an almost +12V to -12V signal swing if driven high enough. A hybrid transformer (T2) provides coupling for the balanced outgoing line with the tap in the secondary winding, together with C14, allowing for DC signalling between stations.


VOLUME CONTROL (ON FRONT PANEL)
FRONT PANEL JACK
(FRONT) J1
1
2
3
6
5
4
AUDIO POWER AMPLIFIER
+12V
-12V
C5 .1µ
C6 .1µ
R4 180
Q1 2N4920
C3 10p
R5 510K
C4 .0047µ
R6 47
Q2 2N4923
R7 180
U1 LM741
7
6
4
2
3
C2 .1µ
R1 51K
R2 51K
R3 620 ½W
LINE DRIVER
T2
C12 .1µ
+12V
U3 LM741
R13
C11
R12 100K
C9 .1µ
U2 LM741
R10 50K
R11 50K
R8 10K
R9 10K
C7 1µ
C8 1µ
D1 1N4730
D2 1N4730
T1
C1 2.2µ
TRANSFORMER FOR INCOMING LINE
(REAR) P1
3
4
8
16
7
13
15
14
6
5
17
18
AUDIO IN
AUDIO GROUND
TO HI/LO FILTERS
TEL. LINE
600Ω AUDIO O/P
SPEAKER O/P
DATA (FSK) IN
VOICE IN (FROM L.P. FILTER)

This drawing is the property of BAYLY ENGINE
LIMITED and may be neither used, copied, repro
or otherwise dealt with nor its contents communica
others without written permission.

66-0643. 029 368. CD-B



DATA / VOICE MIXER
T2
C14 2.2µ
D3 IN4130
D4 IN4130
R17 22
R18 820
R14 1.5K
R15
R16 47
C13 .1µ
-12V
U3 LM741
R13 5K
C11 .1µ
U2 LM741
C10 .1µ
C9
R9 10K
50K
C8 1µ
2.3kHz LOW PASS FILTER FOR VOICE
L2
L4
L6
FL1-C1
FL1-C2
FL1-C3
FL1-C4
FL1-C5
FL1-C6
FL1-C7
10
12
9
11
28
29
30
1
2
32
BALANCED O/P TO TELEPHONE LINE
VOICE IN
FILTER GROUND
VOICE OUT TO MIXER
+12V
-12V
COM. GND

NOTES: 1. UNLESS OTHERWISE SPECIFIED
a. ALL RESISTOR VALUES ARE IN OHMS
b. ALL CAPACITOR VALUES ARE IN FARADS

2-232

| | | | |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| 01 | PROTOTYPE RELEASE | 24.02.83 | K/ |
| REV NO | REVISION | DATE | APPR BY |

DRAWN I. CLARK DATE JUNE 25.81. CHECKED BY APPD BY

**BAYLY** ENGINEERING LTD a member of

TITLE SCHEMATIC DIAGRAM
AUDIO COMMUNICATION DOPPLER DF.

DWG NO. 66-0643. 029 368. CD-B 01

### 2.7.2 **High/Low Filter**

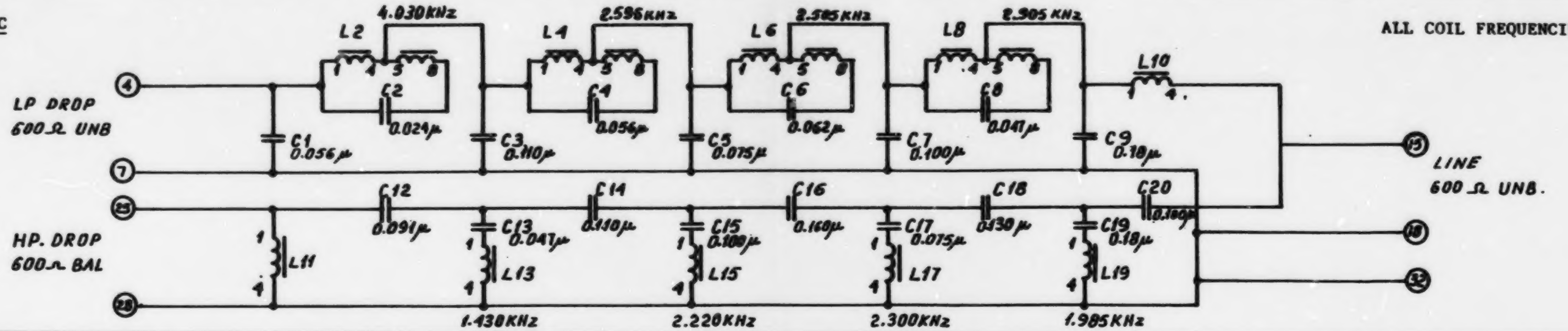
The HIGH/LOW FILTER card is used in Operator and Receiver Control panels to separate the voice and data (FSK) signals which are transmitted over the same telephone line.

Passive filters with fairly steep roll-off characteristics are used on this card. The high-pass filter has a cut-off frequency of about 2500 Hz and a rejection of better than 60 dB for frequencies of 2300 Hz or lower, i.e. the entire range used for voice transmission. The output of the high-pass filter is passed on to the FSK DETECTOR card.

The low-pass filter has a cut-off frequency of about 2300 Hz and a rejection of better than 60 dB for the frequencies used for data transmission. The output of the low-pass filter goes to the audio amplifier and/or the telephone set.

## 1.0 FILTER SCHEMATIC

ALL COIL FREQUENCIES IN KHZ


4.030KHz
L2
1
4
5
8
C2
0.024µ
2.596KHz
L4
C4
0.056µ
2.585KHz
L6
C6
0.062µ
2.305KHz
L8
C8
0.047µ
L10
1
4
④
LP DROP
600Ω UNB
⑦
C1
0.056µ
C3
0.110µ
C5
0.075µ
C7
0.100µ
C9
0.18µ
⑮
LINE
600Ω UNB.
㉕
HP. DROP
600Ω BAL
㉘
C12
0.091µ
C14
0.110µ
C16
0.160µ
C18
0.130µ
C20
0.160µ
C13
0.047µ
C15
0.100µ
C17
0.075µ
C19
0.18µ
L11
L13
L15
L17
L19
⑱
㉜
1.430KHz
2.220KHz
2.300KHz
1.985KHz

## 2.0 FILTER SPECIFICATION

2.1 INPUT IMPEDANCE: 600Ω UNBAL

2.2 OUTPUT IMPEDANCE: 600Ω UNBAL

2.3 AMPLITUDE RESPONSE

| FREQ. | LOSS IN DB | FREQ | LOSS IN DB |
|---|---|---|---|
| LOW PASS | | HIGH PASS | |
| 1.0 KHz | ≤ 1.0dB | 3.0 KHz | ≤ 1.0dB |
| 2.275KHz | ≤ 3.0dB ↑ | 265 KHz | ≤ 1.0dB ↑ |
| 2.3 KHz | ≤ 3.5dB ↑ | 2.6 KHz | ≤ 1.5dB ↑ |
| 2.6 KHz<br>TO 10 KHz | ≥ 60dB ↑ | 300 KHz<br>TO 2.3KHz | ≥ 60 dB |

NOTES:

2.4 DELAY DISTORTION

| FREQ. | DELAY IN |
|---|---|
| | |

NOTES:

2.5 RETURN LOSS

| FREQ. | LOSS IN DB | FREQ | LOSS IN DB |
|---|---|---|---|
| | | | |

NOTES:

2.6 IMPEDANCE

| FREQ. | IMPEDANCE IN |
|---|---|
| | |

NOTES:

2.7 OTHER

## 3.0 FILTER TESTS

✓3.1 RESONATE COILS AND STRAP JUMPERS :

✓3.2 FREQUENCY RESPONSE :

3.3 IMPEDANCE :

3.4 RETURN LOSS :

✓3.5 SECURE ADJ. SCREWS :

✓3.6 HEAT CYCLE :

✓3.7 VISUAL INSPECTION :

3.8 OTHER :

3.9 EQUIPMENT :

2-234

FOR PARTS LIST SEE DWG. # 729-0643.031 510 -PL-A

FOR WOUND COMPONENT DATA SEE DWG. # 729-0643.031 510 -TCD.B

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV NO | REVISION | DATE | APPR. BY |
|---|---|---|---|
| - | | | |
| - | | | |
| 01 | RELEASED | | |

DRAWN BY M.R. DATE 23.11.81 CHECKED BY

BAYLY ENGINEERING LTD a member of

TITLE HIGH/LOW FILTERS 2.6KHz/2.3KHz

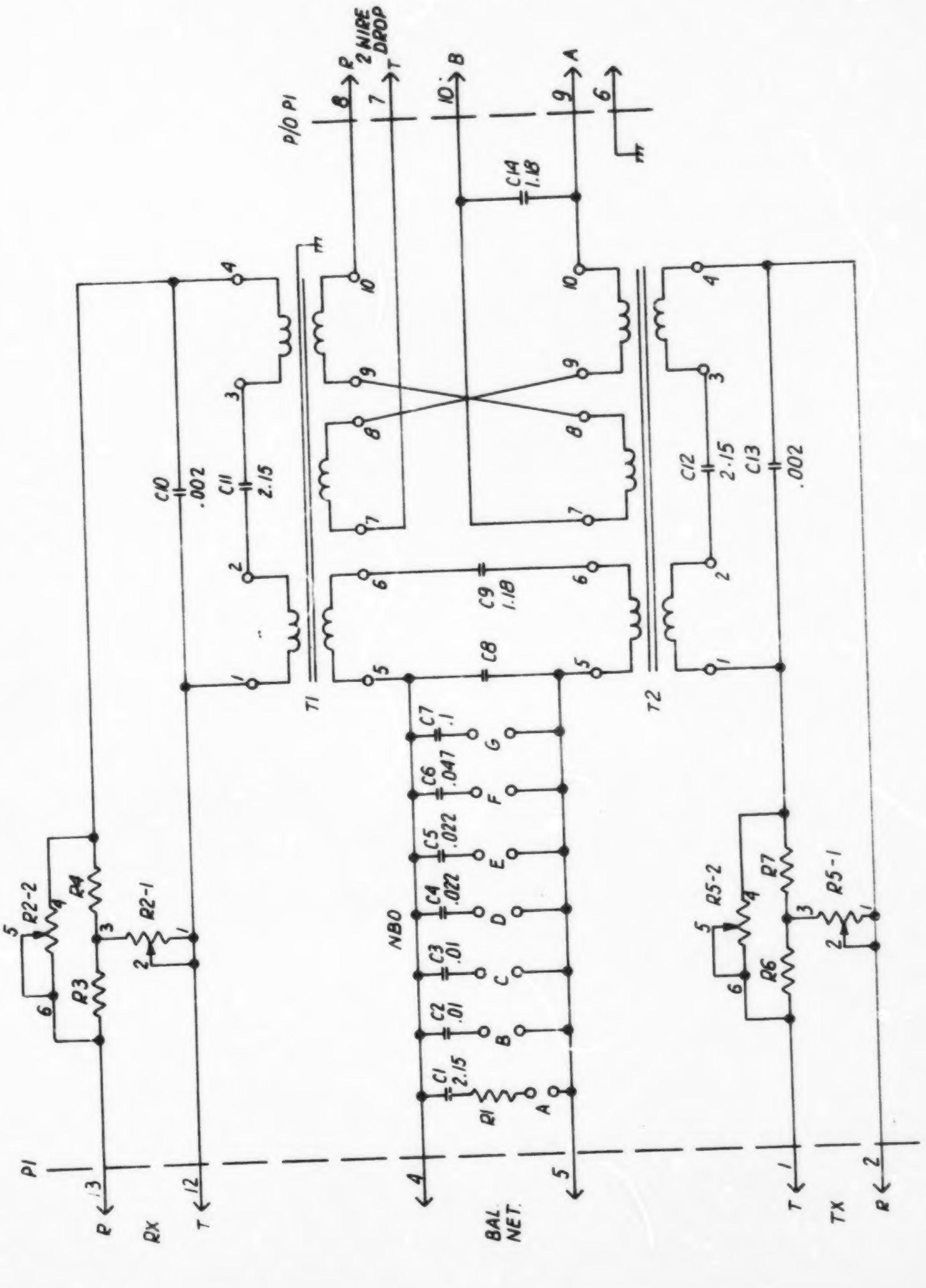
DRAWING NO. 729-0643.031 510 FL-B. 01

### 2.7.3 Hybrid 2/4 Wire

The hybrid 2/4 wire is a Bayly M6383 'terminal set'. This is a 'Toll' quality hybrid unit used for converting a four-wire transmission path to a two-wire circuit. The unit features compact construction, high return loss and trans-hybrid balance. The M6383 also features strappable NBO capacitance and two models offer a choice of strapping of continuous adjustment of through loss.

**Specifications**

| | | |
|---|---|---|
| Four-wire Impedance | : | 600 Ohms balanced |
| Two-wire Impedance | : | 600 Ohms/2 uF |
| NBO Capacitance | : | Strappable .01 to .21 uF, .01 uF steps |
| Through Loss | : | < 4 dB |
| Frequency Response | : | 20 Hz to 3500 Hz ±1 dB<br>500 Hz to 2500 Hz ±5 dB |
| Return Loss | : | 200-4000 Hz 24 dB |
| (2 wire line against 600 Ohms plus 2 F) | : | 750-4000 Hz 27 dB |
| Trans-hybrid Loss | : | > 50 dB |
| Tx and Rx Pads | : | Continuously adjustable |
| A and B Lead Current | : | 120 mA maximum |


P/O P1
8
7
10
9
6
R
T
2 WIRE DROP
B
A
C14
1.18
4
3
2
1
10
9
8
7
6
5
T1
T2
C10
.002
C11
2.15
C12
2.15
C13
.002
C9
1.18
C8
C7
.1
C6
.047
C5
.022
C4
.022
C3
.01
C2
.01
C1
2.15
R1
A
B
C
D
E
F
G
NBO
R2-2
R2-1
R3
R4
R5-2
R5-1
R6
R7
P1
13
12
4
5
1
2
R
T
RX
BAL. NET.
T
R
TX

**BAYLY ENGINEERING LTD.**

TITLE SCHEMATIC DIAGRAM
4 WIRE TERMINATING SET
TYPE M6383 LIST6

DRAWING NO. 22-0643.027 682.CD-A

| REV NO | REVISION | DATE | APPR. BY |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |

DRAWN BY J.C.
DATE JAN.12.81
CHECKED BY J.L.
APPR. BY

### 2.7.4 **Frequency Shift Keying Detector**

The 'Frequency Shift Keying Detector' is used in both the Receiver Unit and the Operator's CDU of the Quasi-Doppler DF System.

The FSK detector is used in the system to convert tone frequencies into logic signals, a high tone, 2794 Hz frequency corresponding to a logic 1 signal and a low tone, 2573 Hz frequency corresponding to a logic 0 signal.

The FSK detector card also contains a tone detecting circuit, which generates an audible alarm if FSK signals are lost as a result of telephone line damage or other disruption of the data link.

The circuit consists of an amplifier/limiter, two active band-pass filters and detectors, four amplifier/buffers, two transient filters, two logic interfaces and a tone detector/amplifier.

The received FSK tones (through pin 20), coming from the Hi-Lo Filter are amplified and limited in the 'amplifier/limiter' (U3 and associated components). The output of this limiter is supplied to the two 'active band-pass filters' (U1 and U4) as well as to the 'tone detector/amplifier' (U9).

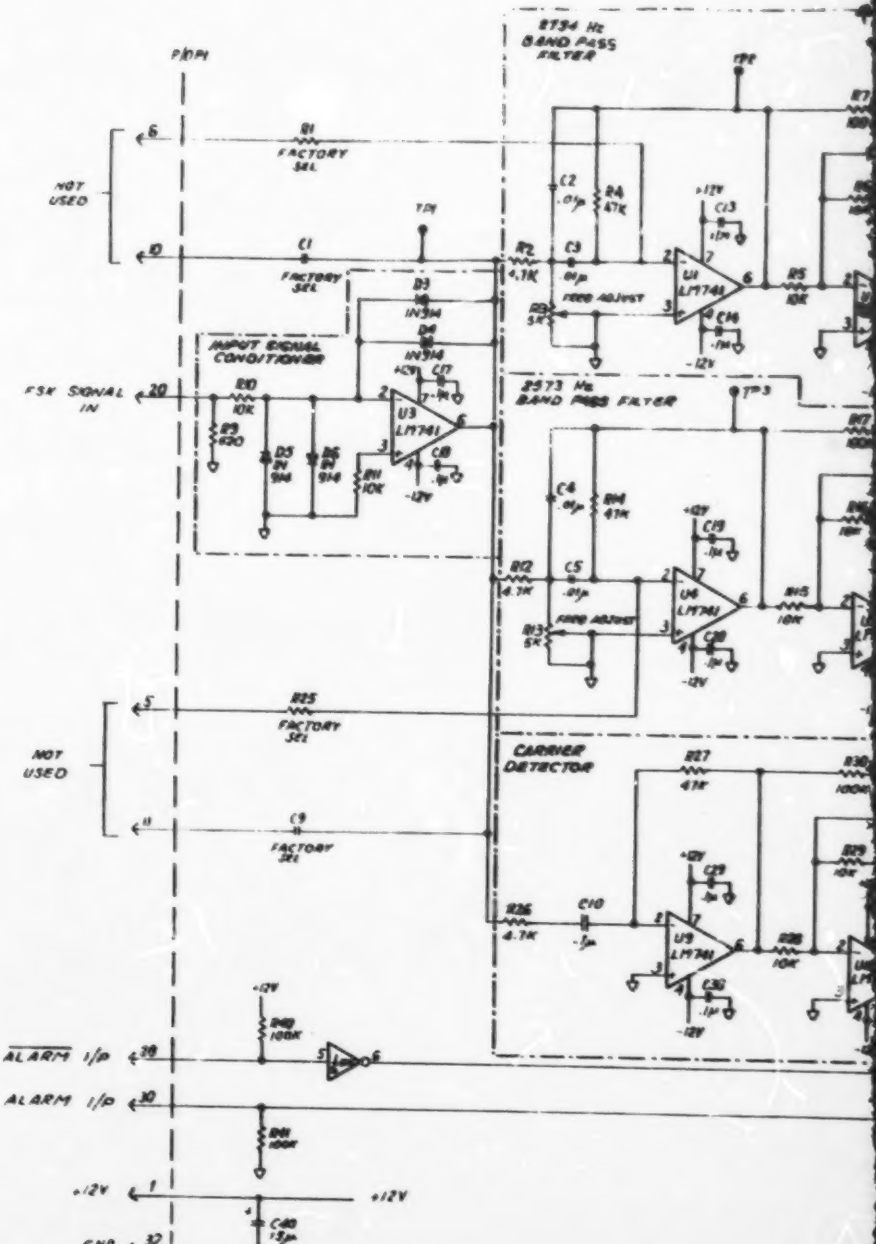
Only one active filter will pass a signal, depending on the frequency, 2794 Hz frequency using U1 and U2 filter/rectifier and 2573 Hz frequency using U4 and U5 filter/rectifier. Both band-pass filter outputs, negative (2573 Hz) and positive (2794 Hz) are connected together, hence, only the dominating output will be passed through the isolation stage. A buffer (U6) isolates and amplifies the dominant output signal from the band-pass filter to 12V. Once the signal has been isolated and amplified, a filter circuit (U7) eliminates the transient signals. A second amplifier/buffer (U8) once again buffers and amplifies the signal to plus or minus 12 volts. Resistor R23 is used to compensate for voltage offset.

The 'logic interface' (U14 pins 1 and 3) buffers the logic signal, then outputs it through the 'True Data' output (pin 26) to the Serial-to-Parallel Converter.

The 'tone detector/amplifier' continuously receives FSK tones from the 'amplifier/limiter' ensuring that the final output at the 'logic interface' (U14 pin 8) is low. This means that the output to the Control Board on pin 27 is low, thus inhibiting the alarm circuits.

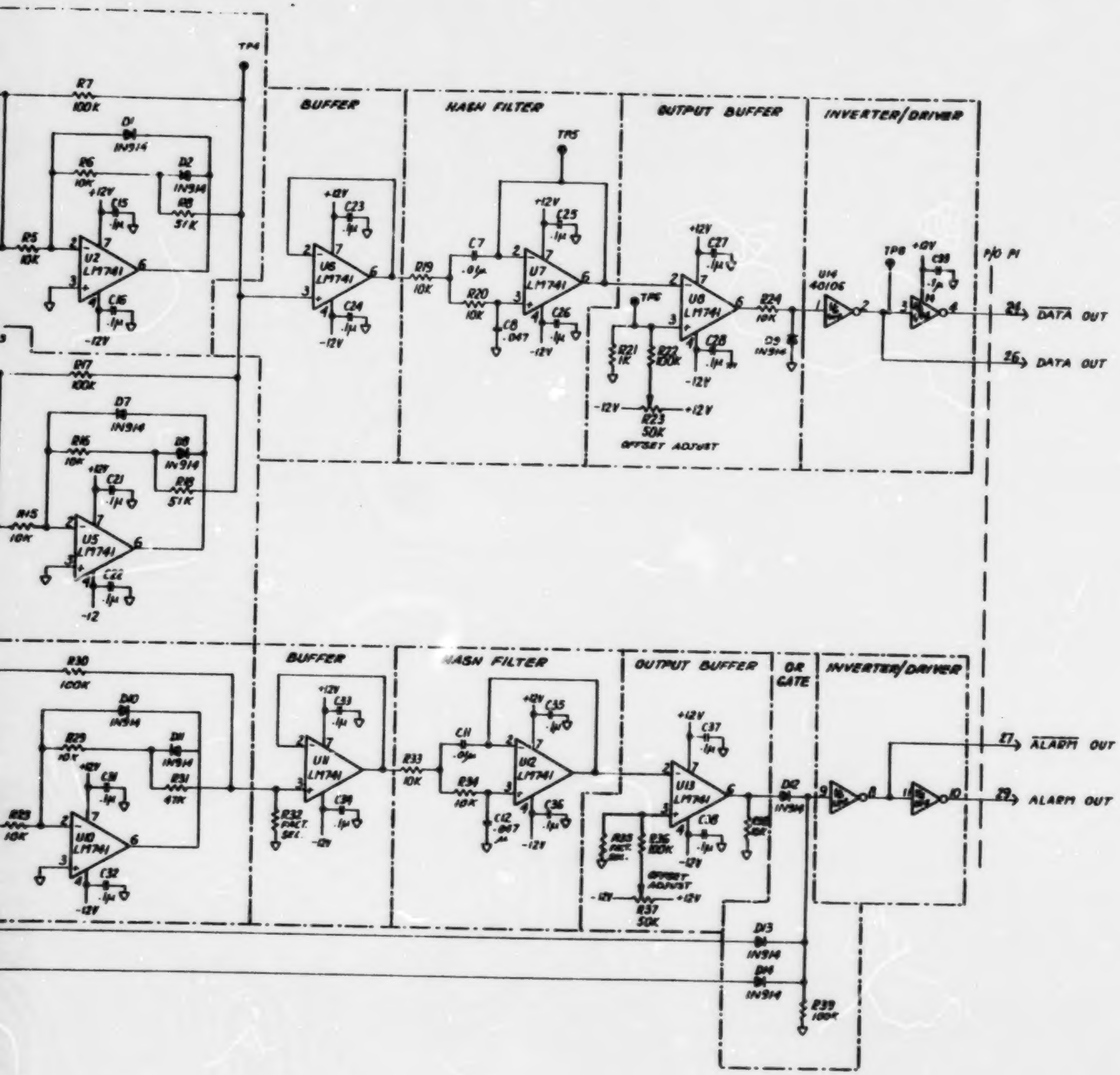
Should there be a disruption in FSK tones, the output from the 'logic interface' (U14 pin 10) goes high, causing a high output to the Control Board on pin 29. This triggers the alarm circuit.

Three diodes, D12, D13 and D14 form an OR gate for additional alarm inputs. A portion of U14 (pin 5) acts as an inverter, which allows the ground signals to trigger the alarm.


P1/J1
NOT USED
6
10
R1 FACTORY SEL
C1 FACTORY SEL
TP1
2734 Hz BAND PASS FILTER
TP2
C2 .01µ
R4 47K
R2 4.7K
C3 .01µ
R3 5K
FREQ ADJUST
U1 LM741
+12V
-12V
C13 .1µ
C14 .1µ
R5 10K
D3 1N914
D4 1N914
INPUT SIGNAL CONDITIONER
FSK SIGNAL IN
20
R10 10K
R9 620
D5 1N914
D6 1N914
U3 LM741
C17 .1µ
C8 .1µ
R11 10K
2573 Hz BAND PASS FILTER
TP3
C4 .01µ
R14 47K
R12 4.7K
C5 .01µ
R13 5K
U4 LM741
C19 .1µ
C20 .1µ
R15 10K
NOT USED
5
11
R25 FACTORY SEL
C9 FACTORY SEL
CARRIER DETECTOR
R27 47K
R26 4.7K
C10 .1µ
U9 LM741
C29 .1µ
C30 .1µ
R28 10K
R30 100K
R29 10K
ALARM I/P
ALARM I/P
28
30
R40 100K
R41 100K
+12V
1
GND
32
-12V
3
C40 15µ
C41 15µ
+12V
GND
- 12V

NOTES 1. UNLESS OTHERWISE SPECIFIED
a) ALL RESISTOR VALUES ARE IN OHMS ±5%, ¼W
b) ALL CAPACITOR VALUES ARE IN FARADS

66-0643 028 122 CD-C



TP4
R7 100K
D1 IN914
R6 10K
D2 IN914
R8 51K
+12V
C15 .1μ
R5 10K
U2 LM741
C16 .1μ
-12V
R17 100K
D7 IN914
R16 10K
D8 IN914
R18 51K
C21 .1μ
R15 10K
U5 LM741
C22 .1μ
-12
R30 100K
D10 IN914
R29 10K
D11 IN914
R31 47K
C31 .1μ
R28 10K
U10 LM741
C32 .1μ
BUFFER
U6 LM741
C23 .1μ
C24 .1μ
HASH FILTER
TP5
C7 .01μ
R19 10K
R20 10K
C8 .047
U7 LM741
C25 .1μ
C26 .1μ
OUTPUT BUFFER
TP6
U8 LM741
C27 .1μ
C28 .1μ
R21 1K
R22 100K
R23 50K
OFFSET ADJUST
R24 10K
D9 IN914
INVERTER/DRIVER
U14 40106
TP8
+12V
C38 .1μ
P/O P1
24 DATA OUT
26 DATA OUT
BUFFER
U11 LM741
C33 .1μ
C34 .1μ
R32 FACT. SEL.
HASH FILTER
C11 .01μ
R33 10K
R34 10K
C12 .047
U12 LM741
C35 .1μ
C36 .1μ
OUTPUT BUFFER
U13 LM741
C37 .1μ
C38 .1μ
R35 FACT. SEL.
R36 100K
OFFSET ADJUST
R37 50K
OR GATE
D12 IN914
INVERTER/DRIVER
27 ALARM OUT
29 ALARM OUT
D13 IN914
D14 IN914
R39 100K

2-238

| | | | |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 24 02 83 | MM |
| 0 | REVISED | OCT 27.81 | I.C |
| REV NO | REVISION | DATE | APPD BY |

DRAWN BY A SMITH DATE MAR 17.81 CHECKED BY

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

BAYLY ENGINEERING LTD a member of

TITLE SCHEMATIC DIAGRAM
FSK DECODER

DWG NO. 66-0643. 028 122.CD-C 01

### 2.7.5 Serial-to-Parallel Converter

The SERIAL-TO-PARALLEL CONVERTER card is used in the Receiver Console and the Operator's Console to convert the serial format data from the FSK Decoder to the parallel form used internally by the consoles.

The heart of the circuit consists of four CD4015 Serial In/Parallel Out shift registers U9 to U12. The parallel outputs are fed to a series of CD4042 latches (U1 to U8) where they are stored for subsequent processing.

A 416.67 Hz clock (derived from the 1.76 MHz system master clock) ensures proper sampling of the serial data stream and a series of delay circuits and pulse generators controls the operation of the latches and appropriate functions in the rest of the system.

The operation of the circuit is as follows:

A RESET pulse resets the shift registers so that all internal registers and outputs are set low. Pin 12 of U17 is high which, via U18, keeps pin 11 (the RESET input) of U20 high and inhibits the generation of the 416.67 Hz clock. Thus, this section of U17 acts as a start/stop control for the clock.

The first bit (or Start Bit) in any new block of serial data is always high. When this first bit is detected by pin 11 of U17, pin 12 goes low and frees the main divider U20. U21, in conjunction with two sections of U19 and one section of U18, is connected to divide the 1.76 MHz clock by 2112, resulting in an 833.33 Hz clock. This is further divided by 2 in the second section of U17 to derive the 416.67 Hz required by the shift registers. The idea of this arrangement is to sample the first (and all subsequent) pulses at the approximate centre of the pulse.

All 32 bits in the data stream are thus shifted through the registers until the start bit appears on pin 10 of U12. When this happens, it is passed through a delay circuit (½ of U16) to ensure that the sampling and shifting in all registers is complete and it is then applied to pin 3 of U15 and pin 11 of U16. Bit 32, the Stop Bit, is applied to the RESET input of U15 (pin 4 via ¼ of U18) which inhibits any action in U15. The second half of U16 finds a high level on its DATA input (pin 9) and thus generates a positive pulse on Q (pin 13) and a negative pulse on Q (pin 12).

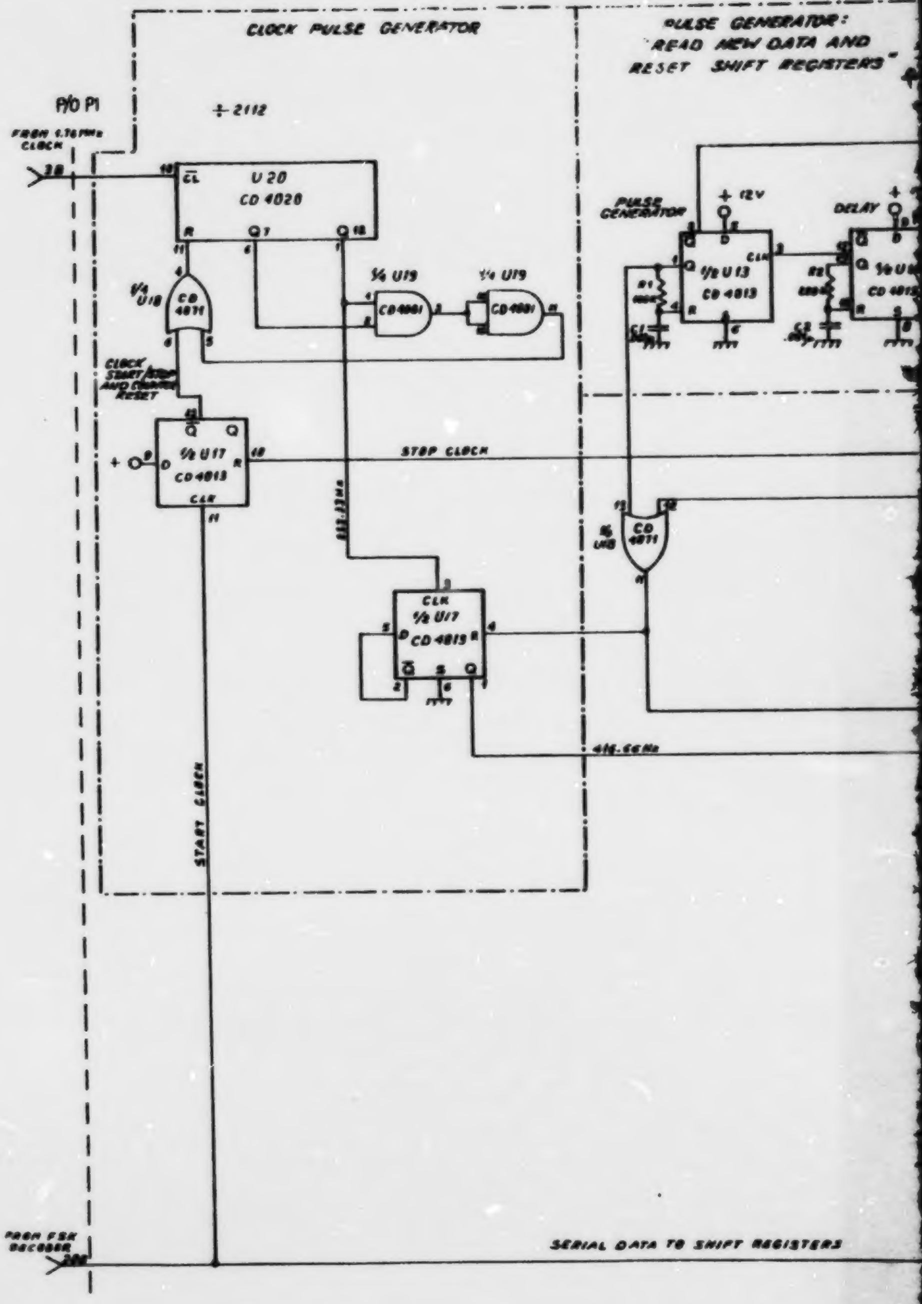
The negative going pulse is used as a strobe to tell the STORED DISPLAY circuit to read the information on the outputs of the latches before the new information on the outputs of the shift registers is stored in the latches and the previous information is obliterated.

The positive going pulse, via ¼ of U18, resets the clock start/stop control (½ of U17) and thus stops the 416.67 Hz clock so that no further sampling and shifting can take place in the shift registers.

If the Stop Bit had not been high, as might happen if the data stream was mutilated, or the circuit had been triggered by a signal other than a legitimate Start Bit, then the DATA input on U16 (pin 9) would not have been high and the pulses would not have been generated. At the same time, the Start/Stop Bit verification circuit (½ of U15) would not have been inhibited but would have generated a pulse which would have stopped the clock and reset all registers. This provides a form of data verification and error trapping by checking that the proper start and stop bits are present before the rest of the information is accepted. C8 and R8 on U15 act as a power-on reset for the entire circuit.

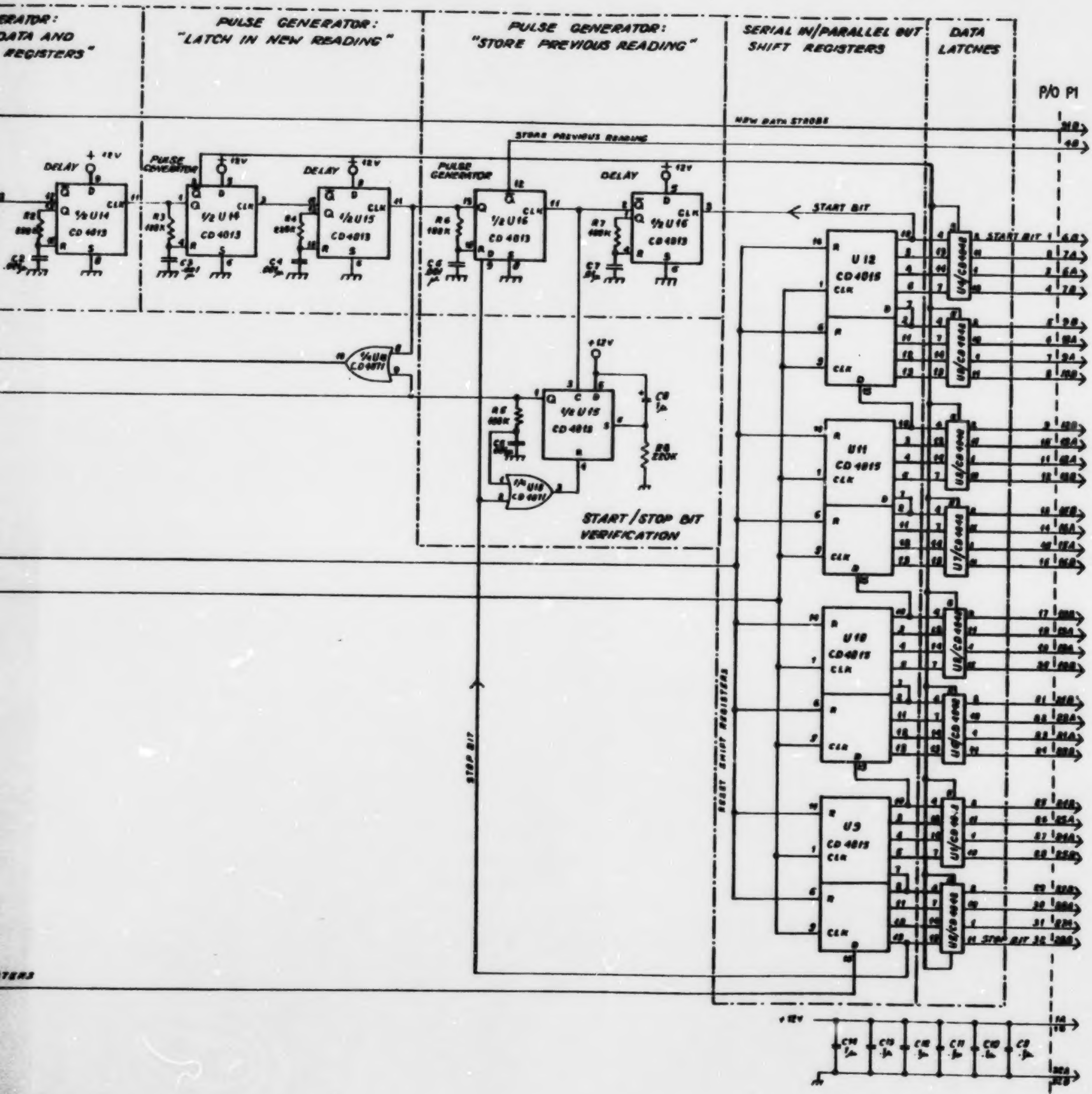
Returning to the positive pulse on pin 13 of U16, a second delay is introduced by the second section of U15, and then the (now delayed) pulse triggers another pulse generator (½ of U14). Again, a positive going and a negative going pulse is generated. The negative going pulse is used to transfer the new information from the shift registers into the latches, so that it is now available to the rest of the system.

The positive going pulse (pin 1 of U14) is delayed again by the other half of U14 and then triggers a third pulse generator (½ of U13). This circuit again generates a positive going and negative going pulse. The negative going pulse is the NEW DATA STROBE which tells the rest of the system that the new information is now available on the latches, while the positive going pulse resets the shift registers (via ¼ of U18) and also initializes the final divider for the 416.67 Hz clock. This divider (½ of U17) positions the latching pulse for the shift registers at the approximate centre of the incoming pulses.


CLOCK PULSE GENERATOR
PULSE GENERATOR:
"READ NEW DATA AND
RESET SHIFT REGISTERS"
P/O P1
÷ 2112
FROM 1.76MHz CLOCK
3B
CL
U 20
CD 4020
R
Q 7
Q 12
¼ U18
CD 4071
¼ U19
CD 4001
¼ U19
CD 4001
CLOCK START/STOP AND COUNTER RESET
Q
Q
½ U17
CD 4013
D
R
CLK
STOP CLOCK
833.33Hz
CLK
½ U17
CD 4013
D
R
Q
Q
S
416.66Hz
START CLOCK
PULSE GENERATOR
+ 12V
D
Q
½ U13
CD 4013
CLK
R
R1
C1
DELAY
R2
C2
½ U18
CD 4071
FROM FSK DECODER
SERIAL DATA TO SHIFT REGISTERS

NOTES: 1. UNLESS OTHERWISE SPECIFIED:
a. ALL RESISTOR VALUES ARE
b. ALL CAPACITOR VALUES ARE

66-0643 026 234.CD-C



...ERATOR:
...DATA AND
... REGISTERS"
PULSE GENERATOR:
"LATCH IN NEW READING"
PULSE GENERATOR:
"STORE PREVIOUS READING"
SERIAL IN/PARALLEL OUT SHIFT REGISTERS
DATA LATCHES
P/O P1
NEW DATA STROBE
STORE PREVIOUS READING
DELAY
PULSE GENERATOR
1/2 U14
CD 4013
1/2 U15
CD 4013
1/2 U16
CD 4013
1/4 U18
CD 4071
+12V
START BIT
STOP BIT
START/STOP BIT VERIFICATION
RESET SHIFT REGISTERS
U12
CD 4015
U11
CD 4015
U10
CD 4015
U9
CD 4015
U8/CD 4042
U7/CD 4042
CLK
START BIT
STOP BIT
C14
C13
C12
C11
C10
C9
...TERS

...E SPECIFIED:
...ALUES ARE IN OHMS ± 5% ¼ W
...ALUES ARE IN FARADS.

2-241

Without prior written consent of
BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| REV. | REVISION | DATE | APPD BY |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 24.03.82 | MM |
| – | RELEASED | JAN 5/82 | |
| A | CO & RD ADDED | DEC 10.81 | VB |

DRAWN N.P. DATE 81.10.1 CHECKED

BAYLY ENGINEERING LTD a member of

TITLE SCHEMATIC DIAGRAM
SERIAL TO PARALLEL CONVERTER

DWG NO 66-0643026 234.CD-C 01

### 2.7.6 **Data Converter**

The DATA CONVERTER card is used in the Receiver Console and the Operator's Console. It has three functions in the system:

(a) Generation of the 1.76 MHz master clock frequency.

(b) Parallel data to serial data conversion.

(c) Generation of the FSK tone frequencies for data conversion.

The 1.76 MHz master clock oscillator consists of one section of NOR gate U13 with a 1.76 MHz crystal in the feedback circuit and a second section of U13 acting as a buffer. This clock is used by the other two sections on the same card, as well as the SERIAL-TO-PARALLEL CONVERTER card.

Conversion of the data from parallel to serial format, suitable for transmission over the data link is accomplished by four cascaded CD4021 Parallel In/Serial Out Shift Registers (U1 to U4). The operation of the circuit is as follows:

A positive going clock pulse of sufficient length is applied to pin 7b on the edge connector (the CLK START). U12, together with two sections of U8, forms a Divide-by-2112 circuit which is constantly running. When Q12 on U12 (= pin 1) goes high, it is combined with the CLK START pulse in an AND Gate (¼ of U8) to provide a clock pulse for one section of U7 (pin 3). Pin 2 goes low and removes the reset condition from the Divide-by-2 circuit (the other section of U7), which will now provide a 16.67 Hz clock for the shift registers.

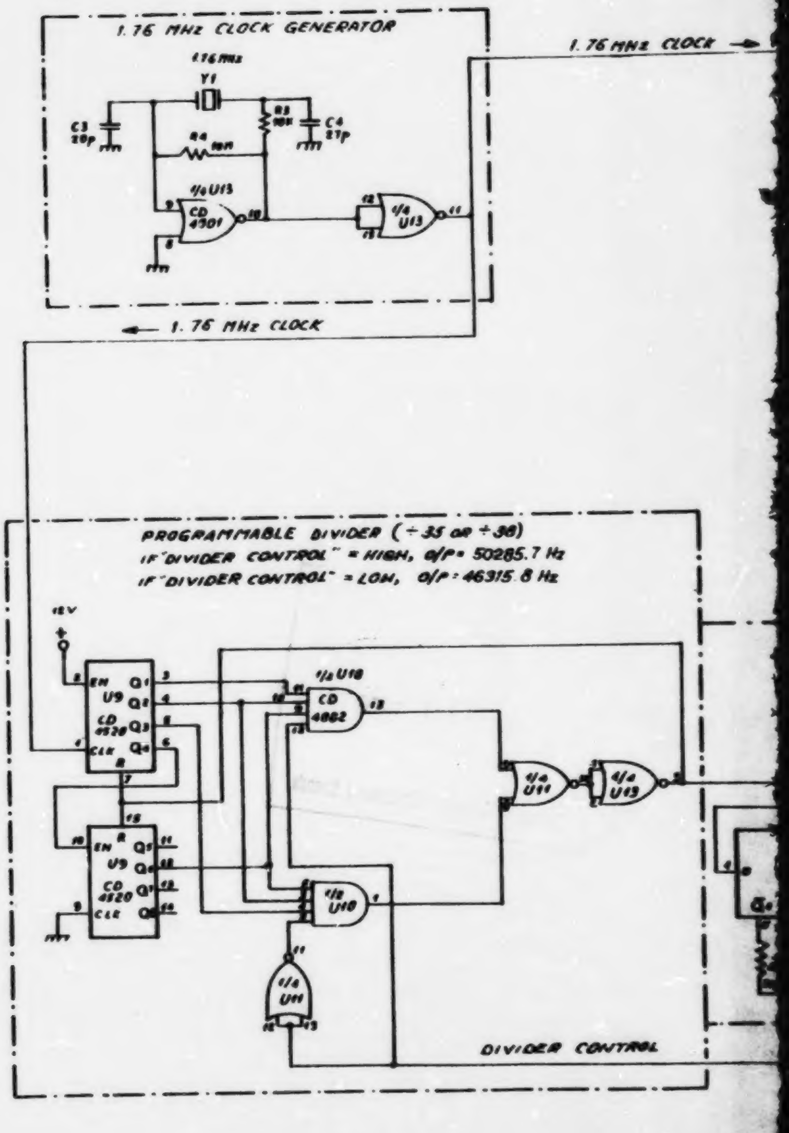
Pin 1 of U7 goes high at the same time and triggers a monostable (½ of U6) which provides the PARALLEL LOAD STROBE for the registers to load the parallel data into the internal registers of the CD4021's. As the 416.67 Hz clock pulses are applied to the shift registers, the whole 32 bits are gradually advanced through the registers and eventually are pushed out on pin 3 of U4 which forms the serial output for the circuit. Note that pin 1 of U4 (= Bit 1, or the Start Bit) and pin 7 of U1 (= Bit 32, or the Stop Bit) are tied permanently high

The 416.67 Hz clock output is also fed to U5, a second CD4020, which is wired to form a Divide-by-33 circuit. Note that the 4020 needs a negative going clock pulse, while the 4021's need a positive pulse. Since the Divide-by-2 circuit (½ of U7) is wired to provide a negative going pulse first, the Divide-by-33 circuit is one half cycle ahead of the shift registers. A monostable (½ of U6) detects the attempt to go to the 33rd step in the shifting clock and resets the clock on/off control (pin 4 of U7), thus disabling the clock to the shift registers after the 32nd pulse.

The circuit which generates the FSK tones consists of two sections: a programmable divider and the sine wave synthesizer.

The programmable divider consists of U9, U10, two sections of U11 and one section of U13. U9, a CD4520 Dual Binary Divider, has its two sections cascaded and the outputs are decoded by two 4-input AND gates (one section each of CD4082 = U10). The first section detects when a count of 35 is reached, while the second section looks for a count of 38. The 'Divider Control' line is low for a '0' level. This is inverted by one section of U11, which puts a high level on pin 2 of U10 and enables the divide-by-38 circuit. If the line is high (= a '1' level), then the divide-by-35 circuit is enabled. Thus, the 1.76 MHz clock is divided by 38 if the control line is low, and by 35 if the control line is high.

The sine wave synthesizer consists of two CD4018 5-stage counters, cascaded over an inverter (¼ of U13). The last output is fed back to the first Data input so that a ring counter is formed. Nine of the counter outputs are connected to a common line over selected resistors to generate an 18-step approximation of a sine wave. The frequency of the sine wave will be the clock frequency (from the programmable divider) divided by 18. Filtering inherent in the subsequent circuits and the telephone line will remove the high frequency components from the step function and a relatively pure sine wave results.

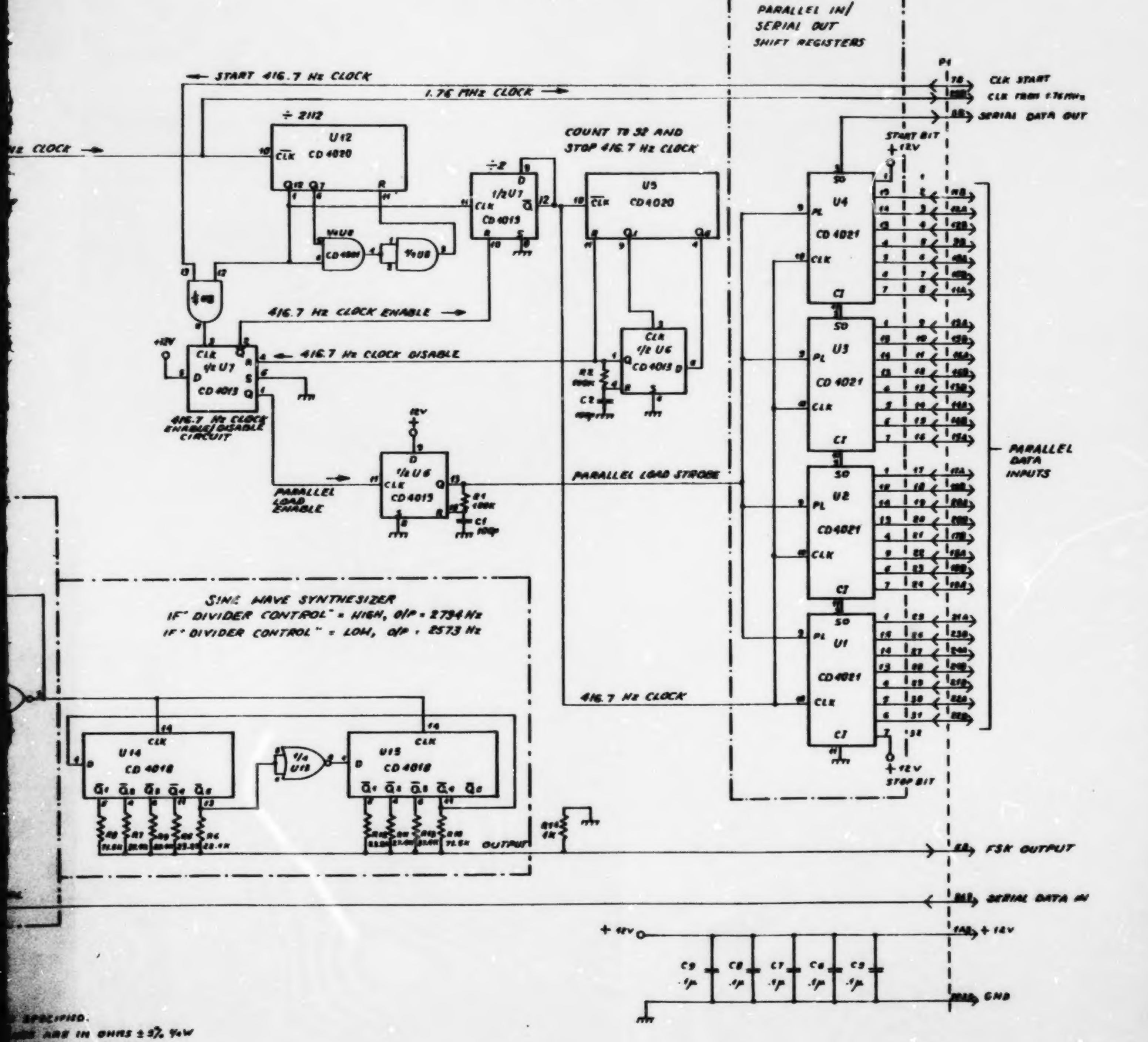

1.76 MHz CLOCK GENERATOR
1.76 MHz
Y1
C3
20p
R4
10M
R3
10K
C4
27p
1/4 U13
CD
4001
9
8
10
12
13
1/4
U13
11
1.76 MHz CLOCK →
← 1.76 MHz CLOCK
PROGRAMMABLE DIVIDER (÷35 OR ÷38)
IF "DIVIDER CONTROL" = HIGH, O/P = 50285.7 Hz
IF "DIVIDER CONTROL" = LOW, O/P = 46315.8 Hz
12V
EN
U9
CD
4520
CLK
Q1
Q2
Q3
Q4
R
2
1
3
4
5
6
7
15
10
9
11
12
13
14
EN
R
U9
CD
4520
CLK
Q1
Q2
Q3
Q4
1/2 U10
CD
4082
13
1/4
U11
1/4
U13
1/2
U10
1
1/4
U11
11
12
13
DIVIDER CONTROL
4
D
Q

NOTES: 1 UNLESS OTHERWISE SPECIFIED.

A. ALL RESISTOR VALUES ARE IN

B. ALL CAPACITOR VALUES ARE IN

66-0643.026 236CD-C


PARALLEL IN/ SERIAL OUT SHIFT REGISTERS
START 416.7 Hz CLOCK
1.76 MHz CLOCK
Hz CLOCK
÷ 2112
U12
CD 4020
÷2
1/2 U7
CD 4013
COUNT TO 32 AND STOP 416.7 Hz CLOCK
U5
CD4020
1/4 U8
CD 4081
416.7 Hz CLOCK ENABLE
416.7 Hz CLOCK DISABLE
+12V
1/2 U7
CD 4013
416.7 Hz CLOCK ENABLE/DISABLE CIRCUIT
1/2 U6
CD 4013
R2
C2
12V
1/2 U6
CD 4013
R1 100K
C1 100p
PARALLEL LOAD ENABLE
PARALLEL LOAD STROBE
416.7 Hz CLOCK
P1
CLK START
CLK FROM 1.76 MHz
SERIAL DATA OUT
START BIT +12V
U4 CD 4021
U3 CD 4021
U2 CD4021
U1 CD4021
SO
PL
CLK
CI
+12V STOP BIT
PARALLEL DATA INPUTS
SINE WAVE SYNTHESIZER
IF "DIVIDER CONTROL" = HIGH, O/P = 2734 Hz
IF "DIVIDER CONTROL" = LOW, O/P = 2573 Hz
U14
CD 4018
U13
CD 4018
1/4 U13
CLK
OUTPUT
R15 1K
FSK OUTPUT
SERIAL DATA IN
+12V
GND
C9 .1µ
C8 .1µ
C7 .1µ
C6 .1µ
C5 .1µ

SPECIFIED.
ARE IN OHMS ±5% ¼W
ARE IN FARADS.

Without prior written consent of BAYLY ENGINEERING LIMITED, this document may be neither used, copied, reproduced or otherwise dealt with, nor its contents communicated to others.

| | | | |
|---|---|---|---|
| 01 | PROTOTYPE RELEASE | 28.09.81 | 19 |
| — | RELEASED | JAN 7/82 | |
| REV NO | [illegible] | DATE | APPD BY |

DRAWN M.P. DATE 81.10.7 CHECKED

BAYLY ENGINEERING LTD

TITLE SCHEMATIC DIAGRAM DATA CONVERTER

DWG NO 66-0643.026 236CDC 01